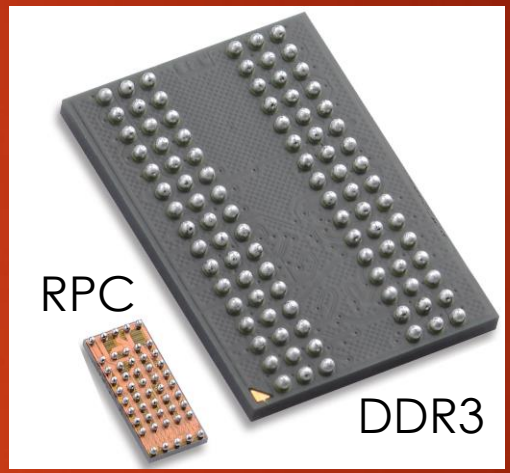
RPC DRAM Powerful & Miniaturized

What is **RPC DRAM®** and why does it matter?

- RPC DRAM
  - 256Mbits
  - High Bandwidth (DDR3 speed)
  - Half the pins of DDR3
  - 1/10 the PCB Footprint of DDR3
- Combined with ECP5 family in 285 csfBGA:
  - Area of two RPC DRAMs + 1 FPGA ~ same PCB space as 1 pc of x16 DDR3

RPC® vs DDR3
Same bandwidth
Half the IO pins
10% of PCB area

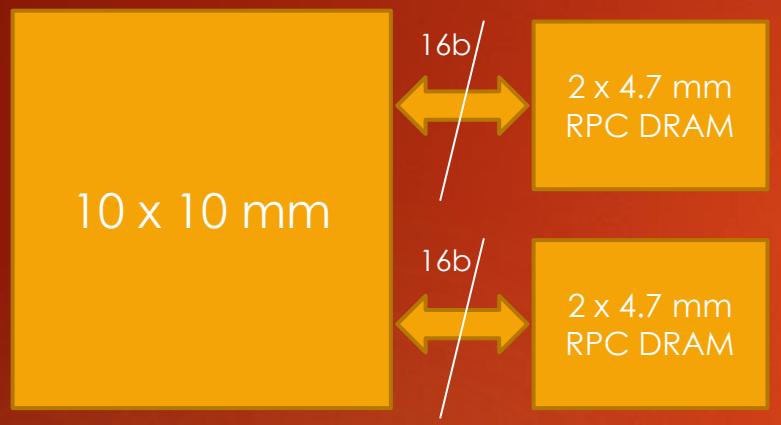


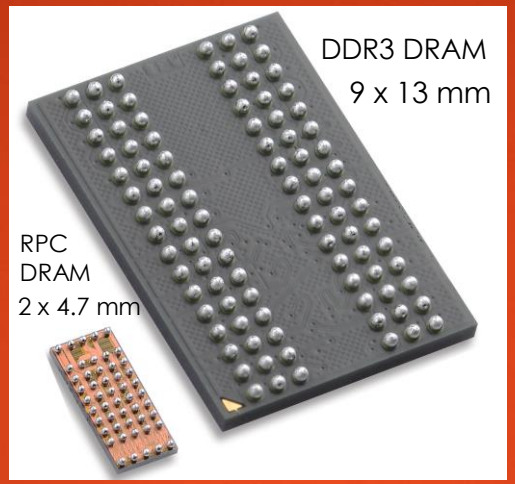
120 mm^2

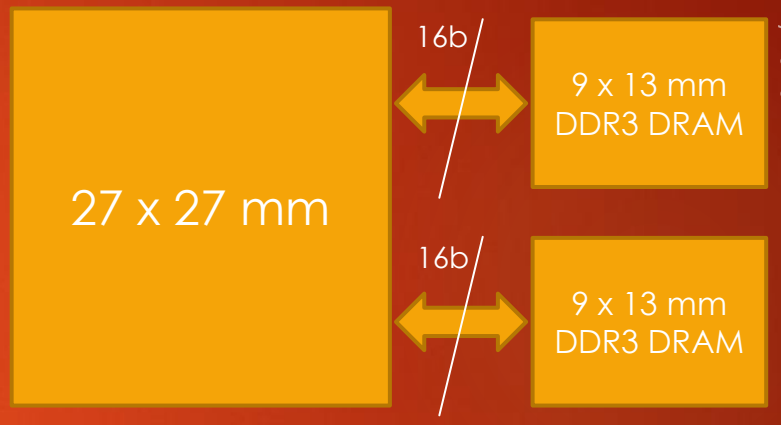
117 mm^2

DDR3
9 x 13 mm

Form factor Comparison





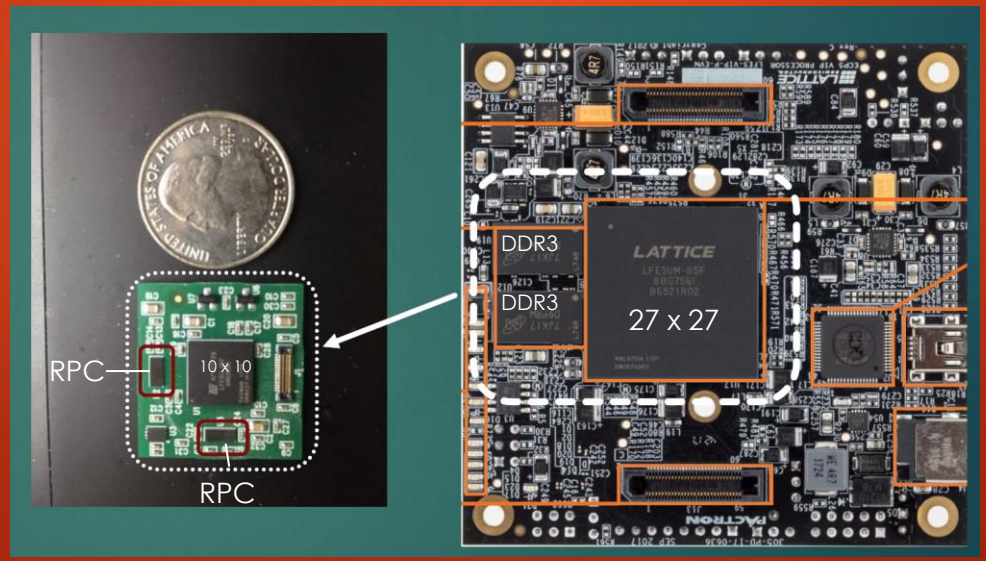


Minimum RPC cap'y: 256 Mbit/chip

Minimum DDR3 cap'y: 1 Gbit/chip

512 Mbits of RPC

1ea 10 x 10 mm ECP5 85K
(285 csfBGA)
2 pcs 2 x 4.7 mm RPC DRAM

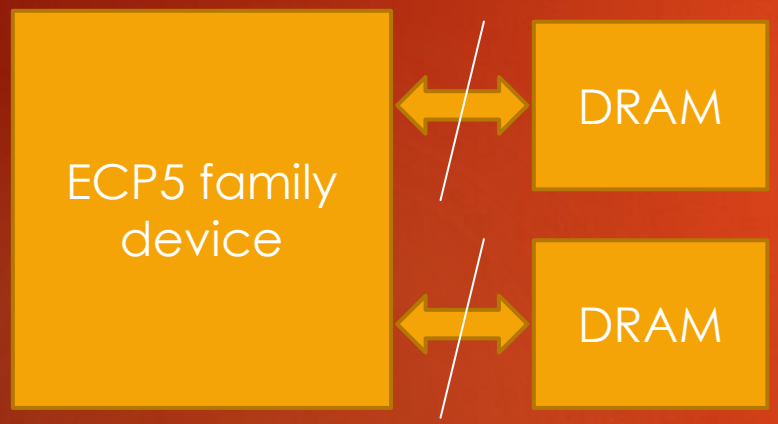


2 Gbits of DDR3
(4K application requires 272 Mbits)

1ea 27 x 27mm ECP5 85K
2 pcs 9 x 13 mm DDR3 DRAM

ECP5 4K Video Implementation

16 bits / channel
Up to DDR400 / channel



For Write/Read 4K at full bandwidth:
(need 2x incoming video rate at minimum)

Required memory bandwidth (write + read at video source rate):

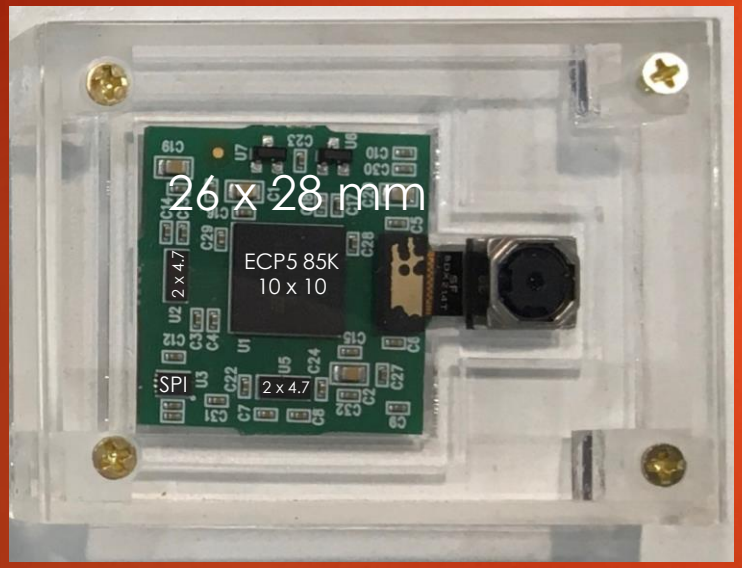
2 x 1024 Mbytes / sec = 2048 Mbytes /sec

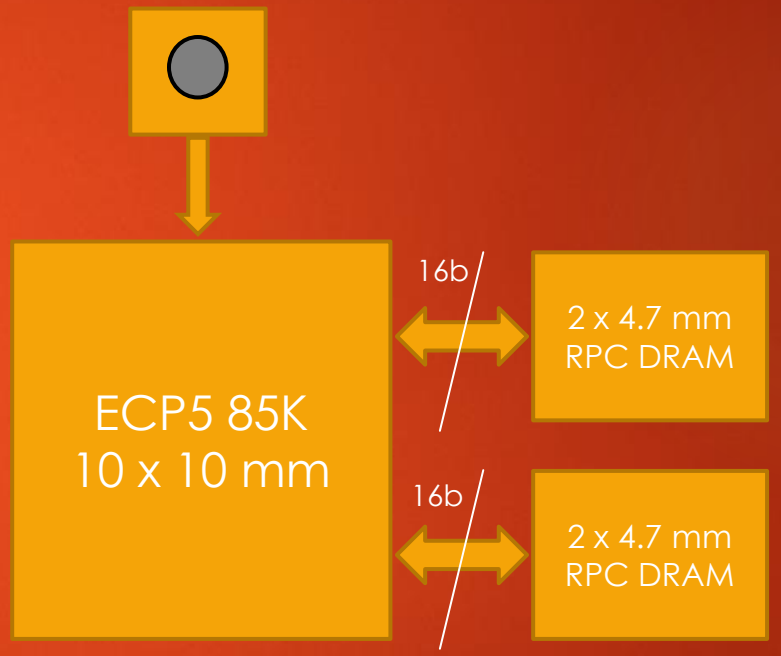
Memory DDR Clock Speed for 1 Channel:

1 channel @ 256 MHz provides 1024 Mbytes/sec: half of what's needed: must use 2 channels @ 256 MHz

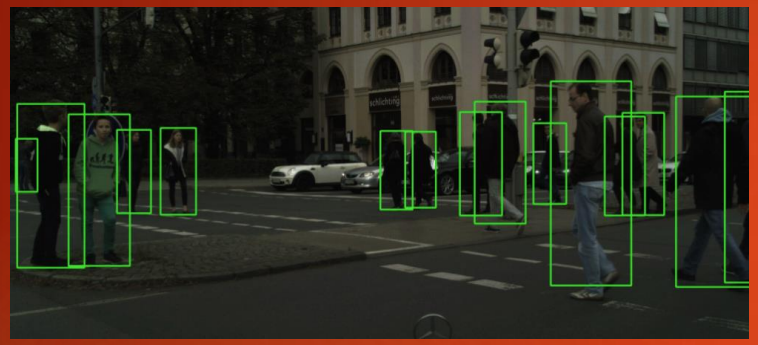
	Minimum Single IC Memory Capacity (Mbits)	# Mbits needed for one 4K frame	# IOs for x16 channel	# IOs for x32 lockstep channel	Minimum Memory Mbits (x16 channel)	Excess (wasted) Mbits) (one channel)	Minimum Memory Mbits (x32 channel)	Excess (wasted) Mbits (two channel)
RPC	256	136.8576	24	48	256	119.1424	512	238.2848
DDR3	1024	136.8576	51	73	1024	887.1424	2048	1774.2848

Miniaturized Module
ECP5 + 2 RPC DRAM + AF Camera



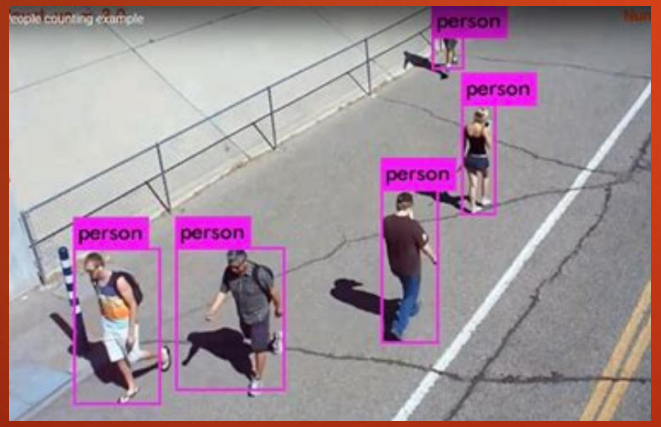


Example AI / Vision Applications ECP5 + Two RPC DRAMs



Social Distance Monitoring

Visible / Thermal image fusion

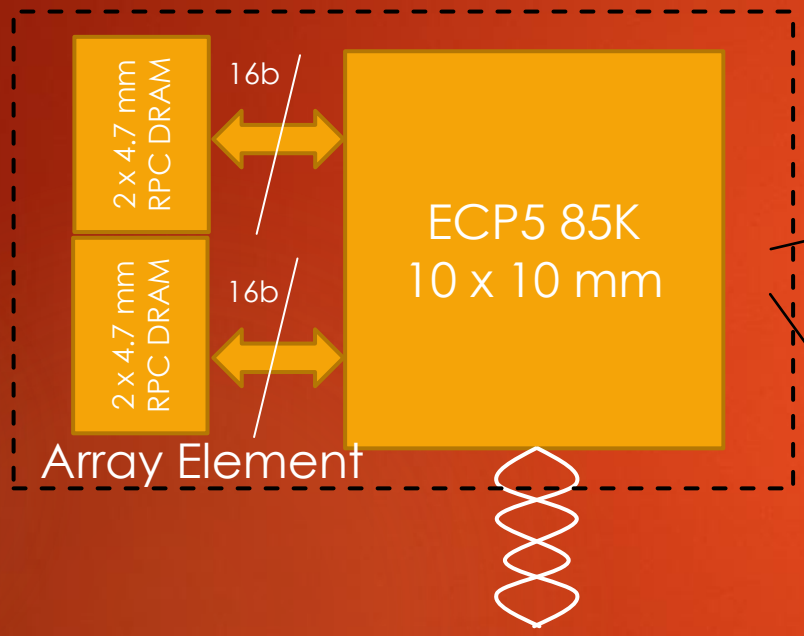


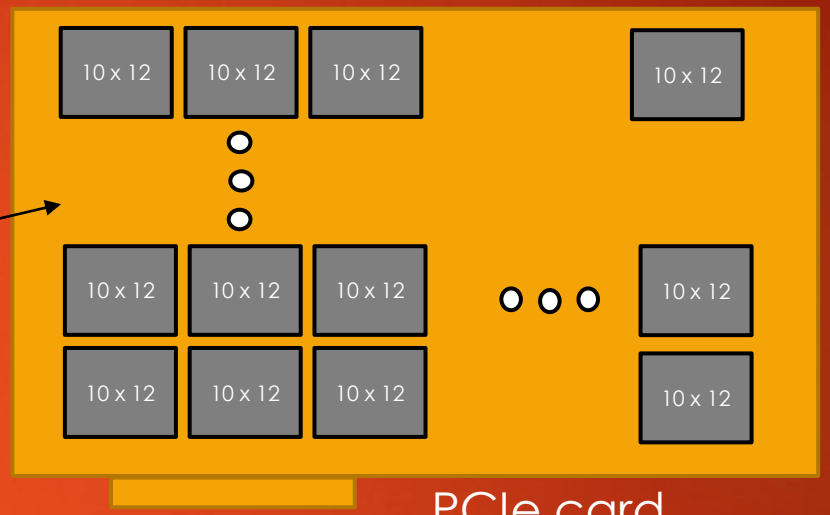
People Counting / Traffic analysis

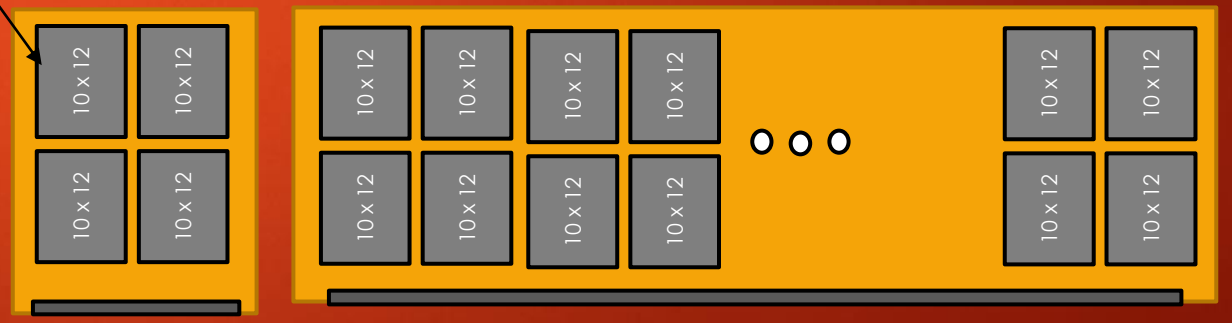
Face ID

Lens Distortion Correction / Rectification

AI/Search/Signal Processing Array Element
ECP5 + 2 RPC DRAM w / SERDES







22 x 30 mm
M.2 form factor

120 mm^2

10 x 12 mm

117 mm^2

DDR3
9 x 13 mm

Design Support We Offer

- RPC DRAM Data Sheet
- RPC DRAM Memory Controller
  - Compatible with Lattice Diamond Tools
  - Compatible with SensAI Neural Network Compiler
- Verilog Model of RPC DRAM
- Reference Design Documentation / examples
- Design support services (provided by Intermotion Technology Inc.)
- Embedded Vision Development Kit Board (after 3Q '20, contact sales)

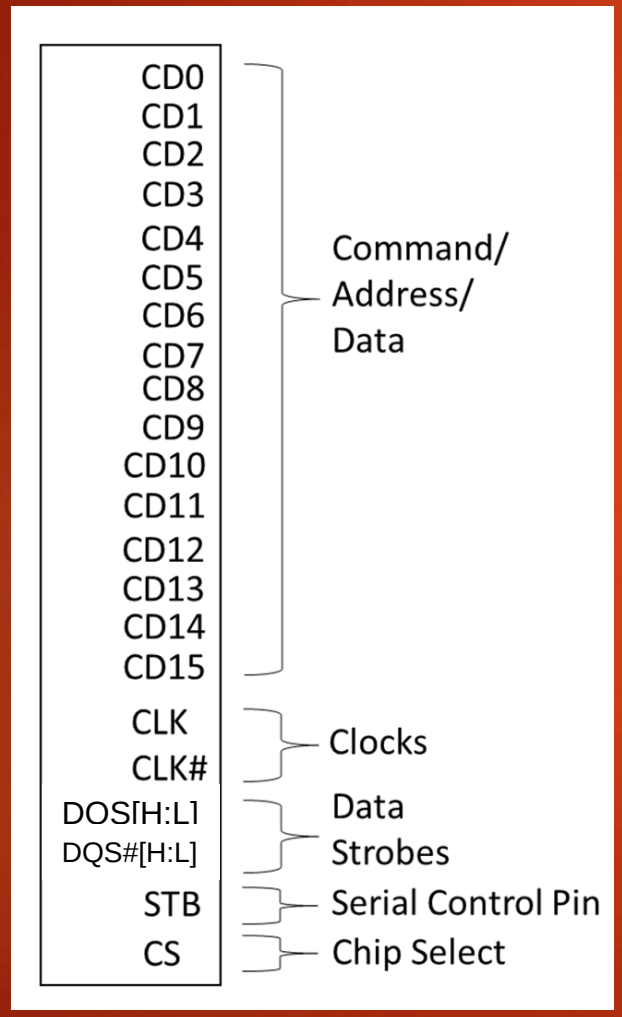
www.etronamerica.com

www.latticesemi.com

www.intermotiontech.com

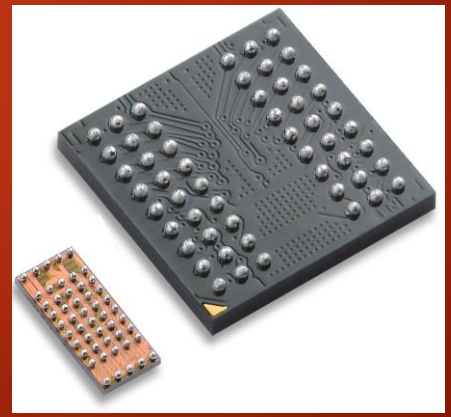
RPC DRAM Backgrounder

RPC DRAM®



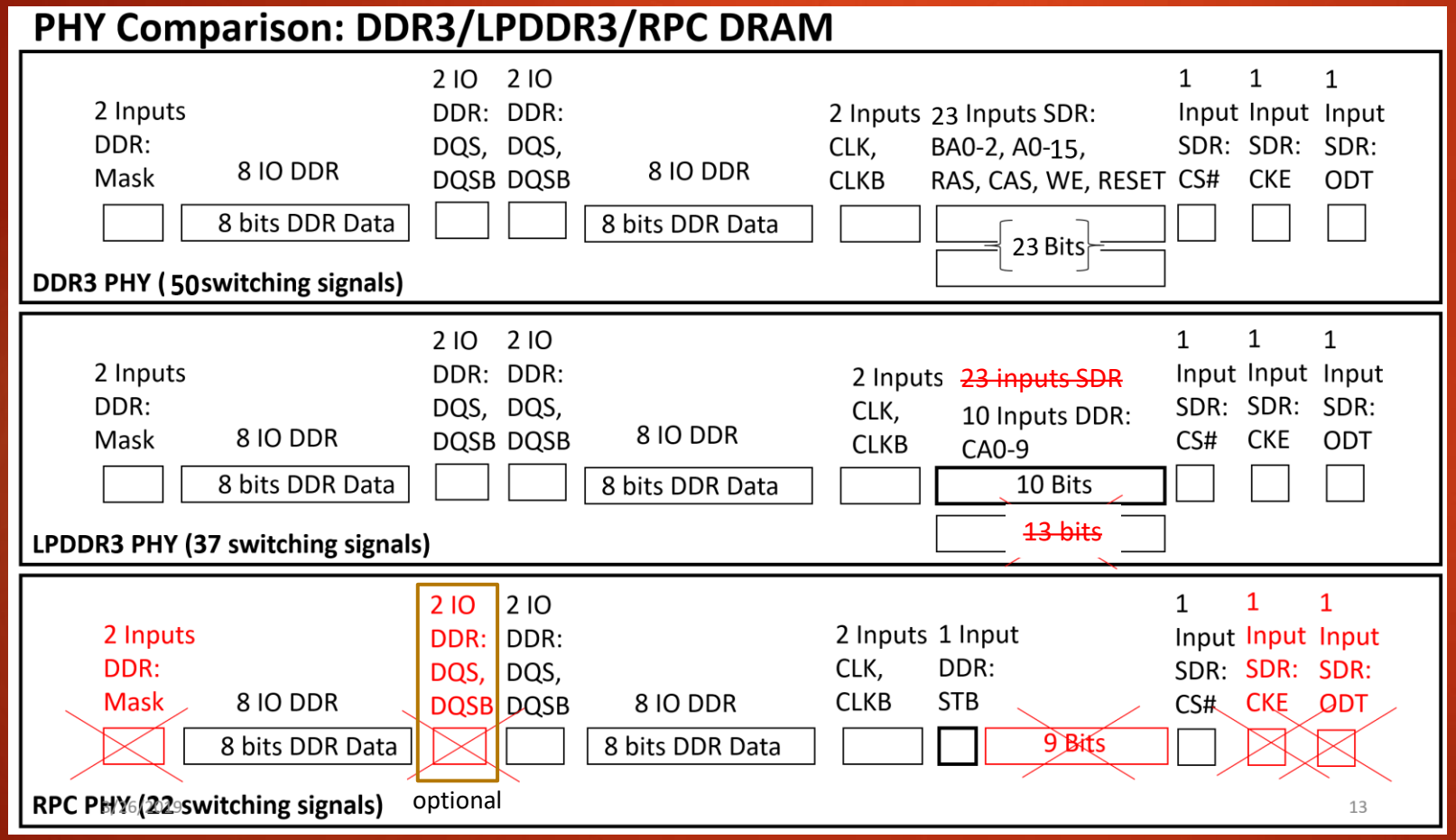
- 256 Mbits
- 4 banks of 64 Mbits
- X16 DDR type external interface
- Memory bus clock up to 1200 MHz (DDR2400)
- 22/24 IO pin interface
- Discrete Packaging
  - 54 BGA (8 x 8 mm)
  - 50 WLCSP (2 x 4.7 mm)
- Bare Die (2 x 4.7 mm KGD)
- Speeds up to DDR 2400
- 1.35 & 1.5V versions

54 BGA (8 x 8 mm)



50 WLCSP (2 x 4.7 mm)

Interface Signal Comparison DDR3, LPDDR3, RPC



DDR3/LPDDR3 vs RPC Architecturally Similar

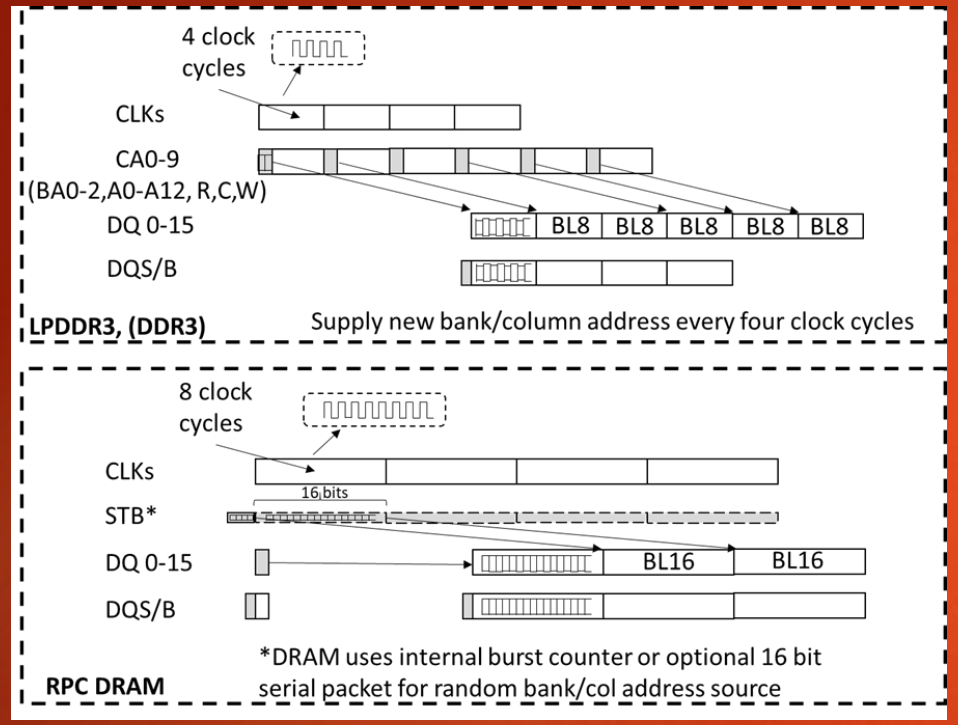


Table 65: Command Truth Table

Notes 1–13 apply to entire table

Command	Command Pins CKE CK(n-1)	CKE CK(n)	CS_n	CA Pins CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK Edge
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X								↓
REFRESH (per bank)	H	H	L	L	L	H	L	X							↑
			X	X										↓
REFRESH (all banks)	H	H	L	L	L	H	H	X							↑
			X	X										↓
Enter self refresh	H	L	L	L	L	H	X								↑
	X		X	X											↓
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2		↑
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14		↓
WRITE (bank)	H	H	L	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2			↑
			X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11		↓
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2		↑
			X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11		↓
PRECHARGE (per bank, all banks)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2		↑
			X	X											↓
ENTER DPD	H	L	L	H	H	L	X								↑
	X		X	X											↓
NOP	H	H	L	H	H	H	X								↑
			X	X											↓
MAINTAIN PD, SREF, DPD (NOP)	L	L	L	H	H	H	X								↑
			X	X											↓
NOP	H	H	H	X											↑
			X	X											↓

LPDDR3 receives Encoded Address/ Commands via double edged command/address bus sampling

LPDDR3 Command Truth Table

Table 6-1. Parallel Packet Command Truth Table

Command	CLK CK_{n-1}	CLK CK_n	CS#	DB Pins 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRS	↑		0		ODT				Zout			nWR			CL		0	1	0
	↓		0	TM	ODT PD	CSR FX	ODT STB				X								0
ACT	↑		0						X						BA1	BA0	1	0	1
	↓		0		X			RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
RD	↑		0	CA6	CA5	CA4		X			BC					BA1	BA0	0	0	0
	↓		0	CA9	CA8	CA7					X								0
WR	↑		0	CA6	CA5	CA4		X			BC					BA1	BA0	0	0	1
	↓		0	CA9	CA8	CA7					X								0
WL-2 (1st DM)	↑		0	DM1 O3	DM0 O3	DM1 E3	DM0 E3	DM1 O2	DM0 O2	DM1 E2	DM0 E2	DM1 O1	DM0 O1	DM1 E1	DM0 E1	DM1 O0	DM0 O0	DM1 E0	DM0 E0
	↓		0	DM1 O3	DM0 O3	DM1 E3	DM0 E3	DM1 O2	DM0 O2	DM1 E2	DM0 E2	DM1 O1	DM0 O1	DM1 E1	DM0 E1	DM1 O0	DM0 O0	DM1 E0	DM0 E0
WL-1 (last DM)	↑		0	DM1 O3	DM0 O3	DM1 E3	DM0 E3	DM1 O2	DM0 O2	DM1 E2	DM0 E2	DM1 O1	DM0 O1	DM1 E1	DM0 E1	DM1 O0	DM0 O0	DM1 E0	DM0 E0
	↓		0	DM1 O3	DM0 O3	DM1 E3	DM0 E3	DM1 O2	DM0 O2	DM1 E2	DM0 E2	DM1 O1	DM0 O1	DM1 E1	DM0 E1	DM1 O0	DM0 O0	DM1 E0	DM0 E0
PRE	↑		0		X					BK3	BK2	BK1	BK0		X		1	0	0
	↓		0							X									0
REF	↑		0		X					BK3	BK2	BK1	BK0		X		1	1	0
	↓		0							X							REF OP1	REF OP0	0
PD Entry	↑		0							X							0	1	0
	↓		0							X							0	0	1
PD Exit		↑	0							X									
		↓	1							X									
DPD Entry	↑		0							X							0	1	0
	↓		0							X							1	0	1
DPD Exit		↑	0							X									
		↓	1							X									
ZQ Calibration	↑		0	ZQC OP1	ZQC OP0					X							0	0	1
	↓		0							X									1
RESET	↑		0							X							0	0	0
	↓		0							X									1
UTR	↑		0					X						UTR OP1	UTR OP0	UTR EN	1	1	1
	↓		0							X									0

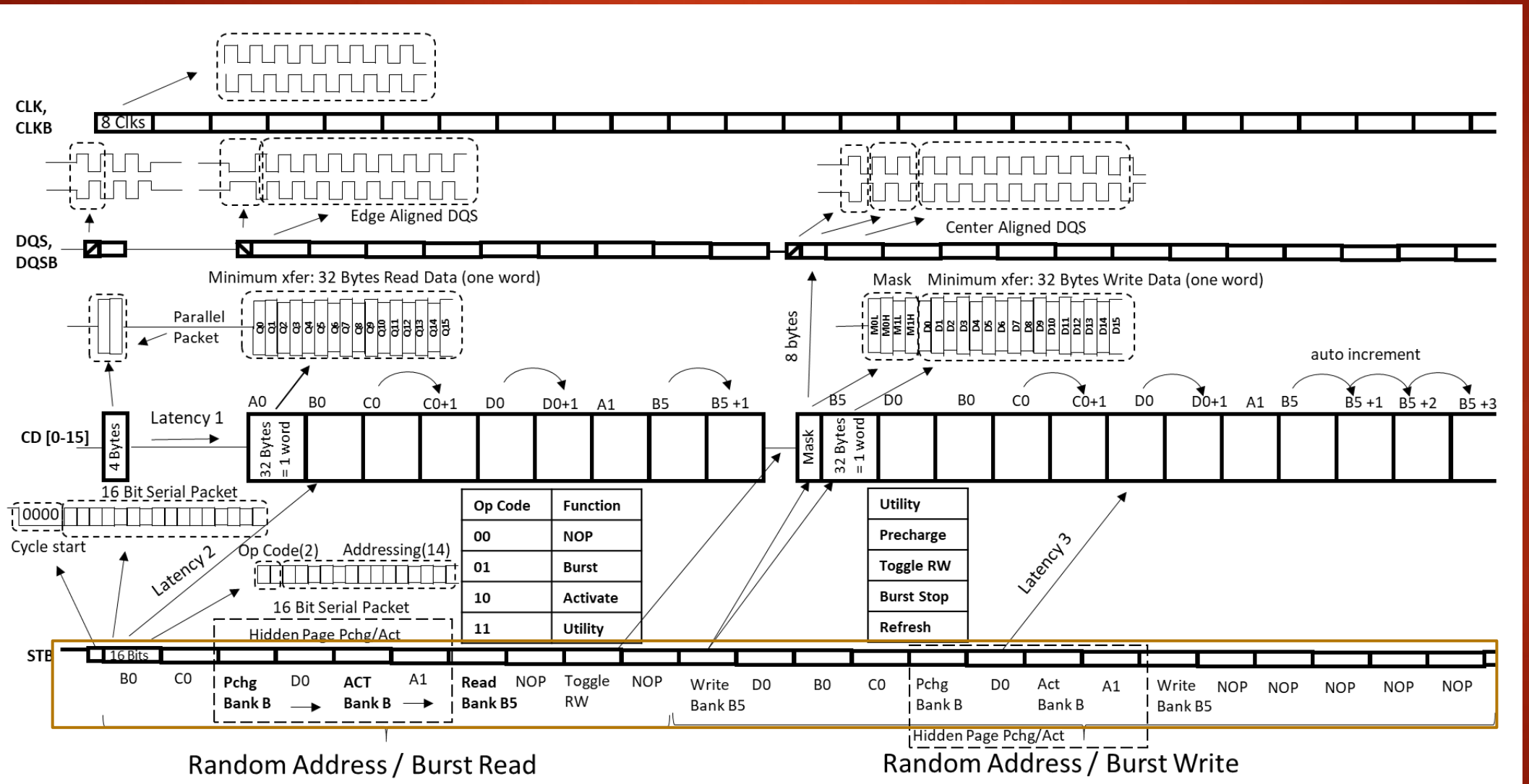
RPC DRAM receives Encoded Address/Commands via double edged command/address bus sampling

RPC DRAM Command Truth Table

DDR3, LPDDR3 & RPC DRAM Main Architectural Differences

Device	X16 DDR3 (256M)	X16 LPDDR3 (256M)	X16 RPC DRAM (256M)
Banks	4	4	4
Arch. Prefetch	128 bits	128 bits	256 bits
Burst Cycle Addressing	New address every 4 clocks	New address every 4 clocks	Internal burst counter -or- Optional new col/bank address every 8 clocks
PHY Signals	51	37	22/24
CA Ports	1: SDR, Separate from Data	1: DDR, Separate from Data	2: DDR, parallel packet port is multiplexed with Data & Serial packet port (STB pin) is separate from Data

RPC Serial Control Protocol

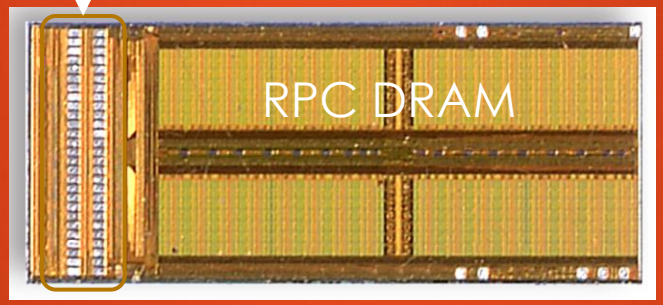


Serial Commands

Alternative Packaging

Bare Die for MCPs

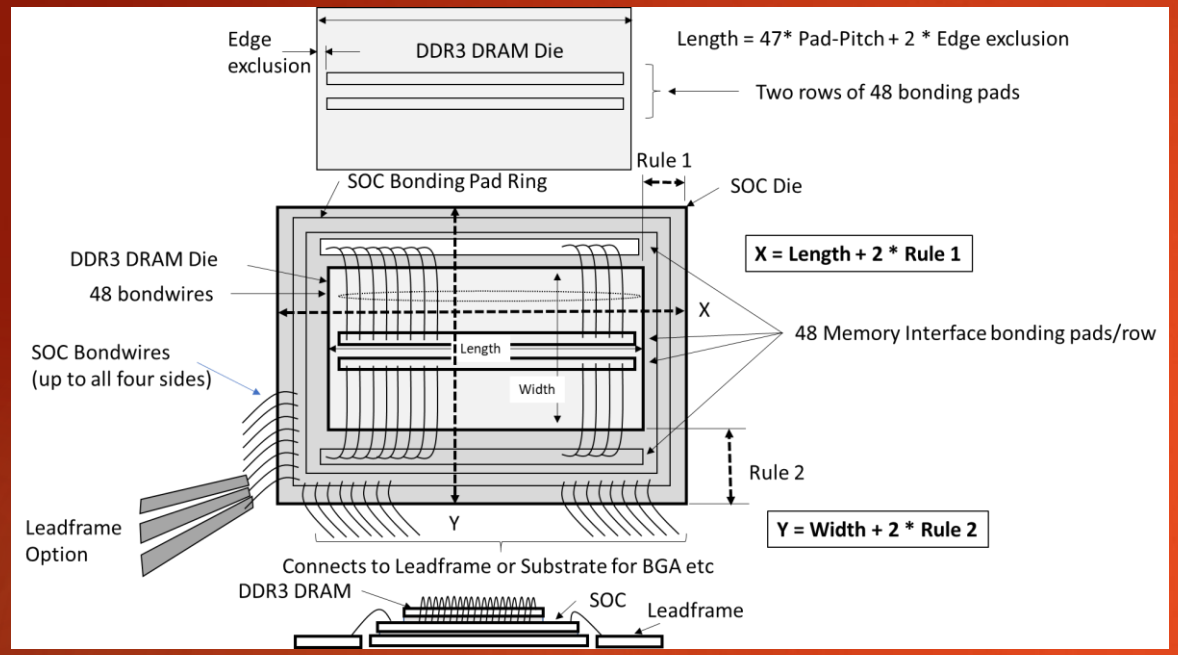
Bonding Pads
(one end only)



4.63 x 1.96 mm

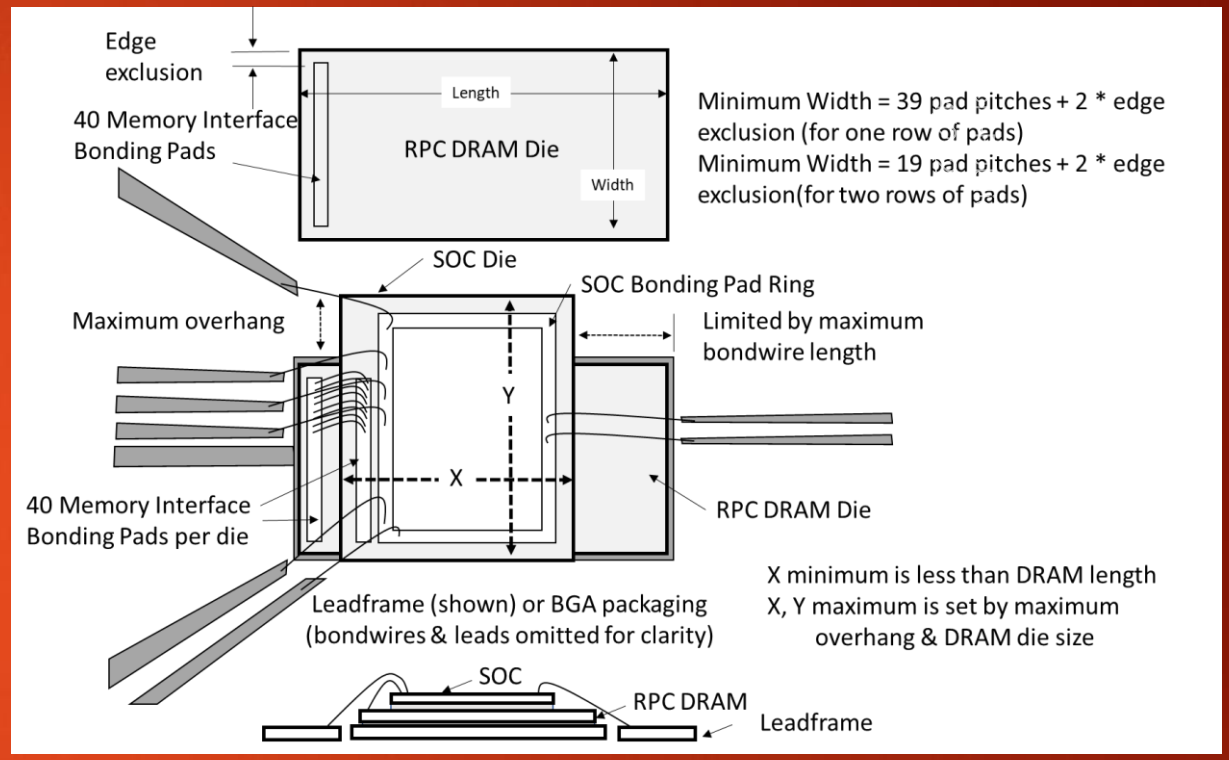
Stacked Die Assembly for MCP w/DRAM

DDR3



DRAM LIMITED

RPC DRAM



SOC is core or pad LIMITED

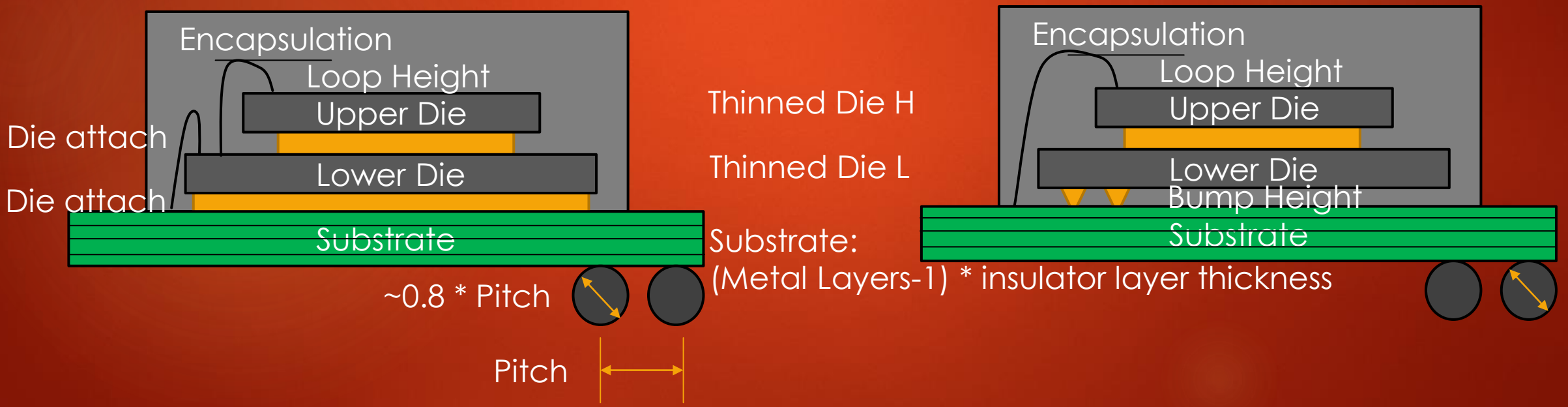
MCP with Stacked die using DDR3 DRAM on top: *DRAM establishes minimum SOC die size*

MCP with Stacked die using SOC on top of stairstep stack with *RPC DRAM allows for much smaller SOC die mechanical size*

Assembly Rules Impact on SOC Die Size

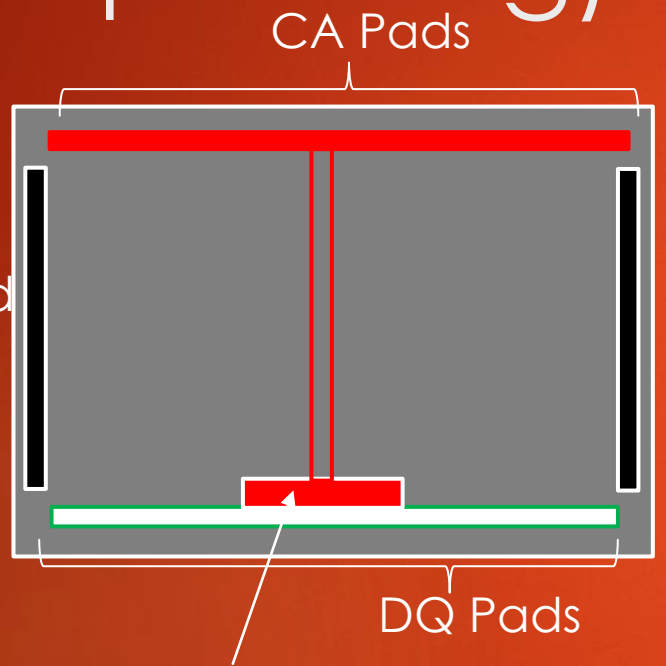
Wirebonded MCP Cross Section Design Rules

All Dimensions are in Microns											
	Pitch	Ball Size (0.8 * ball pitch)	Substrate Metal Layer Count	Thickness: substrate insulator layer	Lower Die attach Thickness or FC Bump Height	Lower Die Thickness	Upper Die Attach Thickness	Upper Die Thickness	Wire Loop Height	Encapsulation	Package Thickness (board to top)
Wirebond	400	320	4	50	35	100	35	100	150	50	940
FC	400	320	4	50	75	100	35	100	150	50	980



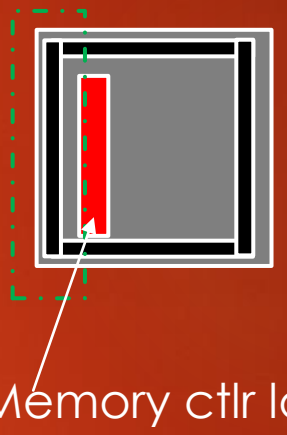
RPC Value Proposition (ASIC Floorplanning)

ASIC
Wirebonded
Stacked
DDR3
Assy



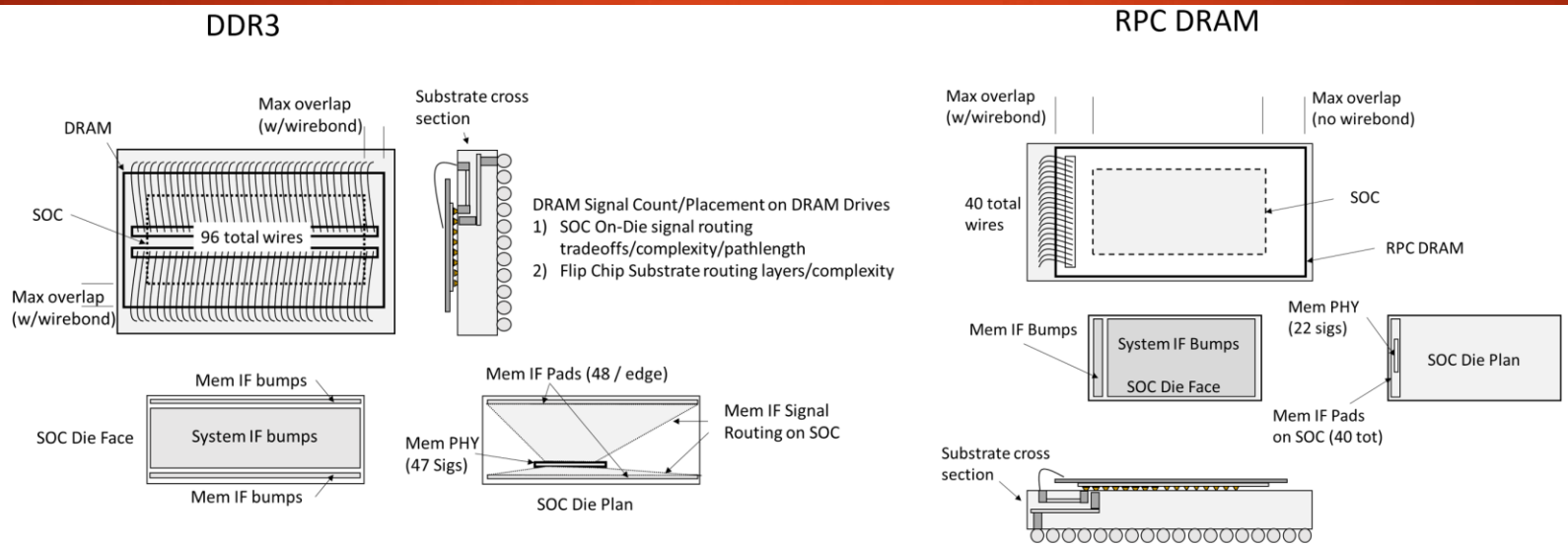
Must route many signals across chip or route through substrate
(address/control and data must bond to opposite sides of the ASIC, but all come from memory controller

ASIC
Wirebonded
Stacked
RPC
Assy



Mem I/F pads adjacent to Mem Ctlr Logic
(everything remains together on the die)

Flip Chip ASIC/SOC with Stacked Die Memory

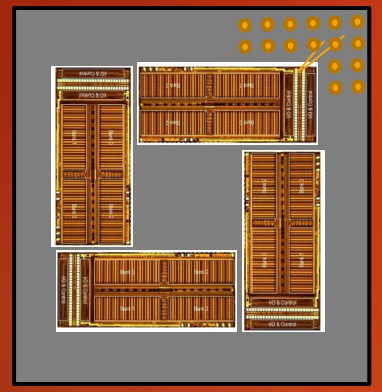


Possible to use Face Up Wirebonded structure with RPC DRAM and avoid Flip Chip technology to get small SOC die size

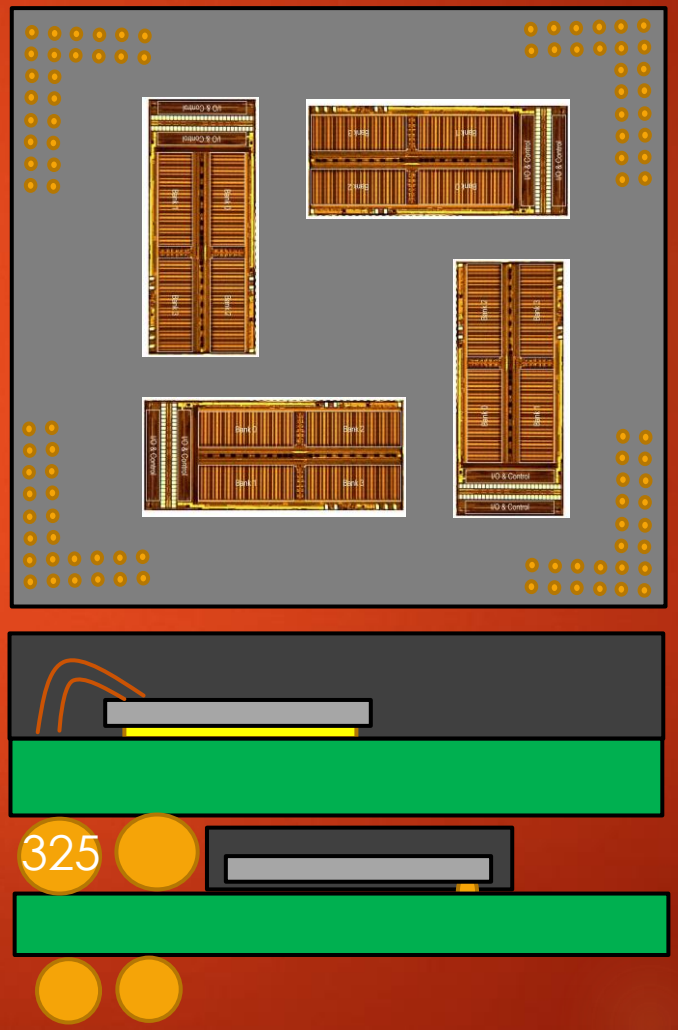
Memory	#Switching Signals	#SOC PHY Pads	Longest Mem IF Path Length
DDR3 (x16)	47	96	DRAM_Width + 0.5 * SOC_Width
RPC (X16)	22	40	2* Max_overhang

168 ball POP/standalone Memory x64, 1Gbit, 19.2 GBytes/sec

23 ball x 23 ball array, 500 micron pitch



12 x 12 mm



0.325 ball,
0.500 pitch