
2Gb: x32 LPDDR4/4X Synchronous DRAM (SDRAM)

Product Preview (Rev. 1.0, Aug. /2026)

Features

- JEDEC Standard Compliant
- Low-voltage Core and I/O Power Supplies:
 - VDD1 = 1.8V (1.7V~1.95V)
 - VDD2 = 1.1V (1.06V~1.17V)
 - VDDQ = 1.1V (1.06V~1.17V)_LPDDR4
 - VDDQ = 0.6V (0.57V~0.65V)_LPDDR4X
- Configuration: 64 Meg x 32 (2 channels x16 I/O)
- Clock rate: up to 1866 MHz
- Data rate: up to 3733 Mbps
- Operating temperature:
 - Commercial: T_C = -25~85°C
 - Industrial: T_C = -40~95°C
- Supports JEDEC clock jitter specification
- Dynamic ODT:
 - DQ ODT: VSSQ Termination
 - CA ODT: VSS Termination
- Interface: LVSTL
- Internal VREF and VREF Training
- ZQ Calibration
- 8 internal banks per each channel
- 16n-bit prefetch architecture
- Single data rate (multiple cycles) CMD/ADR bus
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies
- Programmable and on-the-fly burst lengths
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Selectable output drive strength (DS)
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- ZQ Calibration
- RoHS compliant
- Packaging options: Pb Free and Halogen Free
 - 200-ball 10 x 15 x 1.1mm (max) FBGA Package

Table 1. Speed Grade Information

Clock Frequency (MHz)	Data Rate (Mbps/pin)	Write Latency		Read Latency	
		Set A	Set B	DBI Disabled	DBI Enabled
1866	3733	16	30	32	36
1600	3200	14	26	28	32

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Table 2. Addressing

Memory Density		64M x 32
Number of Channels		1
Number of Ranks		1
Density per channel		1Gb
Density per package		2Gb
Configuration		8Mb x 16DQ x 8 banks x 2 channel
Number of Banks (per Channel)		8
Array Pre-Fetch (Bits, per channel)		256
Number of Rows (per channel)		8,192
Number of Columns (fetch boundaries)		64
Page Size (Bytes)		2048
Bank Address		BA0-BA2
x16	Row Addresses	R0-R12
	Column Addresses	C0-C9
Burst Starting Address Boundary		64-bit

Table 3. Ordering Information

Commercial Grade				
Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6LD32MBAPA-53H	1866MHz	3733Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 1.1V	FBGA
EM6LD32MBAPA-62H	1600MHz	3200Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 1.1V	FBGA
EM6PD32MBAPA-53H	1866MHz	3733Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 0.6V	FBGA
EM6PD32MBAPA-62H	1600MHz	3200Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 0.6V	FBGA
Industrial Grade				
Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6LD32MBAPA-53IH	1866MHz	3733Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 1.1V	FBGA
EM6LD32MBAPA-62IH	1600MHz	3200Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 1.1V	FBGA
EM6PD32MBAPA-53IH	1866MHz	3733Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 0.6V	FBGA
EM6PD32MBAPA-62IH	1600MHz	3200Mbps/pin	V _{DD1} 1.8V, V _{DD2} 1.1V, V _{DDQ} 0.6V	FBGA

BAP: indicates 10 x 15 x 1.1mm FBGA package

A (Last digit): indicates Generation Code

I: indicates Industrial Grade

H: indicates Pb and Halogen Free

Ball Assignment

	1	2	3	4	5	...	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ		NC	VDD2	VSS	NC	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ		VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS		VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_A	VSS	VDDQ		VDDQ	VSS	DQS1_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0#_A	DQ5_A	VSS		VSS	DQ13_A	DQS1#_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2		VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS		VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	NC	CS_A	VDD2		VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE_A	NC		CK_A	CK#_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
L											
M											
N	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE_B	NC		CK_B	CK#_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	NC	CS_B	VDD2		VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS		VSS	VDD1	VSS	RESET#	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2		VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0#_B	DQ5_B	VSS		VSS	DQ13_B	DQS1#_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_B	VSS	VDDQ		VDDQ	VSS	DQS1_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS		VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ		VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS		VSS	VDD2	VSS	NC	NC

Figure 1. 200-Ball (FBGA Top View)

Package Block Diagram

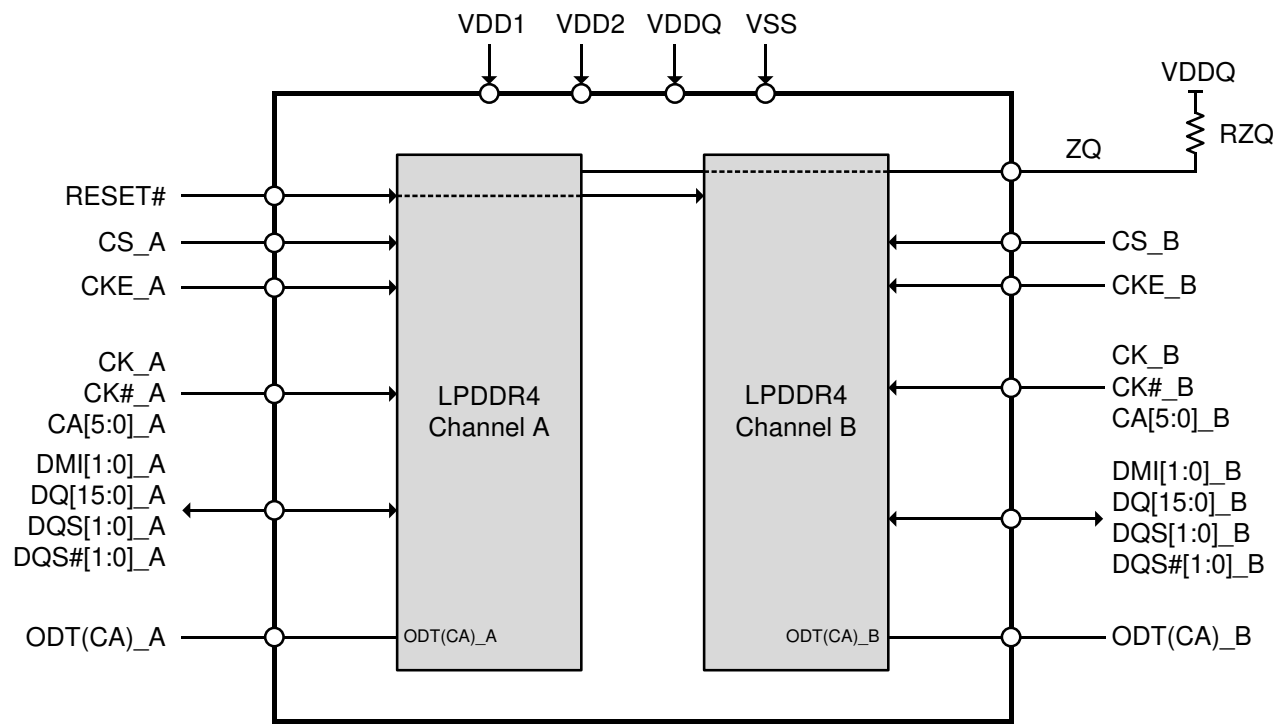


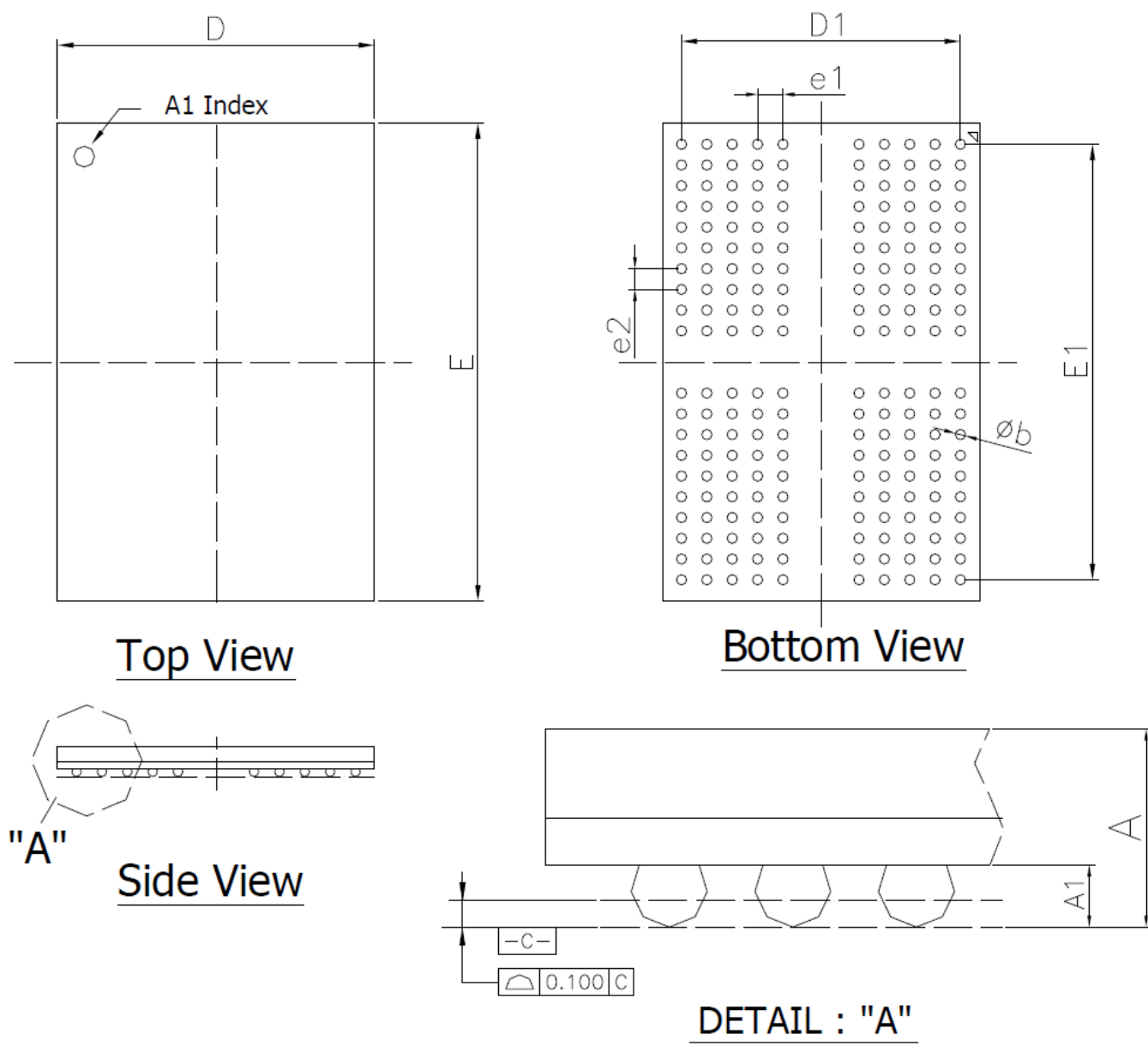
Figure 2. Dual Channel Package Block Diagram (x32)

Functional Description

The LPDDR4/4X SDRAM is organized as 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

This LPDDR4/4X device uses a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. More detailed information can be found in JESD209-4E and JESD209-4-1B.

Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.0433	--	--	1.10
A1	0.0085	0.0104	0.0124	0.215	0.265	0.315
D	0.3898	0.3937	0.3976	9.90	10.00	10.10
E	0.5866	0.5906	0.5945	14.90	15.00	15.10
D1	--	0.3465	--	--	8.80	--
E1	--	0.5374	--	--	13.65	--
e1	--	0.0315	--	--	0.80	--
e2	--	0.0256	--	--	0.65	--
b	0.0118	0.0138	0.0157	0.30	0.35	0.40

Figure 3. 200-Ball FBGA Package 10x15x1.1mm(max)