1Gb: x16 LPDDR4/4X Synchronous DRAM (SDRAM)

Product Preview (Rev. 1.0, Jun. /2026)

Features

- JEDEC Standard Compliant
- Low-voltage Core and I/O Power Supplies:
  - VDD1 = 1.8V (1.7V~1.95V)
  - VDD2 = 1.1V (1.06V~1.17V)
  - VDDQ = 1.1V (1.06V~1.17V)_LPDDR4
  - VDDQ = 0.6V (0.57V~0.65V)_LPDDR4X
- Configuration: 64 Meg x 16 (1 channels x16 I/O)
- Clock rate: up to 2133 MHz
- Data rate: up to 4266 Mbps
- Operating temperature:
  - Commercial: T_C = -25~85°C
  - Industrial: T_C = -40~95°C
- Supports JEDEC clock jitter specification
- Dynamic ODT:
  - DQ ODT: VSSQ Termination
  - CA ODT: VSS Termination
- Interface: LVSTL
- Internal VREF and VREF Training
- ZQ Calibration
- 8 internal banks per each channel
- 16n-bit prefetch architecture
- Single data rate (multiple cycles) CMD/ADR bus
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies
- Programmable and on-the-fly burst lengths
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Selectable output drive strength (DS)
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- ZQ Calibration
- RoHS compliant
- Packaging options: Pb Free and Halogen Free
  - 200-ball 10 x 15 x 1.1mm (max) FBGA Package
  - Known Good Die

Table 1. Speed Grade Information

Clock Frequency (MHz)	Data Rate (Mbps/pin)	Write Latency		Read Latency	
		Set A	Set B	DBI Disabled	DBI Enabled
2133	4266	18	34	36	40
1866	3733	16	30	32	36
1600	3200	14	26	28	32

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Table 2. Addressing

Memory Density		64M x 16
Organization		x16
Number of Channels		1
Number of Ranks		1
Density per channel		1Gb
Configuration		8Mb x 16DQ x 8 banks x 1 channel
Number of Banks (per Channel)		8
Array Pre-Fetch (Bits, per channel)		256
Number of Rows (per channel)		8,192
Number of Columns (fetch boundaries)		64
Page Size (Bytes)		2048
Bank Address		BA0-BA2
x16	Row Addresses	R0-R12
	Column Addresses	C0-C9
Burst Starting Address Boundary		64-bit

Table 3. Ordering Information

Commercial Grade				
Part Number	**Clock Frequency**	**Data Rate**	**Power Supply**	**Package**
EM6LC16MBAPA-46H	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6LC16MBAPA-53H	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6LC16MBAPA-62H	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6PC16MBAPA-46H	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PC16MBAPA-53H	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PC16MBAPA-62H	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6LC16MGDA-46/46R	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6LC16MGDA-53/53R	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6LC16MGDA-62/62R	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6PC16MGDA-46/46R	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD
EM6PC16MGDA-53/53R	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD
EM6PC16MGDA-62/62R	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD
Industrial Grade				
Part Number	**Clock Frequency**	**Data Rate**	**Power Supply**	**Package**
EM6LC16MBAPA-46IH	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6LC16MBAPA-53IH	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6LC16MBAPA-62IH	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	FBGA
EM6PC16MBAPA-46IH	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PC16MBAPA-53IH	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PC16MBAPA-62IH	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6LC16MGDA-46I/46IR	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6LC16MGDA-53I/53IR	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6LC16MGDA-62I/62IR	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 1.1V	KGD
EM6PC16MGDA-46I/46IR	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD
EM6PC16MGDA-53I/53IR	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD
EM6PC16MGDA-62I/62IR	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	KGD

BAP: indicates 10 x 15 x 1.1mm FBGA package
GD: indicates Known Good Die
A (Last digit): indicates Generation Code
I: indicates Industrial Grade
H: indicates Pb and Halogen Free
R: indicates RDL Project

Ball Assignment

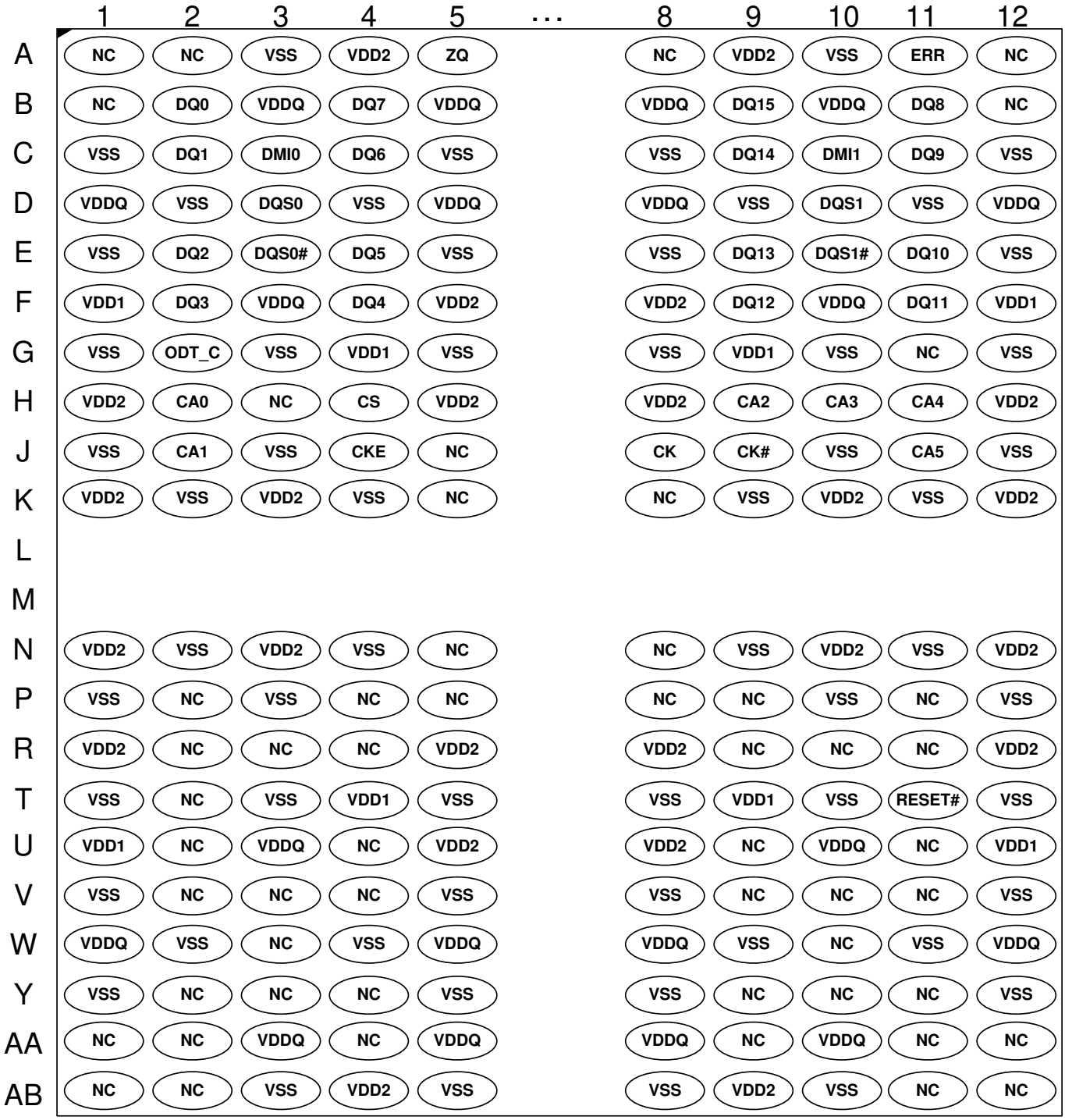


Figure 1. 200-Ball (FBGA Top View)

Package Block Diagram

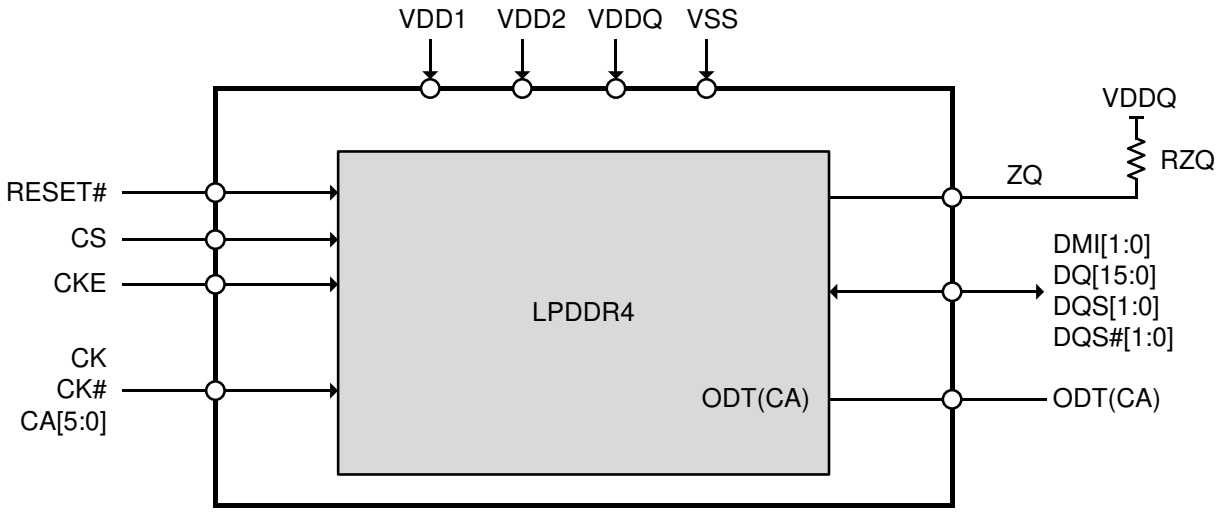


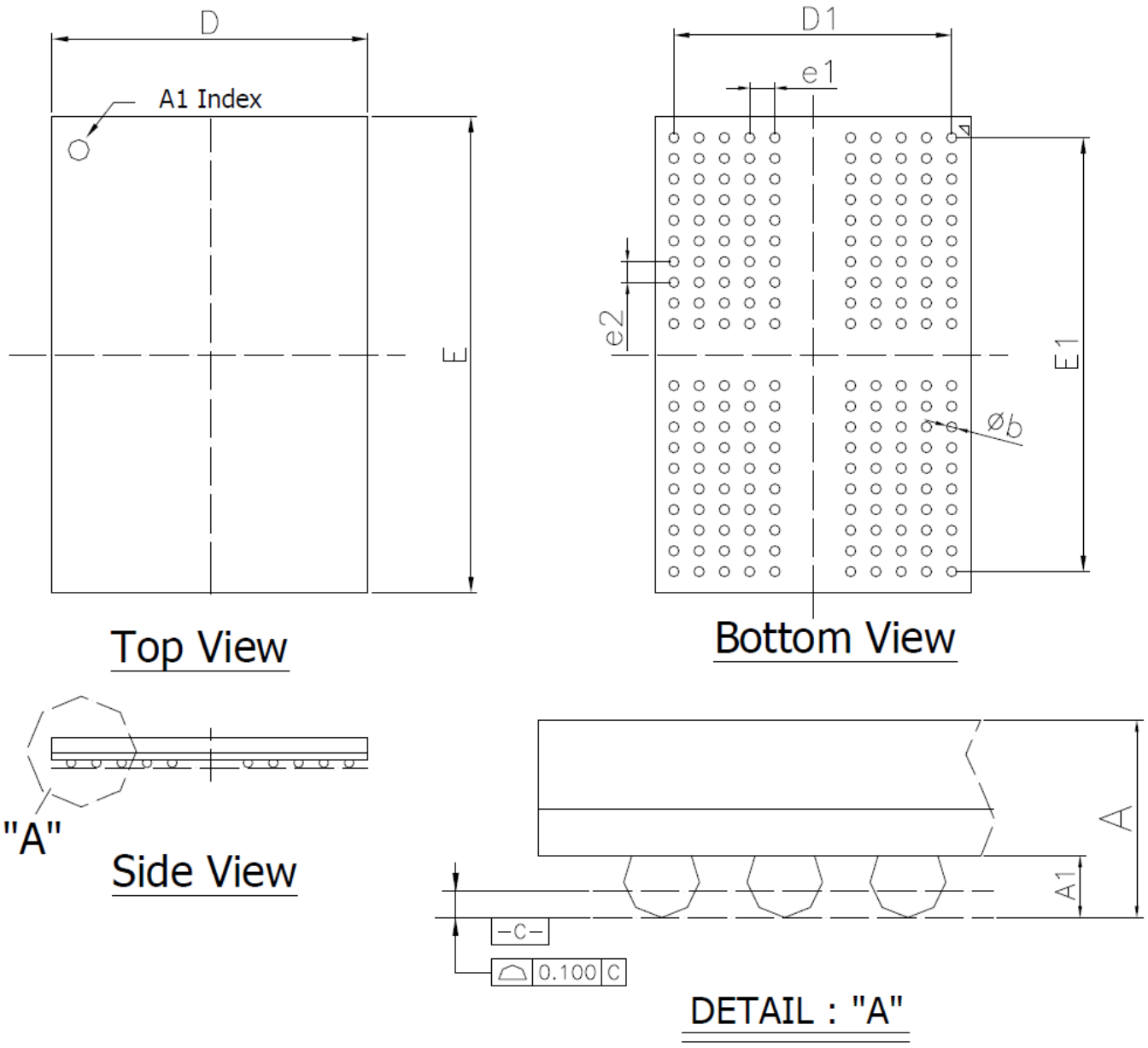
Figure 2. Single Channel Package Block Diagram (x16)

Functional Description

The LPDDR4/4X SDRAM is organized with one channel per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

This LPDDR4/4X device uses a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. More detailed information can be found in JESD209-4E and JESD209-4-1B.

Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.0433	--	--	1.10
A1	0.0085	0.0104	0.0124	0.215	0.265	0.315
D	0.3898	0.3937	0.3976	9.90	10.00	10.10
E	0.5866	0.5906	0.5945	14.90	15.00	15.10
D1	--	0.3465	--	--	8.80	--
E1	--	0.5374	--	--	13.65	--
e1	--	0.0315	--	--	0.80	--
e2	--	0.0256	--	--	0.65	--
b	0.0118	0.0138	0.0157	0.30	0.35	0.40

Figure 3. 200-Ball FBGA Package 10x15x1.1mm(max)