
4Gb: x8, x16 DDR4 Synchronous DRAM (SDRAM)

Product Preview (Rev. 1.0, Sep. /2026)

Features

- JEDEC Standard Compliant
- AEC-Q100 Compliant
- Configuration: 256Mx16, 512Mx8
- Fast clock rate:
 - 1600MHz @ CL = 22 (DDR4-3200)
 - 1333MHz @ CL = 19 (DDR4-2666)
 - 1200MHz @ CL = 17 (DDR4-2400)
- Power supplies:
 - V_{DD} & $V_{DDQ} = +1.2V \pm 0.06V$
 - $V_{PP} = +2.5V - 0.125V / +0.25V$
- Operating temperature:
 - Commercial: $T_C = 0 \sim 95^{\circ}C$
 - Industrial: $T_C = -40 \sim 95^{\circ}C$
 - Automotive A3: $T_C = -40 \sim 95^{\circ}C$
 - Automotive A2: $T_C = -40 \sim 105^{\circ}C$
- Supports JEDEC clock jitter specification
- Bidirectional differential data strobe, DQS & DQS#
- Differential Clock, CK & CK#
- 8 internal banks (x16): 2 groups of 4 banks each
- 16 internal banks (x8): 4 groups of 4 banks each
- Separated IO gating structures by Bank Group
- 8n-bit prefetch architecture
- Precharge & Active power down
- Auto Refresh and Self Refresh
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Self Refresh Abort
- Fine Granularity Refresh
- Dynamic ODT (R_{TT_PARK} & R_{TT_Nom} & R_{TT_WR})
- Package: Pb Free and Halogen Free
 - 96-ball 7.5 x 13 x 1.0mm FBGA for x16
 - 78-ball 7.5 x 10.6 x 1.0mm FBGA for x8
- Write Leveling
- DQ Training via MPR
- Programmable preamble is supported both of $1t_{CK}$ and $2t_{CK}$ mode
- Command/Address (CA) Parity
- Data bus write cyclic redundancy check (CRC)
- Boundary Scan Mode
- Internal V_{REFDQ} Training
- Read Preamble Training
- Control Gear Down Mode
- Per DRAM Addressability (PDA)
- Output Driver Impedance Control
- Dynamic on-die termination (ODT)
- Input Data Mask (DM) and Data Bus Inversion (DBI)
- ZQ Calibration
- Command/Address latency (CAL)
- Maximum Power Saving Mode (MPSM)
- Asynchronous Reset
- DLL enable/disable
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Burst type: Sequential / Interleave
- CAS Latency (CL)
- CAS Write Latency (CWL)
- Additive Latency (AL): 0, CL-1, CL-2
- Average refresh period
 - 8192 cycles per 64ms (7.8us for $T_C \leq 85^{\circ}C$)
 - 8192 cycles per 32ms (3.9us for $85^{\circ}C < T_C \leq 95^{\circ}C$)
 - 8192 cycles per 16ms (1.95us for $95^{\circ}C < T_C \leq 105^{\circ}C$)
- Data Interface: Pseudo Open Drain (POD)
- RoHS compliant
- Hard post package repair (hPPR)
- Soft post package repair (sPPR)

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Table 1. Ordering Information

Commercial Grade				
Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6OE16NWBC-08H	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-07H	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-62H	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE08NW9C-08H	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-07H	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-62H	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
Industrial Grade				
EM6OE16NWBC-08IH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-07IH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-62IH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE08NW9C-08IH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-07IH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-62IH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
Automotive Grade 3				
EM6OE16NWBC-08AH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-07AH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-62AH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE08NW9C-08AH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-07AH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-62AH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
Automotive Grade 2				
EM6OE16NWBC-08BH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-07BH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE16NWBC-62BH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	96-ball FBGA
EM6OE08NW9C-08BH	1200MHz	2400Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-07BH	1333MHz	2666Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA
EM6OE08NW9C-62BH	1600MHz	3200Mbps/pin	V _{DD} /V _{DDQ} 1.2V, V _{PP} 2.5V	78-ball FBGA

WB: indicates 7.5 x 13 x 1.0mm FBGA Package for x16

W9: indicates 7.5 x 10.6 x 1.0mm FBGA Package for x8

C: indicates Generation Code

I: indicates Industrial Grade

A: indicates Automotive Grade 3

B: indicates Automotive Grade 2

H: indicates Pb and Halogen Free

Basic Functionality

DDR4 SDRAM is a high-speed dynamic random-access memory device. It is internally organized as 8 banks (2 bank groups × 4 banks) in the x16 configuration and 16 banks (4 bank groups × 4 banks) in the x8 configuration. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Activate Command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate Command are used to select the bank and row to be activated (BG0-BG1 in x8 and BG0 in x16 select the bank group; BA0-BA1 select the bank; A0-A14 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation. For more details, refer to the JEDEC Standard Specification JESD79-4D.

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	t _{RCD} (ns)	t _{RP} (ns)
DDR4-2400	1200MHz	17	14.16	14.16
DDR4-2666	1333MHz	19	14.25	14.25
DDR4-3200	1600MHz	22	13.75	13.75

Table 3. Addressing

Parameter	256M x16	512M x8
Row Addressing	A0-A14	A0-A14
Column Addressing	A0-A9	A0-A9
Bank Addressing	BA0-BA1	BA0-BA1
Bank Groups	BG0	BG0-BG1
Page size	2KB	1KB

Ball Assignment

	1	2	3	...	7	8	9
A	VDDQ	VSSQ	DQ8		UDQS#	VSSQ	VDDQ
B	VPP	VSS	VDD		UDQS	DQ9	VDD
C	VDDQ	DQ12	DQ10		DQ11	DQ13	VSSQ
D	VDD	VSSQ	DQ14		DQ15	VSSQ	VDDQ
E	VSS	UDM#/ UDBI#	VSSQ		LDM#/ LDBI#	VSSQ	VSS
F	VSSQ	VDDQ	LDQS#		DQ1	VDDQ	ZQ
G	VDDQ	DQ0	LDQS		VDD	VSS	VDDQ
H	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ
J	VDD	VDDQ	DQ6		DQ7	VDDQ	VDD
K	VSS	CKE	ODT		CK	CK#	VSS
L	VDD	WE#/ A14	ACT#		CS#	RAS#/ A16	VDD
M	VREFCA	BG0	A10/AP		A12/ BC#	CAS#/ A15	VSS
N	VSS	BA0	A4		A3	BA1	TEN
P	Reset#	A6	A0		A1	A5	Alert#
R	VDD	A8	A2		A9	A7	VPP
T	VSS	A11	PAR		NC	A13	VDD

Figure 1. 96-Ball (FBGA Top View) for x16

	1	2	3	...	7	8	9
A	VDD	VSSQ	TDQS#		DM#/DBI# /TDQS	VSSQ	VSS
B	VPP	VDDQ	DQS#		DQ1	VDDQ	ZQ
C	VDDQ	DQ0	DQS		VDD	VSS	VDDQ
D	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ
E	VSS	VDDQ	DQ6		DQ7	VDDQ	VSS
F	VDD	NC	ODT		CK	CK#	VDD
G	VSS	NC	CKE		CS#	NC	NC
H	VDD	WE#/A14	ACT#		CAS#/ A15	RAS#/ A16	VSS
J	VREFCA	BG0	A10/AP		A12/BC#	BG1	VDD
K	VSS	BA0	A4		A3	BA1	VSS
L	Reset#	A6	A0		A1	A5	Alert#
M	VDD	A8	A2		A9	A7	VPP
N	VSS	A11	PAR		NC	A13	VDD

Figure 2. 78-Ball (FBGA Top View) for x8

Functional Block Diagram

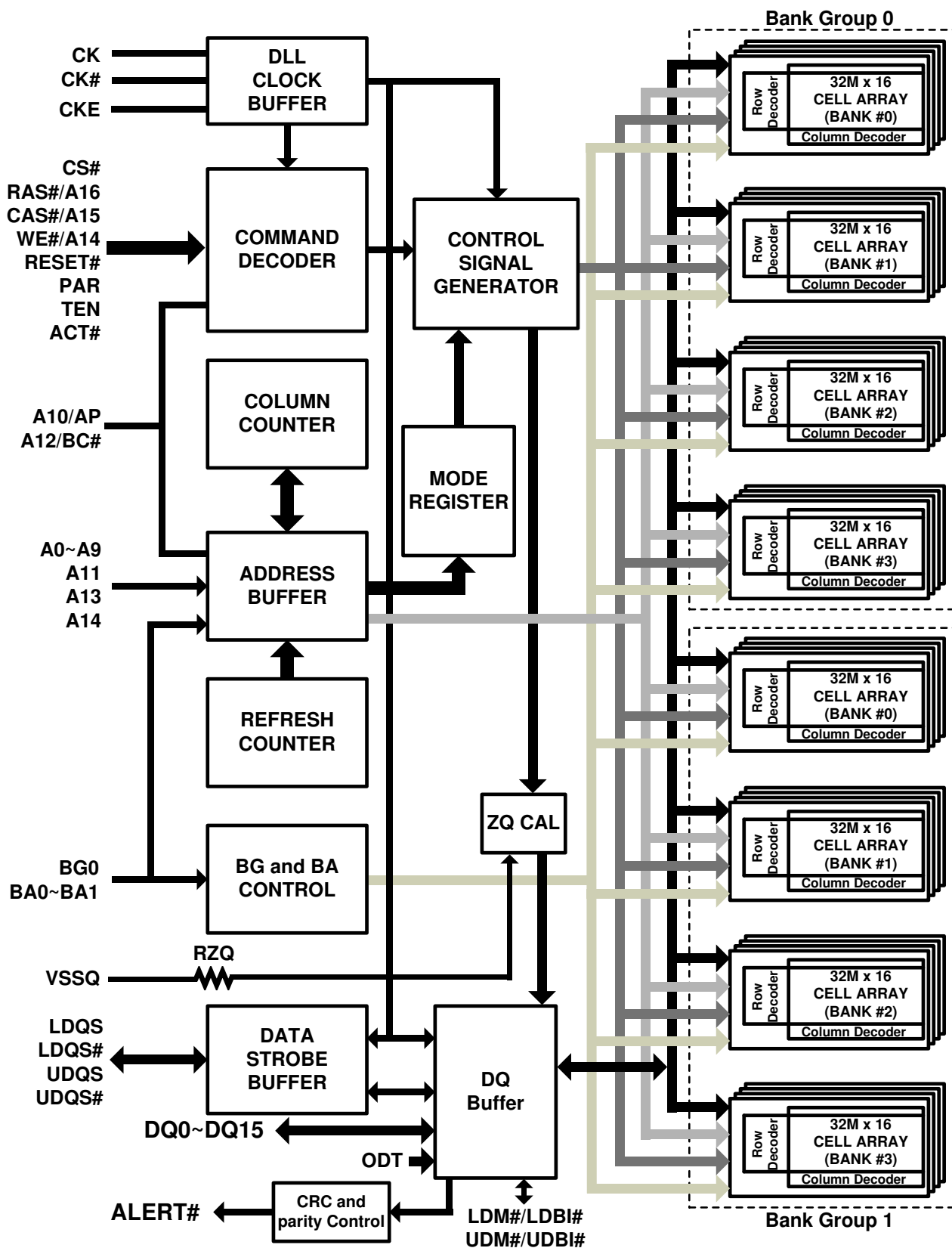


Figure 3. Block Diagram (x16)

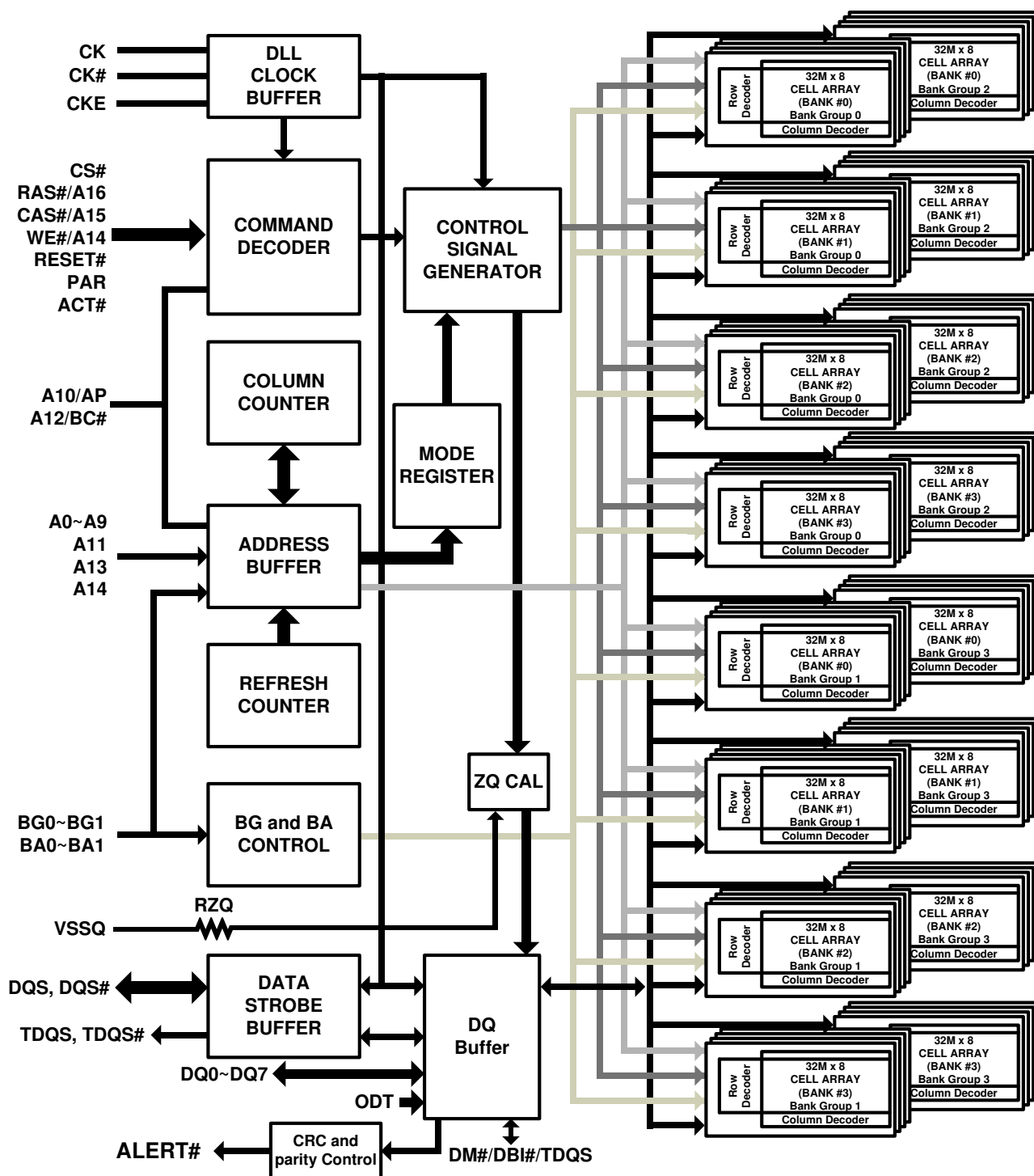
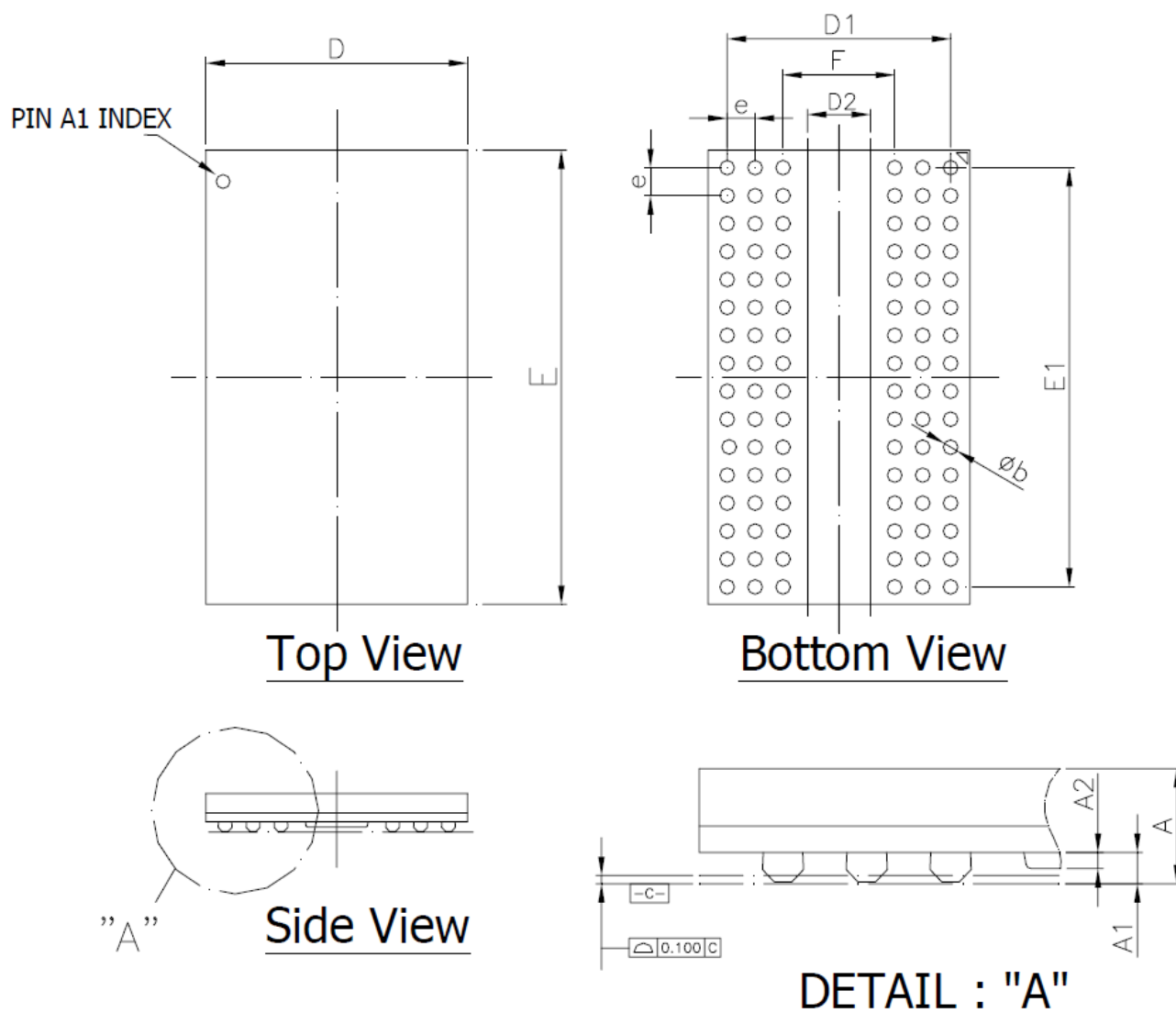


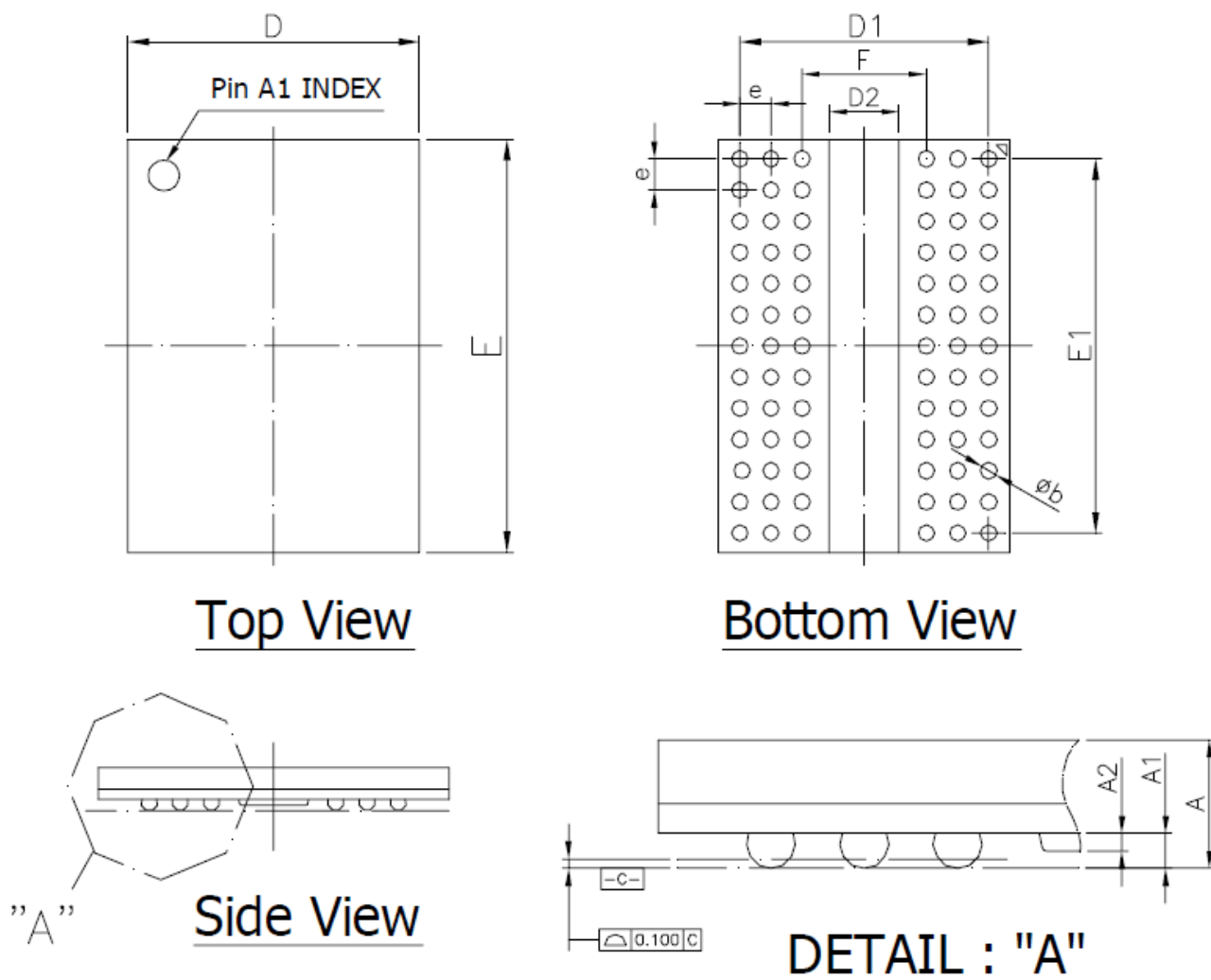
Figure 4. Block Diagram (x8)

Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.039	--	--	1.00
A1	0.010	--	0.016	0.25	--	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

Figure 5. 96-Ball FBGA Package 7.5x13x1.0mm(max) for x16



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.039	--	--	1.00
A1	0.010	--	0.016	0.25	--	0.40
A2	--	--	0.008	--	--	0.20
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.413	0.417	0.421	10.50	10.60	10.70
D1	--	0.252	--	--	6.40	--
E1	--	0.378	--	--	9.60	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
D2	--	--	0.081	--	--	2.05

Figure 6. 78-Ball FBGA Package 7.5x10.6x1.0mm(max) for x8