Emerging Technology and Business Solutions for System Chips

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I. INTRODUCTION

In the last three decades, the IC industry has developed from Small-Scale Integration (SSI, with only a few transistors on a chip) to today's GigaScale Integration (GSI, with $\geq 10^9$ transistors on a chip) [1]. Silicon technology has been scaled from a linewidth of a few microns to less than 0.1 microns, and has migrated from NMOS to CMOS. In adjunction to Moore's Law [2] and Dennard's scaling theory [3], Meindl has derived a Chip Performance Index (CPI) to measure how technology integration and scaling generate signal-transfer robustness per unit of energy (input energy ≡ power-delay-product: $P \bullet \tau$, in Joules) from 10^{13} devices/J in SSI to 10^{24} devices/J in GSI for digital switches. Therefore, electronic systems (ES) could be produced at a lower cost, in smaller formfactors, and with more complicated functionality, by using more and more IC content. This drove the migration of computer systems from bulky mainframes to compact PCs.

The business structure of the mainframe computer industry in the '70s was based on the *vertical integration* of a *closed* system within one company; that is, most of the knowledge used to build an ES, covering specialized skills in the *application*, *system architecture*, *software and hardware* segments (Fig. la), was developed and owned by individual companies with internally defined standards; for example, IBM's mainframe computers and AT&T's phone switching systems. The corresponding vertically integrated business structure in the IC industry included an integration of application and subsystem design, chip design, wafer fabrication, and packaging and testing, within a single company (an *Integrated Device Manufacturer* model: IDM) (Fig. 2a). The pervasive use of ICs has since facilitated the creation of open systems such as PCs, which allow the insertion of IC components and software, even after the ES framework has been built. Open systems defined clear interfaces across different knowledge segments, forming standards in the public domain and thus creating business opportunities for companies with unique core competencies, such as Microsoft in software, IBM and HP in systems and service, and Dell in channel segments, respectively (Fig. 1b). The impact on the IC industry was to create more business opportunities to sell *standard* IC components in massive volume, allowing companies such as Intel to flourish. Therefore, in the mid-80s through the 90s, a new *horizontal segmentation* of the original IDM business structure in the IC industry created many new companies whose products focused on specialty knowledge segments, which include value-added distributors with special application skills, innovative design *fabless* companies, independent photomask shops, pure-play foundries for wafer manufacturing, and packaging and testing vendors (Fig. 2b).

II.SYSTEM CHIP TRENDS

This work describes both changes and trends in the technology development and business structures of the IC industry as it enters the 21st century. As both circuit techniques and process technologies, specialized for digital, analog, memory, or RF functions, advanced rapidly through the late 90s, ICs with various functions were developed to further reduce the cost and size of electronic systems, as well as to diversify their applications. The long-standing demand for a portable networking ES has driven the emergence of *mobile intelligence appliances* (MIA) such as PDAs, portable audio/video devices, bluetooth/GPS/other autoand home-connectivity devices, digital cameras, and cellular phones, whose shipping units alone have exceeded that of PCs Interestingly, these MIAs were built as vertically integrated closed systems with an additional constraint that they be of a limited size (that is, with volume measured in cm^3), but the system complexity is dramatically increasing along with the end user's desire for complete 4C (Computer, Communication, Consumer, Content) functionality through a single MIA - for instance, an advanced cellular phone is being made with fewer but more complex ICs to present voice, data, and image communication features, along with multimedia entertainment functions and a camera, or even video recording. The pressure to drive down both cost and size while increasing the functionality embedded in MIAs requires most subsystem functions to be implemented in ICs. These ICs need to merge digital, analog, memory, RF, and power-related IC functions (referred to, below, as the five IC *families*), as much as possible into a smaller packaging formfactor - An era of system chips (SC) is emerging! It is believed that once the technology has matured, system chips will also be used for general applications. One trend being followed is to design an SoC (System-on-a-Chip), which includes all or part of five families on a single die (Fig. 3a). Another alternative, known as SiP (System in a Package), is to assemble different IC family dies horizontally on the same substrate within a package (Fig. 3b). Meanwhile, a new technology permitting the *stacking of Multiple dies* in a small *Chip Scale Package* (MCSP) is emerging, which allows the third-dimension to be used to achieve higher density in a given footprint area. One example of a Stacked CSP is a Memory Combo that includes two to six layers of memory in a BGA package (Fig. 3c). Besides conventional wire bonding, flip-chip techniques using solder bumps and interpolation layers are being adopted increasingly.

A key challenge to the prosperity of the future IC industry is how to effectively assemble multiple functions into a limited formfactor with justifiable cost controls while being able to optimize performance of individual families which usually have behaviors that are too distinct to be easily merged onto a single die.

Moore's Law pointed out that a driving force behind growth in the IC industry, especially for digital and memory ICs, is the impetus to place more transistors on a two-dimensional die area [2]. Meindl showed that such a driving force results in an exponential increase of CPI(digital) (CPI(d) ≡$N/P \bullet \tau$, i.e. the number of components per unit of energy, in $Joule^{-1}$) by 100 billion times from SSI to GSI (Fig. 4) [1].

To analyze the behavior of analog-circuit chips as technology is scaled, a CPI(analog) is described here by simplifying the Figureof-Merit (FoM) defined in [4]:

$$CPI(a) \equiv \frac{(S/N)}{P \bullet \tau} \text{ (units: Joule}^{-1}\text{)}$$

where S/N is a signal-to-noise ratio. According to published data on pipeline A/D converters, the CPI(a) generally improves as technology is scaled, but the CPI(a) of the best designs for each technology generation reaches a barrier regardless of device scaling (Fig. 5). This indicates that the highest ratio of S/N per unit energy consumed in such analog circuits is not significantly improved even when technology is scaled, especially if signals are actually reduced due to the scaling of supply-voltage levels from 5V down to 3V or 1V. The sampling frequency can be increased through technology scaling, i.e. τ is reduced. However, reducing t is subject to the tradeoff that more power needs to be consumed in order to maintain the

S/N under a saturated CPI(a). Thus, integrating an ADC onto an advanced digital chip, for instance, with a 90nm technology under a 1-V supply, which may be subject to a power-consumption limit, may not be an optimal solution.

For radio-frequency chips, a simplified CPI(RF) has been developed to study the behavior of RF ICs such as low-noise amplifiers (LNAs) and single-chip receivers (including LNA, mixer and phase-lock-loop circuits on one CMOS chip):

$$CPI(RF) \equiv \frac{1}{P \bullet \tau \bullet (NF-1)} \equiv \frac{N_{in} \ / \ \Delta N}{P \bullet \tau} \text{ (units: Joule}^{-1}\text{)}$$

where NF is the Noise Figure ($\equiv (S/N)_{in}/(S/N)_{out}$), ΔN ($\equiv N_{out}$/gain - N_{in}) is the input referred excess noise, and N_{in} and N_{out} are noises at the input and output, respectively. As technology is improved, the noise-level-suppression capability per unit of energy consumption is improved in both CMOS LNA chips and single-chip receivers (Fig. 6). Although the effect of technology scaling on CPI(RF) is positive, sensitive control of the NF in RF circuits may prohibit optimization of RF circuits with the other circuit families on the same die.

The memory systems used in today's PCs are composed mostly of RAMs, including SRAMs as cache memories embedded in CPU chips and DRAM modules as main memories, and rarely use non-volatile memories. The size of main memories is determined by how many DRAM modules are used, and can be modified after the system has been built as long as vacant slots are available for inserting DRAM modules. However, the memory systems in MIAs are different: they need both RAMs and non-volatile memories and can hardly be changed after the system has been built. In order to shrink the size of memory systems, the pressure is to integrate the entire memory system into one IC package. This memory-system IC must be specifically targeted to application needs and meet a strict cost-performance target, since it is hard to alter memories once the system plan is frozen. Therefore, MIAs are driving a new trend toward developing memory chips in an *application-driven way,* here termed *application-driven memory* ICs (ADM) (note that ADMs are not application-specific because cost concerns drive designers to target ADMs at common denominators of specifications for multiple memory systems used in several applications). An ADM used in a cellular phone appeared in 1998 as a Combo having a 4Mb low-power SRAM stacked over a 32Mb flash memory, and has been advanced to today's top-line Combo containing five layers of memories, such as an 8Mb low power SRAM stacked on a 32Mb Pseudo SRAM, sitting atop a 128Mb low-power DRAM, built on a 64Mb NORFlash, which is stacked on a 256Mb NAND-flash (Fig. 7). Since an ADM is already a heterogeneously integrated system chip, it is hard to use one analytical formula to define the metrics that an ADM is expected to achieve. Various CPIs can be used to measure different aspects of an ADM's performance. For example, a CPI_1 (ADM) is used to understand the cost implication of an ADM:

$$CPI_1(ADM) \equiv \sum \frac{(BC_i \bullet \sigma_i \bullet n_i)}{A_P} \text{ (units: bits/cm}^2\text{)}$$
$$= \frac{BC_{SRAM} \bullet 16 + BC_{PSRAM} \bullet 3 + BC_{DRAM} \bullet 2 + BC_{NOR} \bullet 4 + BC_{NAND}}{(L_{max} + \Delta L) \bullet (W_{max} + \Delta W)}$$

where BC is the number of bits (called bit capacity), o is a density factor used to adjust the equivalent cost to be proportional to the number of bits (e.g. BC_{SRAM} times16 is equivalent to BC_{DRAM} times 2 under an assumption based on a 6-Transistor SRAM cell versus a one-transistor DRAM cell), n is the number of chips of the kind in the stack, A_P is the footprint area of the package, L_{max} and W_{max} are the maximum length and width of all stacked dies, and ΔL and ΔW are the length and width of rims required for packages, respectively. One should note the significant difference between CPI_1 (ADM) and commodity DRAM's CPI, which is given by BC/Chip-Area. Another measure of ADM performance is focused on their speed and power:

$$CPI_2(ADM) = \sum \left(\frac{BC_i}{P}\right) \bullet \left(\frac{nIO}{\tau}\right) \quad \text{(units: bits}^2\text{/Joule)}$$

where nIO is the number of Inputs and Outputs, and power (P) and bandwidth (nIO/τ) are measured parameters.

A study of these CPIs for the four IC families reveals that they exhibit quite different behaviors as technology is scaled. Combining different families on a die with a combined technology base may not permit an optimized solution. With the rapid development of SoC, SiP, and Stacked CSP technologies, it is envisioned that the most powerful system chip in the coming decade should incorporate *an integrated structure using multiple dies with heterogeneous* technologies and voltage operations, which fully utilize the multi-dimensional space within a CSP package. An example would include separately connected building blocks, including a stack of memory dies, an analog die overlaid on either a SoC or digital die, and an independent RF die, located on top of a multi-layer interconnected substrate inside a package, each with different control and I/O paths (Fig. 8). In addition, control software would be coded into the non-volatile memory in the memory stack. Making an appearance on the IC technology horizon is such a new technology known as *Multidimensional Die-integration System Chips* (MDSCs)! The architecture of MDSCs can be conceptualized as a Metropolitan-citylike Die Society Cluster, structured similarly to modern-day cities such as New York or Taipei! It is projected that in addition to continuously increasing the number of transistors on a "digital die", or merging more functions on a "SoC die", MDSCs will permit another level of integration that emphasizes functions *heterogeneously integrated* together. This can be accomplished by using different family dies with extensions to a 3-D vertical stack and/or to parallel placement in the neighboring vicinity, all within an advanced package using a multi-layered substrate structure. How to design an effective SC using either SoC, SiP, or MDSC, can be analyzed by using a generalized metric with individual CPI studies, including various cost evaluations to select correct technologies and ways of functional partitioning for optimal integration:

$$CPI(MDSC) = \frac{f(CPI(d), CPI(a), CPIj(ADM), CPI(RF))}{V_P}$$

where V_P is the IC package volume (cm^3).

III. EMERGING BUSINESS STRUCTURES FOR SYSTEM-CHIP (SC) PRODUCERS

IC companies face challenges from the risks induced by technology obsolescence and cyclic business shakeouts. A successful company must at least have a superior technology or a correct business model that fits with industry trends. During the 70s to the mid-80s, the IC industry was characterized either by *vertical captive systems* or by *innovative technologies.* Thus, vertically integrated companies, such as IBM, and start-ups, such as Intel, which first introduced innovative products such as microprocessors and DRAMs, were able to flourish. From the mid-80s into the 90s, industry trends shifted to favor open systems driven by *standard-product mass producers,* such as Japanese IDMs, with strong manufacturing power, especially in memories. From the 90s to today, industry trends gave rise to *design-fabless* and foundry companies with core competencies either in their products

or fast and flexible deliverables, such as nVidia, TSMC, and Xilinx. Especially notable was TSMC, whose success arose from its consistent pure-play foundry business model. This business model won the trust of customers who drove the explosive growth of TSMC, even though, from its early years through the mid-90s, TSMC's technology lagged behind those of IDMs who also offered foundry services but had their own products which competed with those of their fabless customers. The coming SC era will be characterized by more stringent competition based on advanced technologies with larger investments and shorter product cycles, and driven by *application needs* and *multiple-heterogeneous-function integration.* A successful company must have a correct business structure and positioning in addition to its essential technical competence. What follows describes several emerging business models being developed by contenders in this new *SC Olympics.*

Although implementing an MIA system has brought back vertical system integration, the required business model is different from that of the mainframe period due to the significant *interactive modes* between the four ES segments – channel/application, system architecture, software, and hardware/ICs. The new vertically integrated system should not be viewed as a closed system, but should be developed as an integrated *circle* with direct interactions between any two segments, even between the application layer at the top and the IC layer at the bottom, thereby allowing faster SC product introduction (Fig. 1c). Due to horizontal segmentation in the 90s, however, not many companies today are capable of developing and owning technologies in all four segments. Instead, each segment has several successful specialty companies. A *clustered* integration structure allows various companies with complementary skills from different specialty segments to either form alliances or partnerships, rather than to undergo merger and acquisition, in order to realize effective vertical integration of knowledge. To shorten the product designwin cycle, companies in clusters need to engage each other early on to co-define specifications and to begin *co-development* sooner. Organizing a cluster of companies together to achieve effective vertical integration is termed *Clustered Virtual Vertical Integration* (CVVI). Since SCs need to be developed just like integrated electronic systems, business structures based on the CVVI of IC companies are emerging as a basic model for future cooperation and growth (Fig. 2c).

Several business models have been developed by major companies in the IC industry, each of whom possesses strong clustering forces. IBM started out as an IDM, but branched out a business division that provides contract manufacturing services using standard cells, is licensing IP and technologies to selected partner companies, and co-develops advanced technologies in multiple alliances. In mid-2002, IBM further formed a *Technology and Engineering Service Division* to provide skills in various specialty segments to serve contract customers who have valuable application and business channels. This new business model allows outsiders to use IBM resources to co-develop products so that IBM and its partners can win markets together. IBM, wellknown as a completely vertically integrated company since the early days of the IC industry, has thus made major strides to be virtually vertically integrated.

In the 90s, TSMC played a major role in stimulating the fast growth of both fabless and foundry companies, the company will continue to maintain its pure-play foundry role to ensure no conflicts of interest with its customers. However, the necessity for CVVI has been recognized, and TSMC is focusing its efforts on co-developing essential technologies with its customers and suppliers, which have requisite knowledge in specialty segments, so that TSMC and its customers may achieve win-win results. For example, TSMC is co-developing flip-chip packaging technologies with assembly manufacturing partners by prototyping direct chip attachment inside a package using TSMC's 12-inch wafers. The complete backend service will be the business of TSMC's partners at the time of mass volume production, however. TSMC is also co-developing 90-nm-technology design-automation tools with EDA company partners to ensure that TSMC's customers can effectively take advantage of TSMC's advanced technologies without delay and misuse.

UMC is the second-largest wafer foundry and has played a significant role in creating partnerships between fabless and foundry companies. In the mid-90s, UMC invited many fabless companies to form several joint-venture factories so that these partners could secure wafer volumes. UMC's business model for the future is to continue as a wafer foundry with a strong emphasis on customer partnership. In order to ensure a diversified and sufficient customer base, however, UMC may choose to invest in some design companies while instituting all possible measures to avoid conflicts of interest with existing customers. UMC believes that healthy cooperation with customers should be based on its own technical proficiency and outstanding services, rather than simply on investment relationships.

Most Japanese Semiconductor Manufacturers (JSMs) were essentially IDMs. However, the business downturn of the past few years has triggered JSMs to either reorganize within themselves or restructure with other companies, leading to two major types of business structure. Most DRAM activity was consolidated into a DRAM specialty manufacturer, Elpida, or was licensed to emerging manufacturers in Taiwan or China. The remaining JSMs are now IDMs without DRAMs, and are focused on SoC, SiP, Combo, and IP development. Meanwhile, JSMs are preparing for the MDSC era and are attempting to be more open to their outside customers with their IP and technologies including some of their leading-edge results. Toshiba has led the creation of the "*SoC-centric Open IDM*" model, which aims to supply application-driven IP licensing, to build up a process technology and automation platform, and to provide partners with product development and foundry integration, by using both SoC and SiP solutions [5]. NEC also aims to establish cooperative relationships with fabless companies, and to provide platform solutions in order to realize shorter design turn-around-times for prototyping and mass production [5]. JSMs are business-savvy enough to try to obtain larger market share by exploiting synergy with their design/system customers by utilizing their sustainable technology strengths.

Samsung Electronics Company started as an electronic system house and developed its semiconductor division as an IDM. With recent successes in ICs, displays, cellular phones, home appliances, and games, however, Samsung is migrating towards a vertically integrated business structure. For MIA products, Samsung has the capability to produce all four system segments, which is one of the reasons why Samsung has achieved business success in the last two years despite the economic depression and the IC industry downturn. Samsung is smartly mixing “closed and owned” technologies with technologies that are “the best imported from the outside" through a vision of Collaborative Alliance [5]. Therefore, the CVVI model is also applicable to Samsung

In short summary, the five selected powerful corporate forces mentioned above are adopting different strategies based on their

individual histories and core competencies, but are taking aim at a common goal – to ensure that they are ready for CVVI to capture a tremendous opportunity for business growth with their clustering force.

Facing the growing SC era, system manufacturers are working actively to secure sources for custom-designed, application-driven SCs in order to meet their business requirements. One way for system manufacturers to achieve this target is to form clustered programs with several IC design companies who can provide multiple functionality dies that can be merged together for MDSC. In this model, the system house is the leader of the cluster, and sometimes controls the software used for the SC. Another way for the system house to play a role as a virtual IC house is to directly engage a new breed of fabless companies called *design-foundry* companies. Design-foundry companies provide both IP and design services, including a turnkey supply of SCs to meet whatever requirements the system house needs. This type of design-foundry company is valuable in the CVVI supply chain since it complements what the system house lacks in IC knowledge, and allows customers to fully own the IP rights of the final products. In order to expand their knowledge bases in various technology segments, design-foundry companies usually form alliances with specific wafer-foundry companies and/or EDA companies – examples include the partnerships between Faraday Company and UMC, as well as between GUC (Global Unichip Company) and TSMC.

There are two key points with regard to the business aspects of the emerging SC industry: First, the success of SC will significantly increase the IC content in electronic systems as MDSC creates additional value over discrete chips. This will be important in helping the IC industry to regain its growth momentum, and to prevent the IC industry from becoming a mature industry. MDSC's merits should help to increase profit margins, thus pulling the industry out of the micro-profit age in which business was only driven by the manufacture of commodity ICs. Secondly, because MIAs are coming into direct contact with end users, the sales volume of these systems is directly proportional to the consumer population. Thus, the SC industry will broaden the restrictive IC industry focus from one that has always prioritized B-to-B (Business) over B-to-C (Consumer), to a view that focuses on B-to-C first and B-to-B second. As a result, *localization* to meet local regional needs also stands out in its importance within today's *globalization* trend. Therefore, SC designers must understand the cultural differences between various end users in different regions in order to be successful. This challenge has rarely been experienced by the IC design community, except for consumer-product companies.

IV.DESIGN AND TECHNOLOGY CHALLENGES FACING VIRTUAL VERTICAL INTEGRATION FOR SYSTEM CHIPS

In parallel with business-structure reform, a CVVI of both design and technology is required to achieve MDSC, because rarely can a single company own all the complete knowledge necessary to succeed in this endeavor alone. Thus, the key to success is how to connect IC knowledge with system knowledge. The complete list of challenges that must be overcome before SCs can reach MDSC maturity is longer than that which can be elaborated here, but several major ones are: (1) Long-time-reliable Known-Good-Die (KGD) technologies with early design for reliability (DFR) and effective production-cost controls; (2) Multilayer interconnected substrates, even including passive components sandwiched inside the layers; (3) Micro-assembly technologies covering thinning wafers, stacking multiple dies, either flip-chip or wire-bonding to the substrate or from die to die, and encapsulating chips; (4) Signal integrity on inter-die, intra-die, and from multiple dies on the substrate to the outside world, including interactions between the MDSC and the system field environments; (5) Supply-voltage management on multiple-family dies and power control of the entire SC to meet both DC and AC requirements; (6) Simulations for die to die, die to package, and package to field, to reduce the cost of MDSC experiments; (7) Testing and verification of multiple circuit family behaviors; (8) Repairability, error correction, programmability, etc.; and (9) All development challenges that must be overcome to migrate from GSI to Terascale Integration (TSI) in each specialty segment. Although the difficulties of system integration have been experienced during the evolution of SoC, the more critical technical challenges facing CVVI will stem from early co-development between different segments, such as between SoC designs and nanometer device technologies, wafer fabrication and assemblyprocess technologies, etc. Thus, the winning clusters in the SC era will be determined by how well and thoroughly companies can closely implement CVVI in their technologies.

The Taiwanese semiconductor industry provides an illustration of the progress of CVVI among various companies and allows a glimpse into worldwide CVVI efforts. The Taiwanese IC industry has grown in a horizontally segmented way, starting from the 80s, and now includes approximately 225 fabless-design companies, 14 design-foundry and IP companies, 8 wafer foundries, 6 IDMs, 4 mask shops, 44 assembly vendors, and 35 testing houses. A fast-growing number of clusters, which involve Taiwanese companies with collaborators from around the world, have been formed to pursue CVVI. Some examples of technical interactions within these clusters are described below:

As an example of the CVVI of design and fabrication segments, TSMC has been co-developing advanced-technology designautomation flow environments with EDA vendor partners. Targeted at 90nm and beyond, TSMC's *Reference Flow* defines Deep-Sub-Micron and Design-for-Manufacturability issues and provides solutions before designers start to adopt advanced technology nodes. By demonstrating how to optimize power and speed tradeoffs with an ARM processor, Reference Flow 4.0 provides simulations on how leakage and power has been minimized while keeping the same clock speed by using various MultiThreshold-Device solutions. Another example is that of GUC, a *design-foundry* company in a cluster with TSMC, that has developed a digital audio/video (DAV) SoC platform so that various system houses can co-define their SoCs with GUC. Specific designs can then be quickly derived from the platform, and chips can rapidly be implemented with appropriate advanced wafer and packaging technologies. An advantage of the aforementioned partnerships is to facilitate the accumulation of learning, and to secure a faster and smoother technology-scaling path in order to meet increasing design-complexity and decreasing timeto-volume demands. An increasingly important issue for systemchip implementation is the rapidly increasing cost of mask sets. Providing multichip projects on a wafer or sharing the mask cost among partners in a cluster are possible solutions.

As an example of the CVVI of mixing design, device, and packaging technology segments, Etron Technology Company has developed various KGD technologies for different memory Combos, including ultra-low-power SRAMs, low-power psuedo-SRAMS, low-power SDRAMs, and multiple-die-stacked broad-bandwidth DDR SDRAM chips. Under a fabless model, Etron has formed partnerships with system customers and specialty wafer foundries (some specializing in SRAM technologies and others in DRAM technologies), allowing Etron to introduce its products more rapidly

and to succeed in maintaining its long-term reliability to less than 200 dpm (defects per million) in customers' final Combo products. Thus, Etron's KGD design and technology is an excellent example of how to leverage a company's unique fabless advantages by utilizing CVVI business structures to select specialty foundries that are best suitable for each product optimization.

As for manufacturing segments, which include wafer fabrication, packaging, and testing, it is informative to examine the technical interactions between partners from various segments aimed at achieving faster MDSC integration success. While TSMC and UMC are entering 90nm-CMOS 12-inch-wafer manufacturing and have started development toward 65nm technologies, one key challenge is how to realize a cost-effective manufacturable photolithography process. Among the wafer, equipment, and photoresist manufacturers, TSMC is driving and coordinating the development of a new *Immersion Lithography* technology, which can shorten the current 193nm wavelength to 134nm by modifying today's Dry system, thus increasing resolution by 44% and Depthof-Focus by 200%. The Advanced Semiconductor Engineering (ASE) Company has co-developed various SiP technologies with its customers: either Stacked-die or Stacked-package CSP as well as modules supporting multiple dies. Besides surface-wire-bonding assembly, companies such as ASE have provided *flip-chip turnkey* capabilities from wafer bumping, bumped-wafer probing, and assembly, to final tests across various chip forms, such as SoC, SiP, or even MDSC. ASE's stacked-die packages can be based either on leadframe or substrate containing up to 5 dies. Chip connections can be achieved through wire bonding, or a combination of wire-bonding and flip-chip, where the flip-chip die can be on top of or beneath the wire-bonded die. Packaged dies can also be stacked in a multi-package BGA, which offers advantages in that the device can be tested fully before assembly and can sometimes use heat slugs to facilitate heat dissipation. Recently, multichip modules, which can be viewed as simplified MDSC packages, have been widely adopted for the packages used with graphics processors and high-end controllers, in addition to their traditional use with RF devices. The key challenges in this field include wafer thinning and reduction of the substrate thickness. At ASE, the grinding of 8-inch-wafers to 2-mil and 12-inch-wafers to 4-mil thicknesses, respectively, has become a manufacturing reality. An example of a multi-chip module is a digital drive packaged and tested at ASE containing 6 flip-chip devices, 9 Wafer-Level CSPs, 4 Very-Fine-Pitch BGAs and 130 surface-mount devices on a substrate of one-inch square. Known-good-die and reworking issues are key challenges that must be overcome to bring multi-chip modules into production. In the specialty-testing segment, Ardentec Company was founded in 2000 in Taiwan and is dedicated to wafer-level and KGD testing-technology services across several IC families. Another startup company in Taiwan, MEGIC, has developed a *Freeway-like Interconnect* technology having thick metals (~5µm copper) and thick dielectrics (~5µm polyimide) on top of the conventional IC passivation and metal layers. This approach applies printed-circuit-board (PCB) process techniques and interconnect architecture to IC wafers, which is particularly useful for SoC design. The Freeway-like architecture has been implemented in a 1Gbit Ethernet four-port transceiver chip. Without a Freeway-like metal scheme, the chip could only drive a copper cable over a 120-meter distance with a voltage supply of 1.5V, and could not meet the specification of a 150 meter drive distance. The addition of a Freeway-like metal scheme not only solved the performance problem, but also reduced the supply voltage from 1.5V down to 1.2V.

As for the silicon Intellectual Property (IP) system segment, an *IP mall* has been established in Taiwan. Many design companies, universities, and industrial research labs have all launched efforts to develop their own silicon IP and are attempting to find more opportunities to license or exchange IP. Interestingly, IP is being licensed even to competitors as long as the IP is used in non-competing areas; thus, *coopetition* should occur quite often as companies get used to *cooperating* and *competing* with each other in the CVVI era.

Finally, several Taiwanese system companies, many of which are leaders in the hardware manufacturing segment, have launched different strategies to deal with the CVVI era. Such has been the experiences of Quanta Computer as a notebook ODM Company, BenQ as a LCD monitor company that has formed a closely-integrated joint-venture called AU Optronics Company as a LCD panel supplier, and Inventec Company, which has combined cellular phones and PDAs and differentiated itself from its competitors by focusing primarily on Chinese users, by smartly adopting various types of application-driven memory and system chips as jointly configured with IC suppliers. These efforts have clearly shaped the CVVI trend of integration across clusters between the electronic system and IC industries.

V.CONCLUSIONS

Monolithic integrated circuits in planar technologies have long served as a driver of the IC industry's successes. For this period, trends in the development of monolithic IC chips have been best measured by Moore's Law, which counts the number of transistors that can be integrated in a two-dimensional die area. Recently, a new IC landscape, best characterized as *Heterogeneous Integration* (HI) of various functions into a single system chip, has developed, motivated by the fast growth of Mobile-Intelligence Appliances. Besides incorporating SoC trends, future system chips will fully utilize multi-dimensional integration, within a single package, of multiple dies that cover a variety of digital, analog, memory, and RF functions and technologies. Measurement of development trends in this new era must focus on the number of functions per unit volume in a limited footprint area, and the ability to achieve low operational energy. Correspondingly, business models of IC companies, which have evolved from vertical integration to horizontal segmentation, must change. In order to meet the challenges of HI, they should adopt *virtual vertical integration, with multiple companies in clustered partnership* operations. Interesting parallels between technical and business activities in the emerging world of heterogeneous integration in system chips have been presented, using Taiwanese IC companies with their global partners, as examples.

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[1] J. D. Meindl, et al., "Prospects for Gigascale (GSI) Beyond 2003,"ISSCC Dig. Tech. Papers, pp. 124-125, Feb. 1993.
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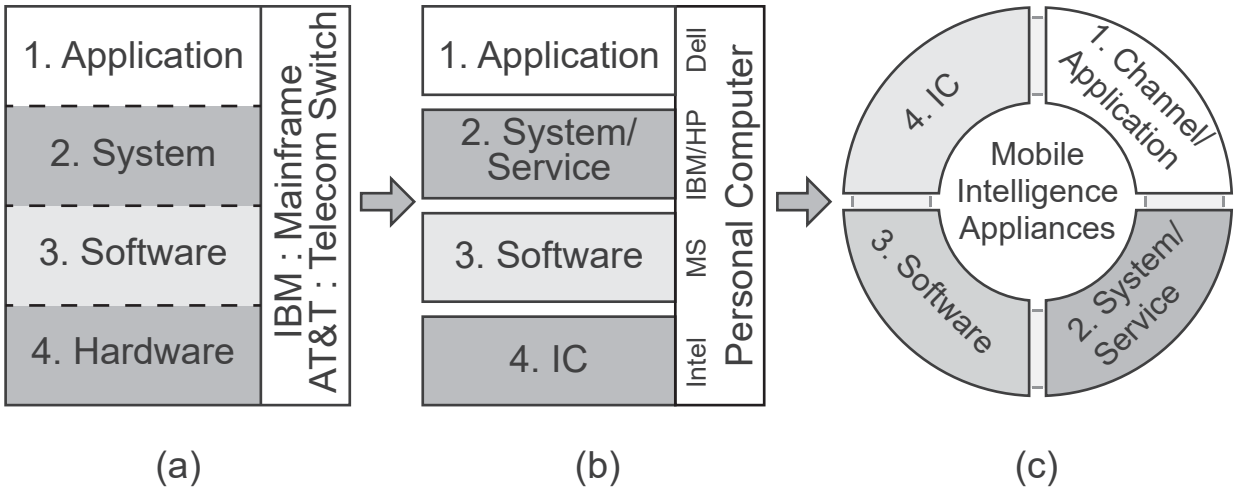

Figure 1.2.1: Business structure evolution in electronic systems: (a) vertical integration within one company, (b) horizontal segmentation for open systems, and (c) virtual vertical integration of multiple companies in clustered integrated circles.

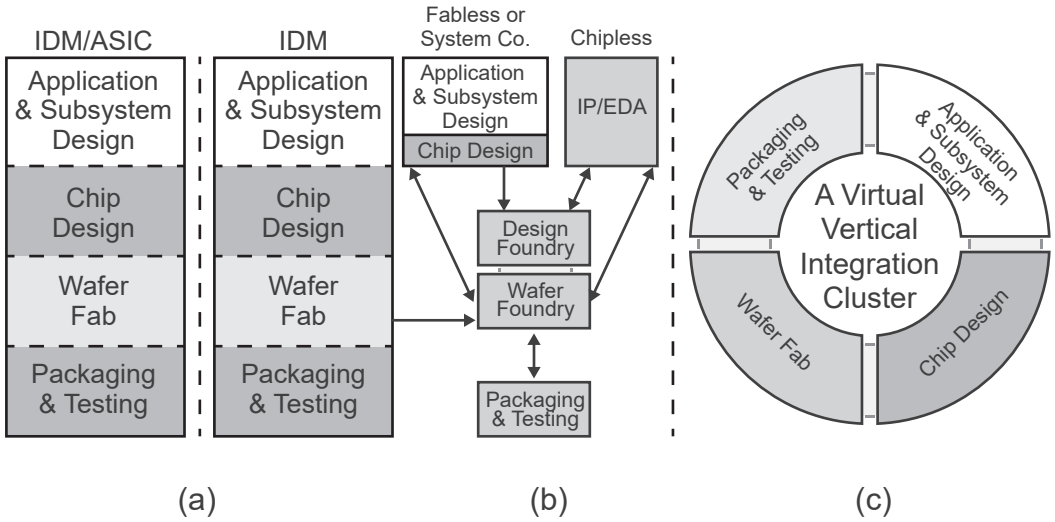

Figure 1.2.2: IC business structure changes: (a) '80s: IDM/ASIC, (b) '90s: emerged fabless, system house, design foundry, wafer foundry, and backend service (F. Tseng, VLSI '99; N. Lu), and (c) emerging clustered virtual vertical integration of multiple companies; the Chip-Design segment includes fabless, chipless, and design foundry (N.Lu).

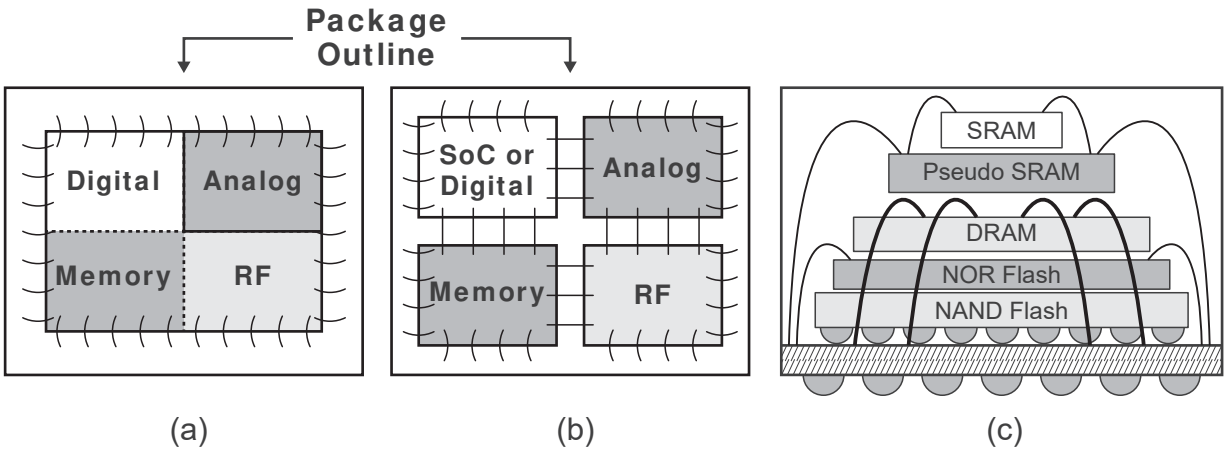

Figure 1.2.3: A schematic illustration of various system-chip structures: top views of (a) a SoC and (b) a SiP, and a side view of (c) a stacked memory combo.

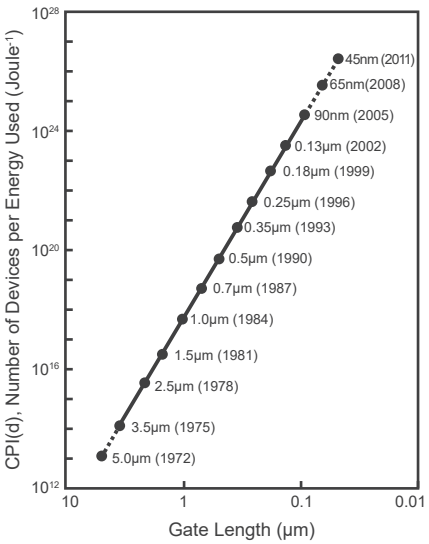

Figure 1.2.4: Chip performance index for digital-circuit chips (J. Meindl[1]).

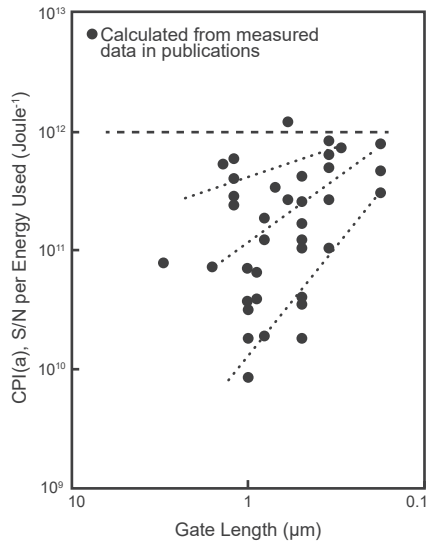

Figure 1.2.5: Chip performance index for analog-circuit chips (J. Wu and N. Lu).

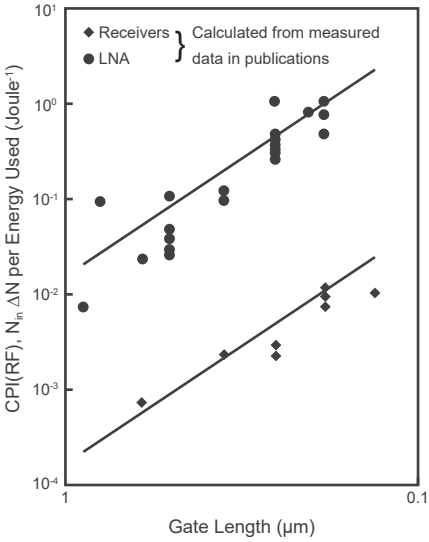

Figure 1.2.6: Chip performance index for radio-frequency-circuit chips (S. Lu, N. Lu, and H. Chiu).

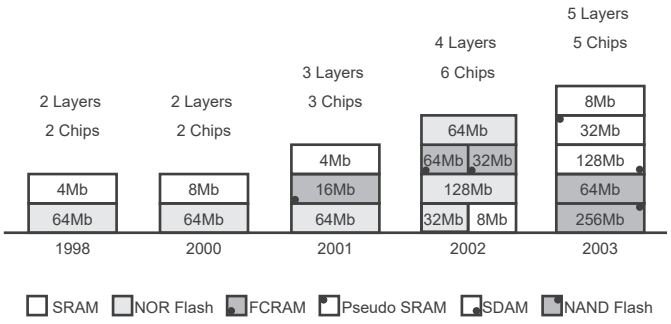

Figure 1.2.7: Evolution path of stacked memory combo's (Samples from 2001 and 2002 were taked from Fujitsu's product announcements).

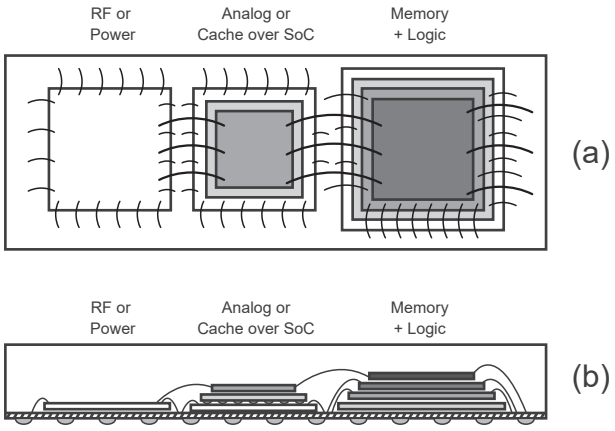

Figure 1.2.8: A schematic illustration of an MDSC (Multi-dimensional Die-integration System Chip) structure: (a) top view and (b) side view.

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