

# **Embedded Multi-Media Card (e.MMC)**

## **Flash Storage Specification e.MMC 5.1 HS400**

EM74J08LVAGC-H

## **Revision History**

| <b>Rev</b> | <b>Date</b>    | <b>Comments</b>                                                                    |
|------------|----------------|------------------------------------------------------------------------------------|
| 1.00       | April 24, 2025 | Initial release                                                                    |
| 1.01       | May 16, 2025   | 1. Adjust the format and wording<br>2. Revised definition of operating temperature |

Etron Technology, Inc. reserves the right to change products or specification without notice.

## Contents

|          |                                                                      |           |
|----------|----------------------------------------------------------------------|-----------|
| <b>1</b> | <b>Introduction.....</b>                                             | <b>6</b>  |
|          | 1.1 Product Features .....                                           | 6         |
|          | 1.2 e.MMC Specific Feature .....                                     | 7         |
| <b>2</b> | <b>Ball Assignment .....</b>                                         | <b>8</b>  |
|          | 2.1 Package Configuration .....                                      | 8         |
| <b>3</b> | <b>Specification .....</b>                                           | <b>9</b>  |
|          | 3.1 System Performance .....                                         | 9         |
|          | 3.2 Power Consumption.....                                           | 9         |
|          | 3.3 Partition Capacity.....                                          | 9         |
| <b>4</b> | <b>e.MMC Device and System.....</b>                                  | <b>10</b> |
|          | 4.1 e.MMC System Overview .....                                      | 10        |
|          | 4.2 Memory Addressing .....                                          | 10        |
|          | 4.3 e.MMC Device Overview .....                                      | 11        |
|          | 4.4 Bus Protocol.....                                                | 12        |
|          | 4.5 Bus Speed Modes.....                                             | 12        |
| <b>5</b> | <b>e.MMC Functional Description.....</b>                             | <b>14</b> |
|          | 5.1 e.MMC Overview .....                                             | 14        |
|          | 5.2 Boot Operation Mode.....                                         | 14        |
|          | 5.3 Device Identification Mode.....                                  | 14        |
|          | 5.4 Interrupt Mode.....                                              | 14        |
|          | 5.5 Data Transfer Mode .....                                         | 15        |
|          | 5.6 Inactive Mode.....                                               | 15        |
|          | 5.7 H/W Reset Operation.....                                         | 15        |
|          | 5.8 Noise Filtering Timing for H/W Reset .....                       | 16        |
|          | 5.9 Enhanced User Data Area.....                                     | 16        |
| <b>6</b> | <b>Register Settings .....</b>                                       | <b>17</b> |
|          | 6.1 OCR Register.....                                                | 17        |
|          | 6.2 Card Identification Register (CID) .....                         | 18        |
|          | 6.3 Card Specific Data Register [CSD].....                           | 19        |
|          | 6.4 Extended Card Specific Data Register [EXT_CSD] .....             | 20        |
|          | 6.5 RCA Register .....                                               | 24        |
|          | 6.6 DSR Register .....                                               | 24        |
| <b>7</b> | <b>e.MMC bus .....</b>                                               | <b>25</b> |
|          | 7.1 Power-up.....                                                    | 26        |
|          | 7.2 Bus Operating Conditions.....                                    | 28        |
|          | 7.3 Bus Signal Levels .....                                          | 32        |
|          | 7.4 Bus Timing .....                                                 | 34        |
|          | 7.5 Bus Timing for DAT Signals During Dual Data Rate Operation ..... | 37        |
|          | 7.6 Bus Timing Specification in HS400 mode .....                     | 39        |
| <b>8</b> | <b>Package Outline Information .....</b>                             | <b>42</b> |

## List of Figures

|                                                            |    |
|------------------------------------------------------------|----|
| Figure 2-1. 153-FBGA Ball Assignment (Top View) .....      | 8  |
| Figure 4-1. e.MMC System Overview .....                    | 10 |
| Figure 4-2. HS400 Host and Device block diagram .....      | 13 |
| Figure 5-1. H/W Reset Waveform .....                       | 15 |
| Figure 5-2. Noise Filtering Timing for H/W Reset .....     | 16 |
| Figure 7-1. Bus Circuitry Diagram .....                    | 25 |
| Figure 7-2. Power-up Diagram .....                         | 26 |
| Figure 7-3. e.MMC Power Cycle .....                        | 27 |
| Figure 7-4. Power Cycle Requirement .....                  | 27 |
| Figure 7-5. e.MMC Internal Power Diagram .....             | 28 |
| Figure 7-6. HS400 reference load .....                     | 31 |
| Figure 7-7. Bus Signal Levels .....                        | 32 |
| Figure 7-8. Timing Diagram .....                           | 34 |
| Figure 7-9. Data Input/Output in Dual Data Rate Mode ..... | 37 |
| Figure 7-10. HS400 Device Data input timing .....          | 39 |
| Figure 7-11. HS400 Device output timing .....              | 40 |
| Figure 8-1. Package Outline Drawing Information .....      | 43 |

## List of Tables

|                                                                           |    |
|---------------------------------------------------------------------------|----|
| Table 1-1. Product Information .....                                      | 6  |
| Table 3-1. Sequential Read / Write Performance .....                      | 9  |
| Table 3-2. Device Power Consumption .....                                 | 9  |
| Table 3-3. Partition Capacity .....                                       | 9  |
| Table 4-1. Communication Interface .....                                  | 11 |
| Table 4-2. e.MMC Register .....                                           | 12 |
| Table 4-3. e.MMC Bus Mode .....                                           | 12 |
| Table 5-1. H/W Reset Timing Parameters .....                              | 15 |
| Table 6-1. OCR Register Setting .....                                     | 17 |
| Table 6-2. CID Register Setting .....                                     | 18 |
| Table 6-3. CSD Register Setting .....                                     | 19 |
| Table 6-4. Extended CSD Register Setting .....                            | 20 |
| Table 7-1. General Operating Conditions .....                             | 28 |
| Table 7-2. Operating Voltage .....                                        | 29 |
| Table 7-3. Voltage Combinations .....                                     | 29 |
| Table 7-4. Signal Line Load .....                                         | 30 |
| Table 7-5. Open-drain Bus Signal Level .....                              | 32 |
| Table 7-6. Push-pull Signal Level — High-voltage e.MMC .....              | 33 |
| Table 7-7. Push-pull Signal Level — 1.7V ~ 1.95V VCCQ Voltage Range ..... | 33 |
| Table 7-8. High-speed Device Interface Timing .....                       | 35 |
| Table 7-9. Backward-compatible Device Interface Timing .....              | 36 |
| Table 7-10. High-speed Dual Data Rate Interface Timing .....              | 38 |
| Table 7-11. HS400 Device input timing .....                               | 39 |
| Table 7-12. HS400 Device output timing .....                              | 40 |
| Table 7-13. HS400 Capacitance and Resistors .....                         | 41 |
| Table 8-1. FBGA (11.5 x 13 x 1.0mm) Dimension Table .....                 | 42 |

## 1 Introduction

The e.MMC products follow the JEDEC e.MMC 5.1 standards. It is an ideal universal storage solution for many electronic devices, including smart phones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. e.MMC encloses the TLC NAND and e.MMC controller inside as one JEDEC standard package, providing a standard interface to the host. The e.MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

### 1.1 Product Features

- **Packaged NAND flash memory with e.MMC 5.1 interface**
- **Backward compatible with all prior e.MMC specification revisions**
- **Operating Voltage Support:**
  - $V_{CC}$ : (3.3V) 2.7V ~ 3.6V
  - $V_{CCQ}$ : (1.8V) 1.7V ~ 1.95V / (3.3V) 2.7V ~ 3.6V
- **Temperature:**
  - Operating Temperature: TA = -25°C to +85°C
  - Storage without operation: -40°C to +85°C
- **Compliant with e.MMC 5.1 JEDEC Standard Number JESD84-B51**
- **Embedded Multi-Media storage in a single Multi-Chip package.**
- **Package: 153-ball 11.5 x 13.0 x 1.0mm FBGA package**

Table 1-1. Product Information

| Part Number    | NAND Density | $V_{CC}$ | $V_{CCQ}$ | Package |
|----------------|--------------|----------|-----------|---------|
| EM74J08LVAGC-H | 16 GB        | 3.3V     | 1.8V/3.3V | FBGA    |

## 1.2 e.MMC Specific Feature

- **Bus modes:**
  - High-speed e.MMC protocol
  - Clock frequency : 0-200MHz
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset
- **Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits**
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate : up to 200Mbyte/s @ 200MHz
  - Dual data rate : up to 400Mbyte/s @ 200MHz
- **Error free memory access**
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- **Security**
  - Support secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options
- **Quality**
  - TSCA, RoHS and HF compliant
- **Field firmware update (FFU)**
- **Enhanced Device Life time**
- **Support Pre EOL information**
- **Optimal Size**
- **Supports Production State Awareness**
- **Supports Power Off Notification for Sleep**
- **Supports HS400**

## 2 Ball Assignment

### 2.1 Package Configuration

|   | 1  | 2    | 3    | 4    | 5     | 6    | 7   | 8   | 9   | 10  | 11 | 12 | 13 | 14 |
|---|----|------|------|------|-------|------|-----|-----|-----|-----|----|----|----|----|
| A | NC | NC   | DAT0 | DAT1 | DAT2  | VSS  | NC  | NC  | NC  | NC  | NC | NC | NC | NC |
| B | NC | DAT3 | DAT4 | DAT5 | DAT6  | DAT7 | NC  | NC  | NC  | NC  | NC | NC | NC | NC |
| C | NC | VDDi | NC   | VSSQ | NC    | VCCQ | NC  | NC  | NC  | NC  | NC | NC | NC | NC |
| D | NC | NC   | NC   | NC   |       |      |     |     |     |     |    | NC | NC | NC |
| E | NC | NC   | NC   |      | NC    | VCC  | VSS | RFU | RFU | RFU |    | NC | NC | NC |
| F | NC | NC   | NC   |      | VCC   |      |     |     |     | RFU |    | NC | NC | NC |
| G | NC | NC   | NC   |      | VSS   |      |     |     |     | RFU |    | NC | NC | NC |
| H | NC | NC   | NC   |      | DS    |      |     |     |     | VSS |    | NC | NC | NC |
| J | NC | NC   | NC   |      | VSS   |      |     |     |     | VCC |    | NC | NC | NC |
| K | NC | NC   | NC   |      | RST_n | NC   | NC  | VSS | VCC | RFU |    | NC | NC | NC |
| L | NC | NC   | NC   |      |       |      |     |     |     |     |    | NC | NC | NC |
| M | NC | NC   | NC   | VCCQ | CMD   | CLK  | NC  | NC  | NC  | NC  | NC | NC | NC | NC |
| N | NC | VSSQ | NC   | VCCQ | VSSQ  | NC   | NC  | NC  | NC  | NC  | NC | NC | NC | NC |
| P | NC | NC   | VCCQ | VSSQ | VCCQ  | VSSQ | NC  | NC  | NC  | RFU | NC | NC | NC | NC |

Figure 2-1. 153-FBGA Ball Assignment (Top View)



## 3 Specification

### 3.1 System Performance

The following table provides sequential read and write speeds for all capacities. Performance numbers may vary under different operating conditions.

**Table 3-1. Sequential Read / Write Performance**

| Product        | Typical value (MB/s) |                  |
|----------------|----------------------|------------------|
|                | Read Sequential      | Write Sequential |
| EM74J08LVAGC-H | 315                  | 195              |

Note 1: Performance numbers might be subject to changes without notice.

### 3.2 Power Consumption

The device current consumption for various device configurations is defined in the power level field of the EXT\_CSD register. The table below summarizes the power consumption values.

**Table 3-2. Device Power Consumption**

| Product        | Read(mA)   |           | Write(mA)  |           | Standby(mA) |           |
|----------------|------------|-----------|------------|-----------|-------------|-----------|
|                | VCCQ(1.8V) | VCC(3.3V) | VCCQ(1.8V) | VCC(3.3V) | VCCQ(1.8V)  | VCC(3.3V) |
| EM74J08LVAGC-H | 160        | 90        | 70         | 60        | 0.1         | 0.05      |

Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, VCC= 3.3V±5%, VCCQ=1.8V±5%.

Note 2: Standby current is measured at VCC=3.3V±5%, 8-bit bus width without clock frequency.

Note 3: Current numbers might be subject to changes without notice.

Note 4: The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.

### 3.3 Partition Capacity

Total user density depends on device type.

For example, 52MB in the SLC mode requires 156 MB in TLC. This results in decreasing.

**Table 3-3. Partition Capacity**

| User density         | Boot partition 1 | Boot partition 2 | RPMB    |
|----------------------|------------------|------------------|---------|
| 15,724,707,840 Bytes | 4096 KB          | 4096 KB          | 4096 KB |

## 4 e.MMC Device and System

### 4.1 e.MMC System Overview

The e.MMC specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

The NAND Device consists of a single chip MMC controller and NAND flash memory module. The microcontroller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

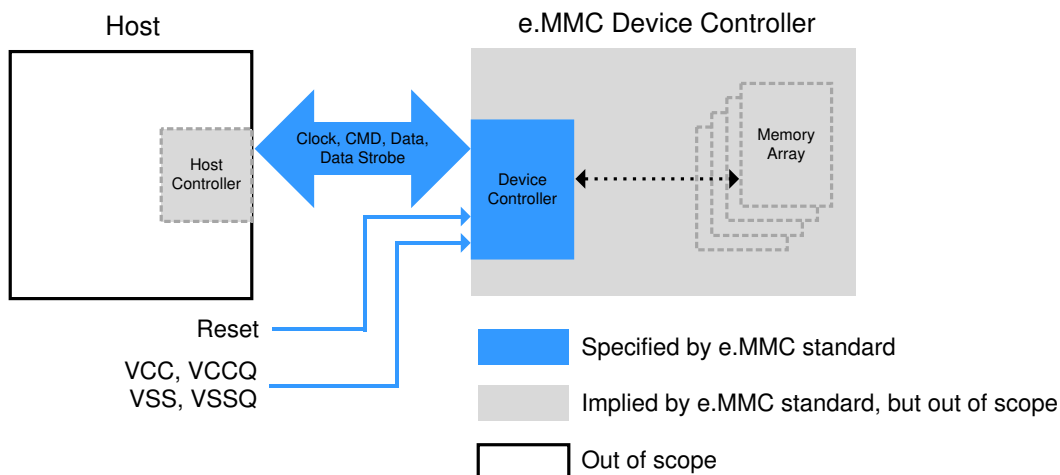


Figure 4-1. e.MMC System Overview

### 4.2 Memory Addressing

Previous implementations of the e.MMC specification are following byte addressing with 32 bit field. This addressing mechanism permitted for e.MMC densities up to and including 2 GB.

To support larger densities, the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register.

## 4.3 e.MMC Device Overview

The e.MMC device transfers data via a configurable number of data bus signals. The communication signals are:

**Table 4-1. Communication Interface**

| Name                                                                                  | Type      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------------------------------------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK                                                                                   | I         | <b>Clock:</b> Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| DAT[7:0]                                                                              | I/O/PP    | <b>Data:</b> These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0- DAT7, by the e.MMC host controller. The e.MMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1-DAT7. |
| CMD                                                                                   | I/O/PP/OD | <b>Command:</b> This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e.MMC host controller to the e.MMC device and responses are sent from the device to the host.                                                                                                                                                                                                                                                                                                                           |
| RST_n                                                                                 | I         | <b>Hardware Reset:</b> By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| VCC                                                                                   | S         | Supply voltage for core                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VCCQ                                                                                  | S         | Supply voltage for I/O                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| VSS                                                                                   | S         | Supply ground for core                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| VSSQ                                                                                  | S         | Supply ground for I/O                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DS                                                                                    | O/PP      | <b>Data Strobe:</b> This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.                                                                                                                                                                                       |
| RFU                                                                                   | -         | Reserved for future use: These pins are not internally connected. Leave floating                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| NC                                                                                    | -         | Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDDi                                                                                  | -         | Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Note: I=Input; O=Output; P=Push-Pull; OD=Open Drain; NC=Not Connected; S=Power Supply |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 4-2. e.MMC Register**

| Name    | Width (Bytes) | Description                                                                                                                       | Implementation |
|---------|---------------|-----------------------------------------------------------------------------------------------------------------------------------|----------------|
| CID     | 16            | Device Identification number, an individual number for identification.                                                            | Mandatory      |
| RCA     | 2             | Relative Device Address is the Device system address, dynamically assigned by the host during initialization.                     | Mandatory      |
| DSR     | 2             | Driver Stage Register, to configure the Device's output drivers.                                                                  | Optional       |
| CSD     | 16            | Device Specific Data, information about the Device operation conditions.                                                          | Mandatory      |
| OCR     | 4             | Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.                    | Mandatory      |
| EXT_CSD | 512           | Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0 | Mandatory      |

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

## 4.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based e.MMC bus protocol. For more details, refer to the JEDEC Standard Specification JESD84-B51.

## 4.5 Bus Speed Modes

The e.MMC standard specifies several bus speed modes, which are detailed in the following table.

**Table 4-3. e.MMC Bus Mode**

| Mode                                         | Data Rate | IO Voltage  | Bus Width | CLK Frequency | Max Data Transfer (implies x8 bus width) |
|----------------------------------------------|-----------|-------------|-----------|---------------|------------------------------------------|
| Backwards Compatibility with legacy MMC card | Single    | 3.3V / 1.8V | 1, 4, 8   | 0 – 26 MHz    | 26 MB/s                                  |
| High Speed SDR                               | Single    | 3.3V / 1.8V | 4, 8      | 0 – 52 MHz    | 52 MB/s                                  |
| High Speed DDR                               | Dual      | 3.3V / 1.8V | 4, 8      | 0 – 52 MHz    | 104 MB/s                                 |
| HS200                                        | Single    | 1.8V        | 4, 8      | 0 – 200 MHz   | 200 MB/s                                 |
| HS400                                        | Dual      | 1.8V        | 8         | 0 – 200 MHz   | 400 MB/s                                 |



## 5 e.MMC Functional Description

### 5.1 e.MMC Overview

All communication between host and device are controlled by the host (main chip). The host sends a command, which results in a device response. For more details, refer to the JEDEC Standard Specification JESD84-B51.

Five operation modes are defined for the e.MMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

### 5.2 Boot Operation Mode

In boot operation mode, the master (e.MMC host) can read boot data from the slave (e.MMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFF, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to the JEDEC Standard Specification JESD84-B51.

### 5.3 Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative Device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to the JEDEC Standard Specification JESD84-B51.

### 5.4 Interrupt Mode

The interrupt mode on the e.MMC system enables the master (e.MMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting e.MMC interrupt mode is an option, both for the host and the Device. For more details, refer to the JEDEC Standard Specification JESD84-B51.

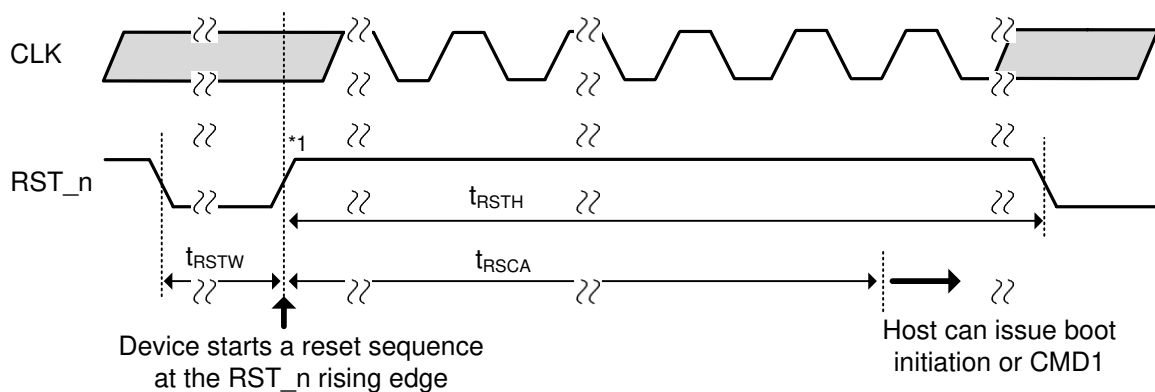
## 5.5 Data Transfer Mode

When the Device is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to the JEDEC Standard Specification JESD84-B51.

## 5.6 Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO\_INACTIVE\_STATE command (CMD15). The device will reset to Pre-idle state with power cycle. For more details, refer to the JEDEC Standard Specification JESD84-B51.

## 5.7 H/W Reset Operation



Note 1. Device will detect the rising edge of RST\_n signal to trigger internal reset sequence.

Figure 5-1. H/W Reset Waveform

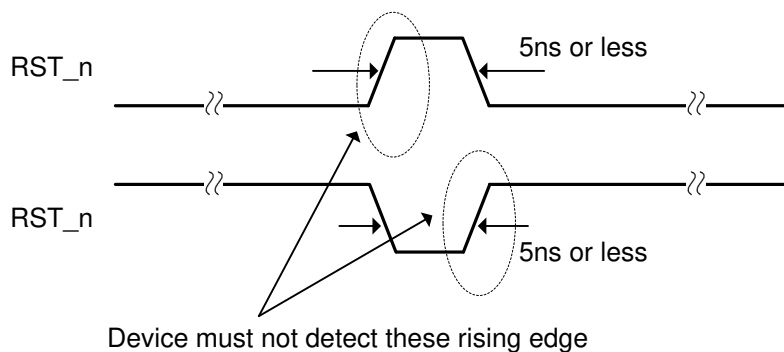
Table 5-1. H/W Reset Timing Parameters

| Symbol     | Comment                           | Min.               | Max. | Unit |
|------------|-----------------------------------|--------------------|------|------|
| $t_{RSTW}$ | RST_n pulse width                 | 1                  | -    | us   |
| $t_{RSCA}$ | RST_n to Command time             | 200 <sup>(1)</sup> | -    | us   |
| $t_{RSTH}$ | RST_n high period (interval time) | 1                  | -    | us   |

Note1: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFF

## 5.8 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity.



**Figure 5-2. Noise Filtering Timing for H/W Reset**

Device must not detect these rising edge.

Device must not detect 5ns or less of positive or negative RST\_n pulse.

Device must detect more than or equal to 1us of positive or negative RST\_n pulse width.

## 5.9 Enhanced User Data Area

This eMMC supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured as SLC Mode. Therefore when host set the Enhanced User Data Area, the area will occupy double size of original set up size. The Max Enhanced User Data Area size is defined as - (MAX\_ENH\_SIZE\_MULT x HC\_WP\_GRP\_SIZE x HC\_ERASE\_GRP\_SIZE x 512 KBytes). The Enhanced use data area size is defined as - (ENH\_SIZE\_MULT x HC\_WP\_GRP\_SIZE x HC\_ERASE\_GRP\_SIZE x 512 KBytes). The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.



## 6 Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT\_CSD, RCA and DSR. These can be accessed only by corresponding commands. For more details, refer to the JEDEC Standard Specification JESD84-B51.

### 6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the device power up procedure has been finished. The OCR register shall be implemented by all devices.

**Table 6-1. OCR Register Setting**

| OCR Register<br>Definitions OCR bit                                                 | VDD voltage window                               | High Voltage<br>Multi-Media Card     | Dual voltage<br>Multi-Media Card and e.MMC |
|-------------------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------|--------------------------------------------|
| [6:0]                                                                               | Reserved                                         | 00 00000b                            | 00 00000b                                  |
| [7]                                                                                 | 1.70 - 1.95V                                     | 0b                                   | 1b                                         |
| [14:8]                                                                              | 2.0 - 2.6V                                       | 000 0000b                            | 000 0000b                                  |
| [23:15]                                                                             | 2.7 - 3.6V                                       | 1 1111 1111b                         | 1 1111 1111b                               |
| [28:24]                                                                             | Reserved                                         | 0 0000b                              | 0 0000b                                    |
| [30:29]                                                                             | Access Mode                                      | 00b (byte mode)<br>10b (sector mode) | 00b (byte mode)<br>10b (sector mode)       |
| [31]                                                                                | (Device power up status bit (busy)) <sup>1</sup> |                                      |                                            |
| Note1 : This bit is set to LOW if the Device has not finished the power up routine. |                                                  |                                      |                                            |

## 6.2 Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the device identification phase (e.MMC protocol). For more details, refer to the JEDEC Standard Specification JESD84-B51.

**Table 6-2. CID Register Setting**

| CID Fields Name       | Field | Width | CID slice | Value                  |
|-----------------------|-------|-------|-----------|------------------------|
| Manufacturer ID       | MID   | 8     | [127:120] | D5h                    |
| Reserved              | -     | 6     | [119:114] | 0h                     |
| Device/BGA            | CBX   | 2     | [113:112] | 1h                     |
| OEM/Application ID    | OID   | 8     | [111:104] | 01h                    |
| Product name          | PNM   | 48    | [103:56]  | (534337344A4Ch) SC74JL |
| Product revision      | PRV   | 8     | [55:48]   | 51h*                   |
| Product serial number | PSN   | 32    | [47:16]   | Random by Production   |
| Manufacturing date    | MDT   | 8     | [15:8]    | month, year            |
| CRC7 checksum         | CRC   | 7     | [7:1]     | - (Note 1)             |
| not used, always "1"  | -     | 1     | [0]       | 1h                     |

Note1. The descriptions are same as e.MMC JEDEC standard.

## 6.3 Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in e.MMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For more details, refer to the JEDEC Standard Specification JESD84-B51.

**Table 6-3. CSD Register Setting**

| Name                                             | Field              | Width | CSD-slice | Value |
|--------------------------------------------------|--------------------|-------|-----------|-------|
| CSD structure                                    | CSD_STRUCTURE      | 2     | [127:126] | 3h    |
| System specification version                     | SPEC_VERS          | 4     | [125:122] | 4h    |
| Reserved                                         | -                  | 2     | [121:120] | 0h    |
| Data read access-time 1                          | TAAC               | 8     | [119:112] | 4Fh   |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC               | 8     | [111:104] | 1h    |
| Max. bus clock frequency                         | TRAN_SPEED         | 8     | [103:96]  | 32h   |
| Device command classes                           | CCC                | 12    | [95:84]   | 8F5h  |
| Max. read data block length                      | READ_BL_LEN        | 4     | [83:80]   | 9h    |
| Partial blocks for read allowed                  | READ_BL_PARTIAL    | 1     | [79:79]   | 0h    |
| Write block misalignment                         | WRITE_BLK_MISALIGN | 1     | [78:78]   | 0h    |
| Read block misalignment                          | READ_BLK_MISALIGN  | 1     | [77:77]   | 0h    |
| DSR implemented                                  | DSR_IMP            | 1     | [76:76]   | 0h    |
| Reserved                                         | -                  | 2     | [75:74]   | 0h    |
| Device size                                      | C_SIZE             | 12    | [73:62]   | FFFh  |
| Max. read current @ VDD min                      | VDD_R_CURR_MIN     | 3     | [61:59]   | 7h    |
| Max. read current @ VDD max                      | VDD_R_CURR_MAX     | 3     | [58:56]   | 7h    |
| Max. write current @ VDD min                     | VDD_W_CURR_MIN     | 3     | [55:53]   | 7h    |
| Max. write current @ VDD max                     | VDD_W_CURR_MAX     | 3     | [52:50]   | 7h    |
| Device size multiplier                           | C_SIZE_MULT        | 3     | [49:47]   | 7h    |
| Erase group size                                 | ERASE_GRP_SIZE     | 5     | [46:42]   | 1Fh   |
| Erase group size multiplier                      | ERASE_GRP_MULT     | 5     | [41:37]   | 1Fh   |
| Write protect group size                         | WP_GRP_SIZE        | 5     | [36:32]   | 0Fh   |
| Write protect group enable                       | WP_GRP_ENABLE      | 1     | [31:31]   | 1h    |
| Manufacturer default ECC                         | DEFAULT_ECC        | 2     | [30:29]   | 0h    |
| Write speed factor                               | R2W_FACTOR         | 3     | [28:26]   | 2h    |
| Max. write data block length                     | WRITE_BL_LEN       | 4     | [25:22]   | 9h    |
| Partial blocks for write allowed                 | WRITE_BL_PARTIAL   | 1     | [21:21]   | 0h    |
| Reserved                                         | -                  | 4     | [20:17]   | 0h    |
| Content protection application                   | CONTENT_PROT_APP   | 1     | [16:16]   | 0h    |
| File format group                                | FILE_FORMAT_GRP    | 1     | [15:15]   | 0h    |
| Copy flag (OTP)                                  | COPY               | 1     | [14:14]   | 0h    |
| Permanent write protection                       | PERM_WRITE_PROTECT | 1     | [13:13]   | 0h    |
| Temporary write protection                       | TMP_WRITE_PROTECT  | 1     | [12:12]   | 0h    |
| File format                                      | FILE_FORMAT        | 2     | [11:10]   | 0h    |
| ECC code                                         | ECC                | 2     | [9:8]     | 0h    |
| CRC                                              | CRC                | 7     | [7:1]     | 2Eh   |
| Not used, always '1'                             | -                  | 1     | [0:0]     | 1h    |

## 6.4 Extended Card Specific Data Register [EXT\_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For more details, refer to the JEDEC Standard Specification JESD84-B51.

**Table 6-4. Extended CSD Register Setting**

| Name                                      | Field                                     | Size (Bytes) | CSD-slice | Value     |
|-------------------------------------------|-------------------------------------------|--------------|-----------|-----------|
| Properties Segment                        |                                           |              |           |           |
| Reserved (note1)                          | —                                         | 6            | [511:506] | 0h        |
| Extended Security Commands Error          | EXT_SECURITY_ERR                          | 1            | [505]     | 0h        |
| Supported Command Sets                    | S_CMD_SET                                 | 1            | [504]     | 1h        |
| HPI features                              | HPI_FEATURES                              | 1            | [503]     | 1h        |
| Background operations support             | BKOPS_SUPPORT                             | 1            | [502]     | 1h        |
| Max packed read commands                  | MAX_PACKED_READS                          | 1            | [501]     | 3Ch       |
| Max packed write commands                 | MAX_PACKED_WRITES                         | 1            | [500]     | 20h       |
| Data Tag Support                          | DATA_TAG_SUPPORT                          | 1            | [499]     | 1h        |
| Tag Unit Size                             | TAG_UNIT_SIZE                             | 1            | [498]     | 3h        |
| Tag Resources Size                        | TAG_RES_SIZE                              | 1            | [497]     | 0h        |
| Context management capabilities           | CONTEXT_CAPABILITIES                      | 1            | [496]     | 5h        |
| Large Unit size                           | LARGE_UNIT_SIZE_M1                        | 1            | [495]     | 5Fh       |
| Extended partitions attribute support     | EXT_SUPPORT                               | 1            | [494]     | 3h        |
| Supported modes                           | SUPPORTED_MODES                           | 1            | [493]     | 1h        |
| FFU features                              | FFU_FEATURES                              | 1            | [492]     | 0h        |
| Operation codes timeout                   | OPERATION_CODE_TIME_OUT                   | 1            | [491]     | 0h        |
| FFU Argument                              | FFU_ARG                                   | 4            | [490:487] | 65535     |
| Barrier support                           | BARRIER_SUPPORT                           | 1            | [486:486] | 1h        |
| Reserved                                  | Reserved                                  | 177          | [485:309] | -         |
| CMD Queuing Support                       | CMQ_SUPPORT                               | 1            | [308:308] | 1h        |
| CMD Queuing Depth                         | CMQ_DEPTH                                 | 1            | [307:307] | 1Fh       |
| Reserved                                  | Reserved                                  | 1            | [306:306] | -         |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4            | [305:302] | 0h        |
| Vendor proprietary health report          | VENDOR_PROPRIETARY_HEALTH_REPORT          | 32           | [301:270] | -         |
| Device life time estimation type B        | DEVICE_LIFE_TIME_EST_TYP_B                | 1            | [269]     | 1h        |
| Device life time estimation type A        | DEVICE_LIFE_TIME_EST_TYP_A                | 1            | [268]     | 1h        |
| Pre EOL information                       | PRE_EOL_INFO                              | 1            | [267]     | 1h        |
| Optimal read size                         | OPTIMAL_READ_SIZE                         | 1            | [266]     | 1h        |
| Optimal write size                        | OPTIMAL_WRITE_SIZE                        | 1            | [265]     | 8h        |
| Optimal trim unit size                    | OPTIMAL_TRIM_UNIT_SIZE                    | 1            | [264]     | 1h        |
| Device version                            | DEVICE_VERSION                            | 2            | [263:262] | 0h        |
| Firmware version                          | FIRMWARE_VERSION                          | 8            | [261:254] | (note5) * |
| Power class for 200MHz, DDR at VCC=3.6V   | PWR_CL_DDR_200_360                        | 1            | [253]     | 0h        |
| Cache size                                | CACHE_SIZE                                | 4            | [252:249] | 1536      |
| Generic CMD6 timeout                      | GENERIC_CMD6_TIME                         | 1            | [248]     | 32h       |

|                                                                |                                    |   |           |          |
|----------------------------------------------------------------|------------------------------------|---|-----------|----------|
| Power off notification(long) time out                          | POWER_OFF_LONG_TIME                | 1 | [247]     | FFh      |
| Background operations status                                   | BKOPS_STATUS                       | 1 | [246]     | 0h       |
| Number of correctly programmed sectors                         | CORRECTLY_PRG_SECTORS_NUM          | 4 | [245:242] | 0h       |
| 1st initialization time after partitioning                     | INI_TIMEOUT_AP                     | 1 | [241]     | 64h      |
| Cache Flushing Policy                                          | CACHE_FLUSH_POLICY                 | 1 | [240]     | 1h       |
| Power class for 52MHz, DDR at 3.6V                             | PWR_CL_DDR_52_360                  | 1 | [239]     | 0h       |
| Power class for 52MHz, DDR at 1.95V                            | PWR_CL_DDR_52_195                  | 1 | [238]     | 0h       |
| Power class for 200MHz at 3.6V                                 | PWR_CL_200_360                     | 1 | [237]     | 0h       |
| Power class for 200MHz, at 1.95V                               | PWR_CL_200_195                     | 1 | [236]     | 0h       |
| Minimum Write Performance for 8bit at 52MHz in DDR mode        | MIN_PERF_DDR_W_8_52                | 1 | [235]     | 0h       |
| Minimum Read Performance for 8bit at 52MHz in DDR mode         | MIN_PERF_DDR_R_8_52                | 1 | [234]     | 0h       |
| Reserved (note1)                                               | -                                  | 1 | [233]     | -        |
| TRIM Multiplier                                                | TRIM_MULT                          | 1 | [232]     | 05h      |
| Secure Feature support                                         | SEC_FEATURE_SUPPORT                | 1 | [231]     | 55h      |
| Secure Erase Multiplier                                        | SEC_ERASE_MULT                     | 1 | [230]     | F7h      |
| Secure TRIM Multiplier                                         | SEC_TRIM_MULT                      | 1 | [229]     | F7h      |
| Boot information                                               | BOOT_INFO                          | 1 | [228]     | 7h       |
| Reserved (note1)                                               | -                                  | 1 | [227]     | -        |
| Boot partition size                                            | BOOT_SIZE_MULT                     | 1 | [226]     | 20h      |
| Access size                                                    | ACC_SIZE                           | 1 | [225]     | 8h       |
| High-capacity erase unit size                                  | HC_ERASE_GRP_SIZE                  | 1 | [224]     | 1h       |
| High-capacity erase timeout                                    | ERASE_TIMEOUT_MULT                 | 1 | [223]     | 11h      |
| Reliable write sector count                                    | REL_WR_SEC_C                       | 1 | [222]     | 1h       |
| High-capacity write protect group size                         | HC_WP_GRP_SIZE                     | 1 | [221]     | 10h      |
| Sleep current (VCC)                                            | S_C_VCC                            | 1 | [220]     | 8h       |
| Sleep current (VCCQ)                                           | S_C_VCCQ                           | 1 | [219]     | 8h       |
| Production state awareness Timeout                             | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | [218]     | 14h      |
| Sleep/awake timeout                                            | S_A_TIMEOUT                        | 1 | [217]     | 15h      |
| Sleep Notification time out                                    | SLEEP_NOTIFICATION_TIME            | 1 | [216]     | 0Fh      |
| Sector Count                                                   | SEC_COUNT                          | 4 | [215:212] | 1D4A200h |
| Reserved (note1)                                               | -                                  | 1 | [211]     | 01h      |
| Minimum Write Performance for 8bit at 52MHz                    | MIN_PERF_W_8_52                    | 1 | [210]     | 8h       |
| Minimum Read Performance for 8bit at 52MHz                     | MIN_PERF_R_8_52                    | 1 | [209]     | 8h       |
| Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52               | 1 | [208]     | 8h       |
| Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz  | MIN_PERF_R_8_26_4_52               | 1 | [207]     | 8h       |
| Minimum Write Performance for 4bit at 26MHz                    | MIN_PERF_W_4_26                    | 1 | [206]     | 8h       |
| Minimum Read Performance for 4bit at 26MHz                     | MIN_PERF_R_4_26                    | 1 | [205]     | 8h       |
| Reserved (note1)                                               | -                                  | 1 | [204]     | -        |
| Power class for 26MHz at 3.6V 1 R                              | PWR_CL_26_360                      | 1 | [203]     | 0h       |
| Power class for 52MHz at 3.6V 1 R                              | PWR_CL_52_360                      | 1 | [202]     | 0h       |
| Power class for 26MHz at 1.95V 1 R                             | PWR_CL_26_195                      | 1 | [201]     | 0h       |
| Power class for 52MHz at 1.95V 1 R                             | PWR_CL_52_195                      | 1 | [200]     | 0h       |
| Partition switching timing                                     | PARTITION_SWITCH_TIME              | 1 | [199]     | FFh      |
| Out-of-interrupt busy timing                                   | OUT_OF_INTERRUPT_TIME              | 1 | [198]     | FFh      |

|                                        |                             |   |           |             |
|----------------------------------------|-----------------------------|---|-----------|-------------|
| I/O Driver Strength                    | DRIVER_STRENGTH             | 1 | [197]     | 1Fh         |
| Device type                            | CARD_TYPE                   | 1 | [196]     | 57h         |
| Reserved (note1)                       | -                           | 1 | [195]     | -           |
| CSD structure version                  | CSD_STRUCTURE               | 1 | [194]     | 2h          |
| Reserved (note1)                       | -                           | 1 | [193]     | -           |
| Extended CSD revision                  | EXT_CSD_REV                 | 1 | [192]     | 08h         |
| <b>Modes Segment</b>                   |                             |   |           |             |
| Command set                            | CMD_SET                     | 1 | [191]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [190]     | -           |
| Command set revision                   | CMD_SET_REV                 | 1 | [189]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [188]     | -           |
| Power class                            | POWER_CLASS                 | 1 | [187]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [186]     | -           |
| High-speed interface timing            | HS_TIMING                   | 1 | [185]     | 1h (note 3) |
| Strobe Support                         | STROBE_SUPPORT              | 1 | [184]     | 1h          |
| Bus width mode                         | BUS_WIDTH                   | 1 | [183]     | 2h (note 4) |
| Reserved (note1)                       | -                           | 1 | [182]     | -           |
| Erased memory content                  | ERASED_MEM_CONT             | 1 | [181]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [180]     | -           |
| Partition configuration                | PARTITION_CONFIG            | 1 | [179]     | 0h          |
| Boot config protection                 | BOOT_CONFIG_PROT            | 1 | [178]     | 0h          |
| Boot bus Conditions                    | BOOT_BUS_CONDITIONS         | 1 | [177]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [176]     | -           |
| High-density erase group definition    | ERASE_GROUP_DEF             | 1 | [175]     | 0h          |
| Boot write protection status registers | BOOT_WP_STATUS              | 1 | [174]     | 0h          |
| Boot area write protection register    | BOOT_WP                     | 1 | [173]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [172]     | -           |
| User area write protection register    | USER_WP                     | 1 | [171]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [170]     | 1Eh         |
| FW configuration                       | FW_CONFIG                   | 1 | [169]     | 0h          |
| RPMB Size                              | RPMB_SIZE_MULT              |   | [168]     | 20h*        |
| Write reliability setting register     | WR_REL_SET                  |   | [167]     | 1Fh         |
| Write reliability parameter register   | WR_REL_PARAM                | 1 | [166]     | 15h         |
| Start Sanitize operation               | SANITIZE_START              | 1 | [165]     | 0h          |
| Manually start background operation    | BKOPS_START                 | 1 | [164]     | 0h          |
| Enable background operations handshake | BKOPS_EN                    | 1 | [163]     | 0h          |
| H/W reset function                     | RST_n_FUNCTION              | 1 | [162]     | 0h          |
| HPI management                         | HPI_MGMT                    | 1 | [161]     | 0h          |
| Partitioning Support                   | PARTITIONING_SUPPORT        | 1 | [160]     | 7h          |
| Max Enhanced Area Size                 | MAX_ENH_SIZE_MULT           | 3 | [159:157] | 624         |
| Partitions attribute                   | PARTITIONS_ATTRIBUTE        | 1 | [156]     | 0h          |
| Partitioning Setting                   | PARTITION_SETTING_COMPLETED | 1 | [155]     | 0h          |
| General Purpose Partition Size         | GP_SIZE_MULT 4              | 3 | [154:152] | 0h          |
| General Purpose Partition Size         | GP_SIZE_MULT3               | 3 | [151:149] | 0h          |
| General Purpose Partition Size         | GP_SIZE_MULT2               | 3 | [148:146] | 0h          |
| General Purpose Partition Size         | GP_SIZE_MULT1               | 3 | [145:143] | 0h          |
| Enhanced User Data Area Size           | ENH_SIZE_MULT               | 3 | [142:140] | 0h          |
| Enhanced User Data Start Address       | ENH_START_ADDR              | 4 | [139:136] | 0h          |
| Reserved (note1)                       | -                           | 1 | [135]     | -           |
| Bad Block Management mode              | SEC_BAD_BLK_MGMNT           | 1 | [134]     | 0h          |
| Reserved (note1)                       | -                           | 1 | [133]     | -           |
| Package Case Temperature is controlled | TCASE_SUPPORT               | 1 | [132]     | 0h          |

|                                                          |                                    |    |           |         |
|----------------------------------------------------------|------------------------------------|----|-----------|---------|
| Periodic Wake-up                                         | PERIODIC_WAKEUP                    | 1  | [131]     | 0h      |
| Program CID/CSD in DDR mode support                      | PROGRAM_CID_CSD_DDR_SUPPORT        | 1  | [130]     | 1h      |
| Reserved (note1)                                         | -                                  | 2  | [129:128] | -       |
| Vendor Specific Fields                                   | VENDOR_SPECIFIC_FIELD              | 64 | [127:64]  | -       |
| Native sector size                                       | NATIVE_SECTOR_SIZE                 | 1  | [63]      | 0h      |
| Sector size emulation                                    | USE_NATIVE_SECTOR                  | 1  | [62]      | 0h      |
| Sector size                                              | DATA_SECTOR_SIZE                   | 1  | [61]      | 0h      |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU                    | 1  | [60]      | 0h      |
| Class 6 commands control                                 | CLASS_6_CTRL                       | 1  | [59]      | 0h      |
| Number of addressed group to be Released                 | DYNCAP_NEEDED                      | 1  | [58]      | 0h      |
| Exception events control                                 | EXCEPTION_EVENTS_CTRL              | 2  | [57:56]   | 0h      |
| Exception events status                                  | EXCEPTION_EVENTS_STATUS            | 2  | [55:54]   | 0h      |
| Extended Partitions Attribute                            | EXT_PARTITIONS_ATTRIBUTE           | 2  | [53:52]   | 0h      |
| Context configuration                                    | CONTEXT_CONF                       | 15 | [51:37]   | 0h      |
| Packed command status                                    | PACKED_COMMAND_STATUS              | 1  | [36]      | 0h      |
| Packed command failure index                             | PACKED_FAILURE_INDEX               | 1  | [35]      | 0h      |
| Power Off Notification                                   | POWER_OFF_NOTIFICATION             | 1  | [34]      | 0h      |
| Control to turn the Cache ON/OFF                         | CACHE_CTRL                         | 1  | [33]      | 0h      |
| Flushing of the cache                                    | FLUSH_CACHE                        | 1  | [32]      | 0h      |
| Reserved (note1)                                         | Reserved                           | 1  | [31]      | -       |
| Mode config                                              | MODE_CONFIG                        | 1  | [30:30]   | 0h      |
| Mode operation codes                                     | MODE_OPERATION_CODES               | 1  | [29:29]   | 0h      |
| Reserved (note1)                                         | Reserved                           | 2  | [28:27]   | -       |
| FFU status                                               | FFU_STATUS                         | 1  | [26:26]   | 0h      |
| Per loading data size                                    | PRE_LOADING_DATA_SIZE              | 4  | [25:22]   | 0h      |
| Max pre loading data size                                | MAX_PRE_LOADING_DATA_SIZE          | 4  | [21:18]   | 972C00h |
| Product state awareness enablement                       | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1  | [17:17]   | 01h     |
| Secure removal type                                      | SECURE_REMOVAL_TYPE                | 1  | [16:16]   | 39h     |
| Command Queue Mode enable                                | CMQ_MODE_EN                        | 1  | [15:15]   | 0h      |
| Reserved (note1)                                         | Reserved                           | 15 | [14:0]    | -       |

Note 1. Reserved bits should read as "0."

Note 2. Obsolete values should be don't care.

Note 3. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing. If the host sets value 2 the Device changes its timing to HS200 interface timing, If the host sets HS\_TIMING[3:0] to 0x3, the device changes its timing to HS400 interface timing. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Note 4. It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.

Note 5. \* Changed by Firmware release note.

## **6.5 RCA Register**

The writable 16-bit relative Device address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed Host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

## **6.6 DSR Register**

The 16-bit driver-level registers (DSR) are defined in the JEDEC standard JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage.



## 7 e.MMC bus

The e.MMC bus has ten communication lines and three supply lines:

- CMD: Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DAT0~7: Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode.
- CLK: Clock is a host to Device signal. CLK operates in push-pull mode.
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

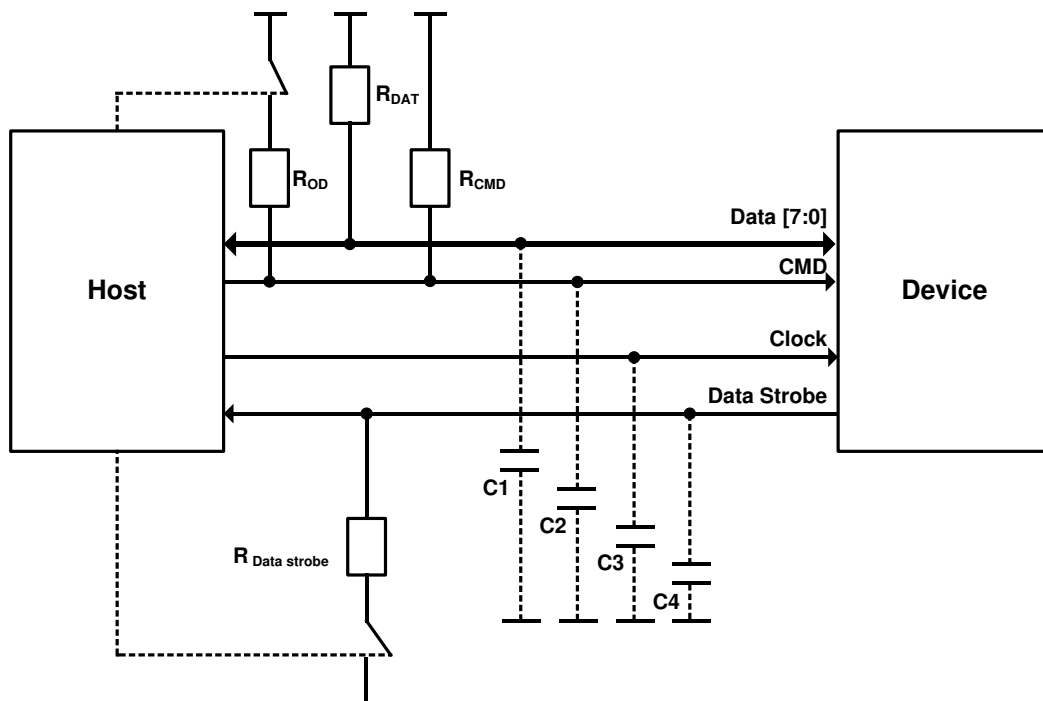


Figure 7-1. Bus Circuitry Diagram

The  $R_{OD}$  is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the  $R_{OD}$ .  $R_{DAT}$  and  $R_{CMD}$  are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the  $R_{OD}$  by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable  $R_{OD}$  implementation, a fixed  $R_{CMD}$  can be used. Consequently, the maximum operating frequency in the open drain mode has to be reduced if the used  $R_{CMD}$  value is higher than the minimal one given in.

$R_{Data\ strobe}$  is pull-down resistor used in HS400 device.

## 7.1 Power-up

### 7.1.1 e.MMC Power-up

An e.MMC bus power-up is handled locally in each device and in the bus master. The diagram below illustrates the power-up sequence, which is subsequently described in detail. For comprehensive guidelines, refer to the JEDEC standard JESD84-B51.

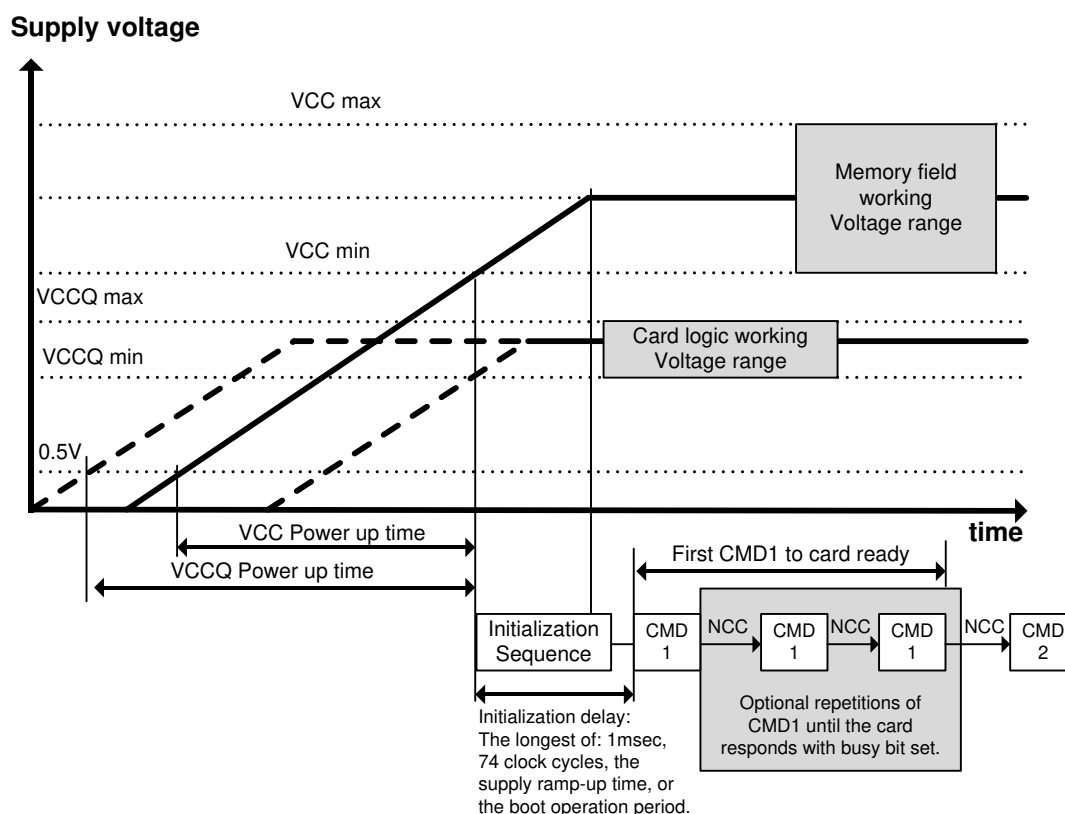


Figure 7-2. Power-up Diagram

## 7.1.2 e.MMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP\_AWAKE) to wake the slave unit. For more information on power cycling, refer to the JEDEC Standard Specification JESD84-B51.

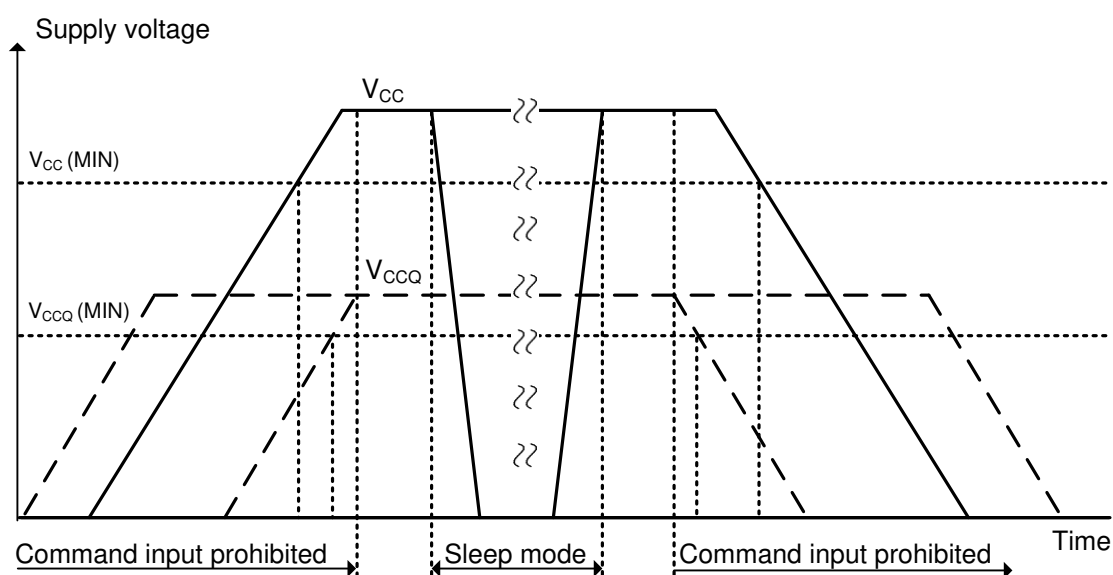


Figure 7-3. e.MMC Power Cycle

## 7.1.3 Power Cycle Requirement

As part of a power cycle, the host shall hold both the VCC and VCCQ voltage levels below 100mV for a minimum time of 1ms.

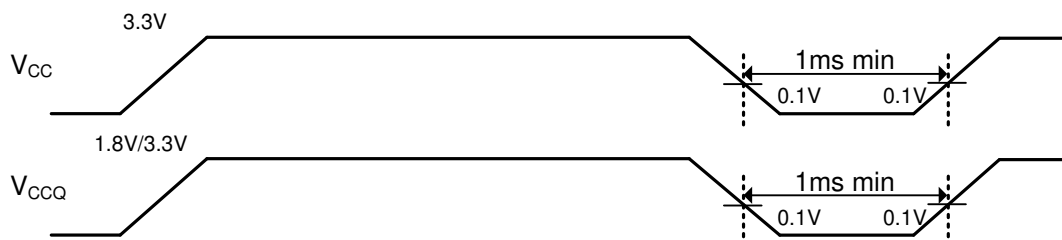


Figure 7-4. Power Cycle Requirement

## 7.2 Bus Operating Conditions

Table 7-1. General Operating Conditions

| Parameter                                                                                                           | Min  | Max        | Unit |
|---------------------------------------------------------------------------------------------------------------------|------|------------|------|
| Peak voltage on all lines                                                                                           | -0.5 | VCCQ + 0.5 | V    |
| All Inputs                                                                                                          |      |            |      |
| Input Leakage Current (before initialization sequence <sup>1</sup> and/or the internal pull up resistors connected) | -100 | 100        | μA   |
| Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)               | -2   | 2          | μA   |
| All Outputs                                                                                                         |      |            |      |
| Output Leakage Current (before initialization sequence)                                                             | -100 | 100        | μA   |
| Output Leakage Current (after initialization sequence) <sup>2</sup>                                                 | -2   | 2          | μA   |

Note 1. For detailed information on the initialization sequence, refer to the JEDEC standard specification JESD84-B51.

Note 2. DS (Data strobe) pin is excluded.

### 7.2.1 Power supply

In the e.MMC, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage as shown in the figure below. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A C<sub>REG</sub> capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

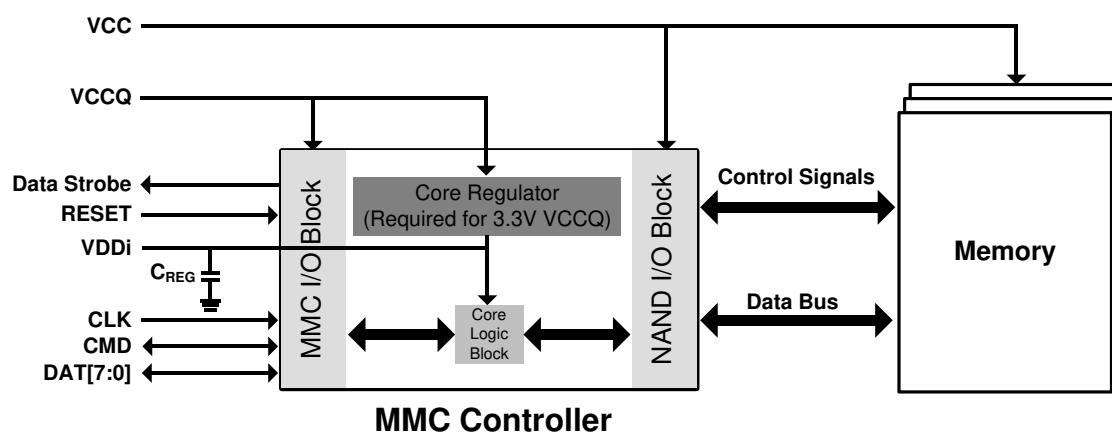


Figure 7-5. e.MMC Internal Power Diagram

## 7.2.2 Power supply Voltage

The e.MMC supports one or more combinations of VCC and VCCQ as shown in the table below. The VCCQ must be defined at equal to or less than VCC.

**Table 7-2. Operating Voltage**

| Parameter                | Symbol | Min   | Max  | Unit |
|--------------------------|--------|-------|------|------|
| Supply voltage (NAND)    | VCC    | 2.7   | 3.6  | V    |
| Supply voltage (I/O)     | VCCQ   | 2.7   | 3.6  | V    |
|                          |        | 1.7   | 1.95 | V    |
| Supply power-up for 3.3V | tPRUH  | 0.036 | 35   | ms   |
| Supply power-up for 1.8V | tPRUL  | 0.018 | 25   | ms   |

The e.MMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table).

**Table 7-3. Voltage Combinations**

| Combinations      | VCCQ         |                          |
|-------------------|--------------|--------------------------|
|                   | 1.7V ~ 1.95V | 2.7V ~ 3.6V <sup>1</sup> |
| VCC = 2.7V ~ 3.6V | Valid        | Valid                    |

Note 1.VCCQ (I/O) 3.3 volt range is not supported in HS200 & HS400 devices.

## 7.2.3 Bus Signal Line Load

The total capacitance  $C_L$  of each line of the e.MMC bus is the sum of the bus master capacitance  $C_{HOST}$ , the bus capacitance  $C_{BUS}$  itself and the capacitance  $C_{DEVICE}$  of e.MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances must be under 20pF.

**Table 7-4. Signal Line Load**

| Parameter                                | Symbol                      | Min     | Typ     | Max     | Unit       | Remark                                                                                                                                                                                                                                     |
|------------------------------------------|-----------------------------|---------|---------|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pull-up resistance for CMD               | $R_{CMD}$                   | 4.7     | 10      | 50      | k $\Omega$ | to prevent bus floating                                                                                                                                                                                                                    |
| Pull-up resistance for DAT0~7            | $R_{DAT}$                   | 10      | 10      | 50      | k $\Omega$ | to prevent bus floating                                                                                                                                                                                                                    |
| Internal pull up resistance DAT1~DAT7    | $R_{RST\_n}$                | 4.7     | 10      | 50      | k $\Omega$ | It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0b)                                                                                                  |
| Bus signal line capacitance              | CL                          | -       | 30      | 30      | pF         | Single Device                                                                                                                                                                                                                              |
| Single Device capacitance                | $C_{BGA}$                   | -       | 6       | 6       | pF         |                                                                                                                                                                                                                                            |
| Maximum signal line inductance           |                             | -       | 16      | 16      | nH         |                                                                                                                                                                                                                                            |
| Impedance on CLK / CMD / DAT0~7          |                             | 45      | 50      | 55      | $\Omega$   | Impedance match                                                                                                                                                                                                                            |
| Serial's resistance on CLK line          | $SR_{CLK}$                  | 0       | 0       | 47      | $\Omega$   |                                                                                                                                                                                                                                            |
| Serial's resistance on CMD / DAT0~7 line | $SR_{CMD}$<br>$SR_{DAT0-7}$ | 0       | 0       | 47      | $\Omega$   |                                                                                                                                                                                                                                            |
| VCCQ decoupling capacitor                |                             | 2.2+0.1 | 2.2+0.1 | 10+0.22 | $\mu F$    | It should be located as close as possible to the balls defined in order to minimize connection parasitic                                                                                                                                   |
|                                          | CH1                         | 1       | 1       | 2.2     | $\mu F$    | CH1 is for HS200 and HS400. It should be placed adjacent to VCCQ -VSSQ balls (#C6 and #C4 accordingly, next to DAT [7~0] balls). It should be located as close as possible to the balls defined in order to minimize connection parasitic. |
| VCC capacitor value                      |                             | 2.2+0.1 | 4.7+0.1 | 10+0.22 | $\mu F$    | It should be located as close as possible to the balls defined in order to minimize connection parasitic.                                                                                                                                  |
| VDDi capacitor value                     |                             | 1+0.1   | 1+0.1   | 2.2+0.1 | $\mu F$    | To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic.                                                                         |

## 7.2.4 HS400 reference load

The circuit shown below represents the reference load used to define HS400 device output timing, as well as overshoot and undershoot parameters.

The reference load is made up by the transmission line and the  $C_{\text{REFERENCE}}$  capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.

Delay time ( $t_d$ ) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

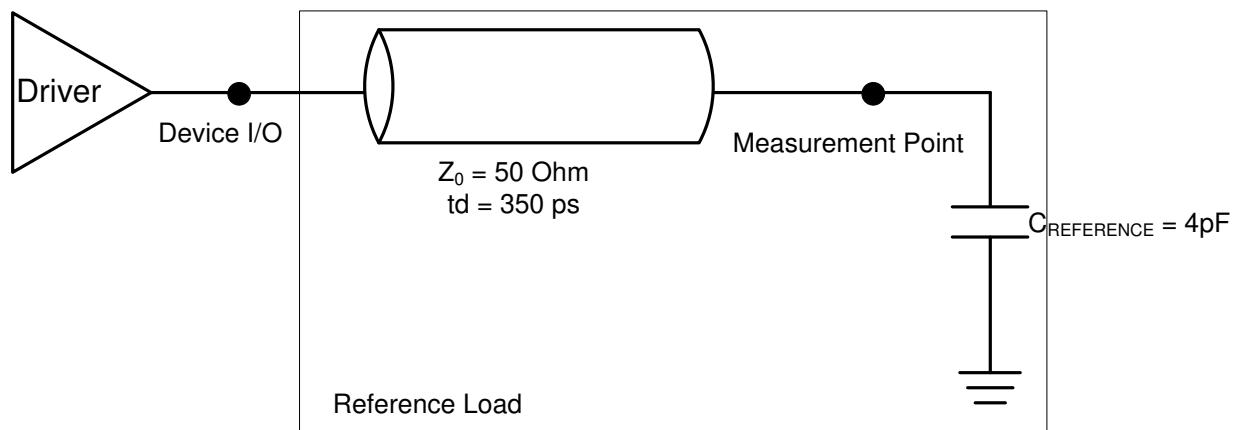


Figure 7-6. HS400 reference load

## 7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

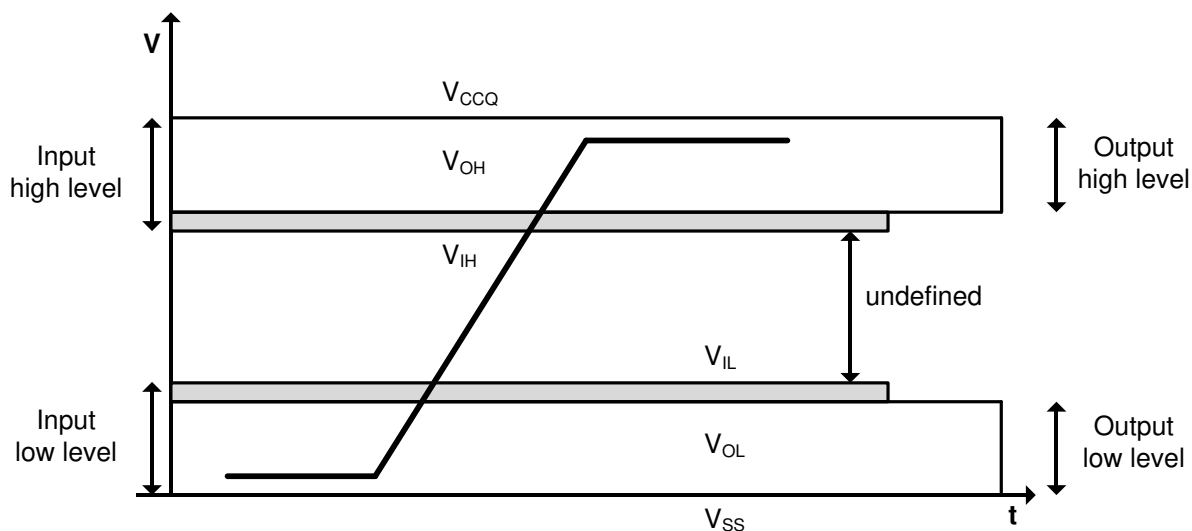


Figure 7-7. Bus Signal Levels

### 7.3.1 Open-drain Mode Bus Signal Level

Table 7-5. Open-drain Bus Signal Level

| Parameter           | Symbol | Min        | Max | Unit | Conditions         |
|---------------------|--------|------------|-----|------|--------------------|
| Output HIGH voltage | VOH    | VCCQ - 0.2 | -   | V    | IOH = -100 $\mu$ A |
| Output LOW voltage  | VOL    | -          | 0.3 | V    | IOL = 2 mA         |

Note: The input levels are identical with the push-pull mode bus signal levels.



## 7.3.2 Push-pull mode bus signal level

The device input and output voltages shall be within the following specified ranges for any VCCQ of the allowed voltage range.

For 2.7V ~ 3.6V VCCQ range (compatible with JESD8C.01)

**Table 7-6. Push-pull Signal Level — High-voltage e.MMC**

| Parameter           | Symbol | Min                 | Max                 | Unit | Conditions                    |
|---------------------|--------|---------------------|---------------------|------|-------------------------------|
| Output HIGH voltage | VOH    | $0.75 \times VCCQ$  | -                   | V    | IOH = -100 $\mu$ A @ VCCQ min |
| Output LOW voltage  | VOL    | -                   | $0.125 \times VCCQ$ | V    | IOL = 100 $\mu$ A @ VCCQ min  |
| Input HIGH voltage  | VIH    | $0.625 \times VCCQ$ | $VCCQ + 0.3$        | V    |                               |
| Input LOW voltage   | VIL    | $VSS - 0.3$         | $0.25 \times VCCQ$  | V    |                               |

For 1.7V ~ 1.95V VCCQ range (Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.)

**Table 7-7. Push-pull Signal Level — 1.7V ~ 1.95V VCCQ Voltage Range**

| Parameter           | Symbol | Min                | Max                | Unit | Conditions  |
|---------------------|--------|--------------------|--------------------|------|-------------|
| Output HIGH voltage | VOH    | $VCCQ - 0.45$      | -                  | V    | IOH = -2 mA |
| Output LOW voltage  | VOL    | -                  | 0.45               | V    | IOL = 2 mA  |
| Input HIGH voltage  | VIH    | $0.65 \times VCCQ$ | $VCCQ + 0.3$       | V    |             |
| Input LOW voltage   | VIL    | $VSS - 0.3$        | $0.35 \times VCCQ$ | V    |             |

## 7.3.3 Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices are the same as those specified in JESD84-B51, with the sole exception that VCCQ = 3.3V is not supported.

## 7.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to the JEDEC Standard Specification JESD84-B51.

## 7.4 Bus Timing

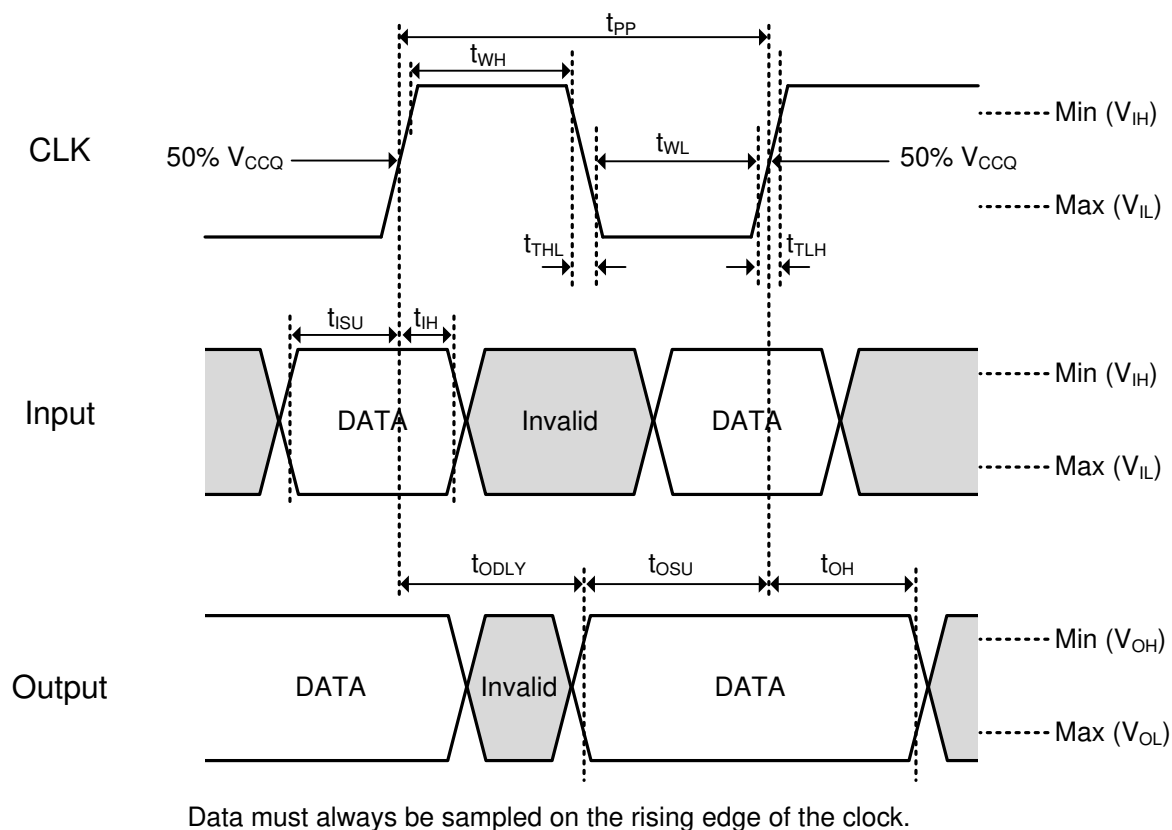


Figure 7-8. Timing Diagram

## 7.4.1 Device Interface Timings

**Table 7-8. High-speed Device Interface Timing**

| Parameter                                            | Symbol | Min | Max             | Unit | Conditions                       |
|------------------------------------------------------|--------|-----|-----------------|------|----------------------------------|
| Clock CLK <sup>1</sup>                               |        |     |                 |      |                                  |
| Clock frequency Data Transfer Mode (PP) <sup>2</sup> | fPP    | 0   | 52 <sup>3</sup> | MHz  | CL ≤ 30 pF<br>Tolerance: +100KHz |
| Clock frequency Identification Mode (OD)             | fOD    | 0   | 400             | kHz  | Tolerance: +20KHz                |
| Clock high time                                      | tWH    | 6.5 | -               | ns   | CL ≤ 30 pF                       |
| Clock low time                                       | tWL    | 6.5 | -               | ns   | CL ≤ 30 pF                       |
| Clock rise time <sup>4</sup>                         | tTLH   | -   | 3               | ns   | CL ≤ 30 pF                       |
| Clock fall time                                      | tTHL   | -   | 3               | ns   | CL ≤ 30 pF                       |
| Inputs CMD, DAT (referenced to CLK)                  |        |     |                 |      |                                  |
| Input setup time                                     | tISU   | 3   | -               | ns   | CL ≤ 30 pF                       |
| Input hold time                                      | tIH    | 3   | -               | ns   | CL ≤ 30 pF                       |
| Outputs CMD, DAT (referenced to CLK)                 |        |     |                 |      |                                  |
| Output delay time during data transfer               | tODLY  | -   | 13.7            | ns   | CL ≤ 30 pF                       |
| Output hold time                                     | tOH    | 2.5 | -               | ns   | CL ≤ 30 pF                       |
| Signal rise time <sup>5</sup>                        | tRISE  | -   | 3               | ns   | CL ≤ 30 pF                       |
| Signal fall time                                     | tFALL  | -   | 3               | ns   | CL ≤ 30 pF                       |

Note 1. CLK timing is measured at 50% of VDD.

Note 2. e.MMC shall support the full frequency range from 0-26MHz or 0-52MHz.

Note 3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.

Note 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

Note 5. Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

**Table 7-9. Backward-compatible Device Interface Timing**

| Parameter                                            | Symbol | Min  | Max | Unit | Conditions <sup>1</sup> |
|------------------------------------------------------|--------|------|-----|------|-------------------------|
| Clock CLK <sup>2</sup>                               |        |      |     |      |                         |
| Clock frequency Data Transfer Mode (PP) <sup>3</sup> | fPP    | 0    | 26  | MHz  | CL ≤ 30 pF              |
| Clock frequency Identification Mode (OD)             | fOD    | 0    | 400 | kHz  |                         |
| Clock high time                                      | tWH    | 10   | -   | ns   | CL ≤ 30 pF              |
| Clock low time                                       | tWL    | 10   | -   | ns   | CL ≤ 30 pF              |
| Clock rise time <sup>4</sup>                         | tTLH   | -    | 10  | ns   | CL ≤ 30 pF              |
| Clock fall time                                      | tTHL   | -    | 10  | ns   | CL ≤ 30 pF              |
| Inputs CMD, DAT (referenced to CLK)                  |        |      |     |      |                         |
| Input setup time                                     | tISU   | 3    | -   | ns   | CL ≤ 30 pF              |
| Input hold time                                      | tIH    | 3    | -   | ns   | CL ≤ 30 pF              |
| Outputs CMD, DAT (referenced to CLK)                 |        |      |     |      |                         |
| Output setup time <sup>5</sup>                       | tOSU   | 11.7 | -   | ns   | CL ≤ 30 pF              |
| Output hold time <sup>5</sup>                        | tOH    | 8.3  | -   | ns   | CL ≤ 30 pF              |

Note 1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high speed interface select.

Note 2. CLK timing is measured at 50% of VDD.

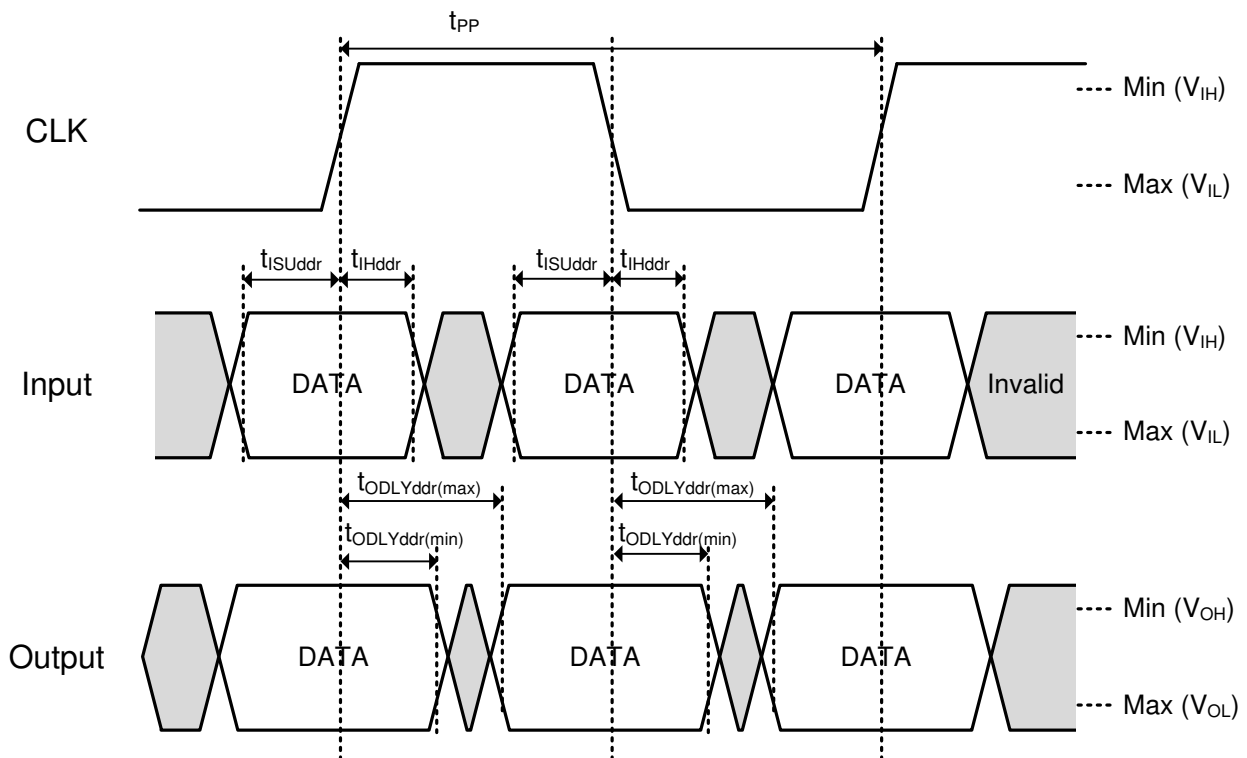
Note 3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high speed interface timing.

Note 4. CLK rise and fall times are measured by min (VIH) and max (VIL).

Note 5. tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set tWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

## 7.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal continues to operate in sync with the rising edge of CLK, in accordance with the specified bus timing, so there is no change in its timing.



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Figure 7-9. Data Input/Output in Dual Data Rate Mode

## 7.5.1 Dual Data Rate Interface Timing

**Table 7-10. High-speed Dual Data Rate Interface Timing**

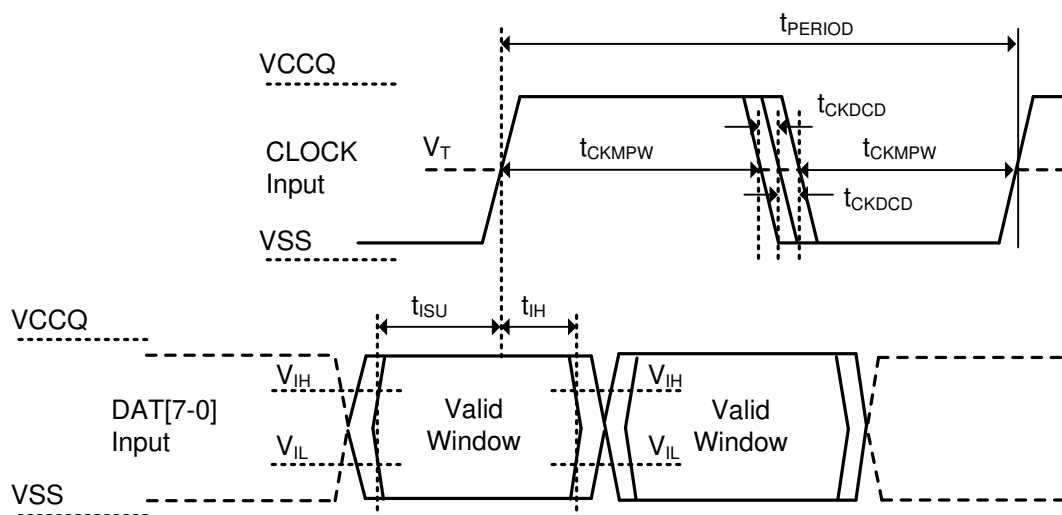
| Parameter                                   | Symbol   | Min | Max | Unit | Conditions                   |
|---------------------------------------------|----------|-----|-----|------|------------------------------|
| Clock CLK <sup>1</sup>                      |          |     |     |      |                              |
| Clock duty cycle                            |          | 45  | 55  | %    | Includes jitter, phase noise |
| Input DAT (referenced to CLK-DDR mode)      |          |     |     |      |                              |
| Input setup time                            | tISUddr  | 2.5 | -   | ns   | CL ≤ 20 pF                   |
| Input hold time                             | tIHddr   | 2.5 | -   | ns   | CL ≤ 20 pF                   |
| Output DAT (referenced to CLK-DDR mode)     |          |     |     |      |                              |
| Output delay time during data transfer      | tODLYddr | 1.5 | 7   | ns   | CL ≤ 20 pF                   |
| Signal rise time (all signals) <sup>2</sup> | tRISE    | -   | 2   | ns   | CL ≤ 20 pF                   |
| Signal fall time (all signals)              | tFALL    | -   | 2   | ns   | CL ≤ 20 pF                   |

Note 1. CLK timing is measured at 50% of VDD.

Note 2. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

## 7.6 Bus Timing Specification in HS400 mode

### 7.6.1 HS400 Device Input Timing



Note1:  $t_{ISU}$  and  $t_{IH}$  are measured at  $V_{IL}$  (max.) and  $V_{IH}$  (min.)

Note2:  $V_{IH}$  denotes  $V_{IH}$  (min.) and  $V_{IL}$  denotes  $V_{IL}$  (max.)

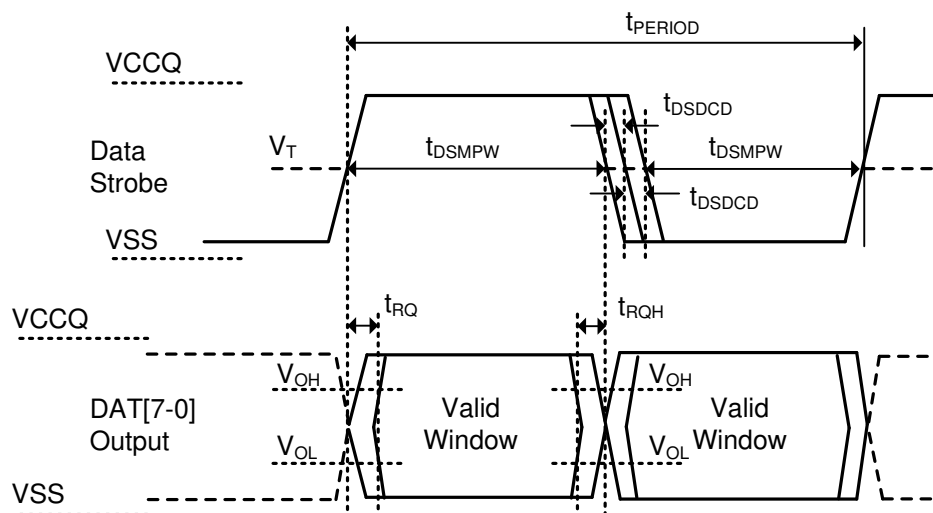
Note3:  $V_T = 50\%$  of  $V_{CCQ}$ , indicates clock reference point for timing measurements.

Figure 7-10. HS400 Device Data input timing

Table 7-11. HS400 Device input timing

| Parameter                     | Symbol       | Min   | Max | Unit | Conditions                                                                                             |
|-------------------------------|--------------|-------|-----|------|--------------------------------------------------------------------------------------------------------|
| Input CLK                     |              |       |     |      |                                                                                                        |
| Cycle time data transfer mode | $t_{PERIOD}$ | 5     | -   | ns   | 200MHz(Max), between rising edges with respect to $V_T$ .                                              |
| Slew rate                     | SR           | 1.125 | -   | V/ns | With respect to $V_{IH}/V_{IL}$ .                                                                      |
| Duty cycle distortion         | $t_{CKDCD}$  | 0.0   | 0.3 | ns   | Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$ . Includes jitter, phase noise |
| Minimum pulse width           | $t_{CKMPW}$  | 2.2   | -   | ns   | With respect to $V_T$ .                                                                                |
| Input DAT (referenced to CLK) |              |       |     |      |                                                                                                        |
| Input setup time              | $t_{ISUddr}$ | 0.4   | -   | ns   | $C_{Device} \leq 6pF$<br>With respect to $V_{IH}/V_{IL}$ .                                             |
| Input hold time               | $t_{IHddr}$  | 0.4   | -   | ns   | $C_{Device} \leq 6pF$<br>With respect to $V_{IH}/V_{IL}$ .                                             |
| Slew rate                     | SR           | 1.125 | -   | V/ns | With respect to $V_{IH}/V_{IL}$ .                                                                      |

## 7.6.2 HS400 Device Output Timing



Note1: VOH denotes VOH(min.) and VOL denotes VOL(max.)  
Note2: VT = 50% of VCCQ, indicates clock reference point for timing measurements.

Figure 7-11. HS400 Device output timing

Table 7-12. HS400 Device output timing

| Parameter                              | Symbol  | Min   | Max | Unit    | Conditions                                                                                                            |
|----------------------------------------|---------|-------|-----|---------|-----------------------------------------------------------------------------------------------------------------------|
| Data Strobe                            |         |       |     |         |                                                                                                                       |
| Cycle time data transfer mode          | tPERIOD | 5     | -   | ns      | 200MHz(Max), between rising edges with respect to VT.                                                                 |
| Slew rate                              | SR      | 1.125 | -   | V/ns    | With respect to VOH/VOL and HS400 reference load                                                                      |
| Duty cycle distortion                  | tDSDCD  | 0.0   | 0.2 | ns      | Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise |
| Minimum pulse width                    | tDSMPW  | 2.0   | -   | ns      | With respect to VT.                                                                                                   |
| Read pre-amble                         | tRPRE   | 0.4   | -   | tPERIOD | Max value is specified by manufacturer. Value up to infinite is valid                                                 |
| Read post-amble                        | tRPST   | 0.4   | -   | tPERIOD | Max value is specified by manufacturer. Value up to infinite is valid                                                 |
| Output DAT (referenced to Data Strobe) |         |       |     |         |                                                                                                                       |
| Output skew                            | tRQ     | -     | 0.4 | ns      | With respect to VOH/VOL and HS400 reference load                                                                      |
| Output hold skew                       | tRQH    | -     | 0.4 | ns      |                                                                                                                       |
| Slew rate                              | SR      | 1.125 | -   | V/ns    |                                                                                                                       |



**Table 7-13. HS400 Capacitance and Resistors**

| Parameter                             | Symbol  | Min | Max | Unit |
|---------------------------------------|---------|-----|-----|------|
| Pull-up resistance for CMD            | RCMD    | 4.7 | 50  | kΩ   |
| Pull-up resistance for DAT0-7         | RDAT    | 10  | 50  | kΩ   |
| Pull-down resistance for Data Strobe  | RDS     | 10  | 50  | kΩ   |
| Internal pull up resistance DAT1-DAT7 | Rint    | 10  | 150 | kΩ   |
| Single Device capacitance             | CDevice | -   | 6   | pF   |

## 8 Package Outline Information

Table 8-1. FBGA (11.5 x 13 x 1.0mm) Dimension Table

| Symbol | Dimension in inch |        |       | Dimension in mm |       |       |
|--------|-------------------|--------|-------|-----------------|-------|-------|
|        | Min               | Nom    | Max   | Min             | Nom   | Max   |
| A      | --                | --     | 0.039 | --              | --    | 1.0   |
| A1     | 0.006             | 0.008  | 0.010 | 0.16            | 0.21  | 0.26  |
| A2     | --                | 0.027  | --    | --              | 0.69  | --    |
| D      | 0.449             | 0.453  | 0.457 | 11.40           | 11.50 | 11.60 |
| E      | 0.508             | 0.512  | 0.516 | 12.90           | 13.00 | 13.10 |
| D1     | --                | 0.256  | --    | --              | 6.50  | --    |
| E1     | --                | 0.256  | --    | --              | 6.50  | --    |
| D2     | --                | 0.098  | --    | --              | 2.50  | --    |
| E2     | --                | 0.098  | --    | --              | 2.50  | --    |
| SD     | --                | 0.0098 | --    | --              | 0.25  | --    |
| SE     | --                | 0.0098 | --    | --              | 0.25  | --    |
| e      | --                | 0.020  | --    | --              | 0.50  | --    |
| b      | 0.010             | 0.012  | 0.014 | 0.25            | 0.30  | 0.35  |

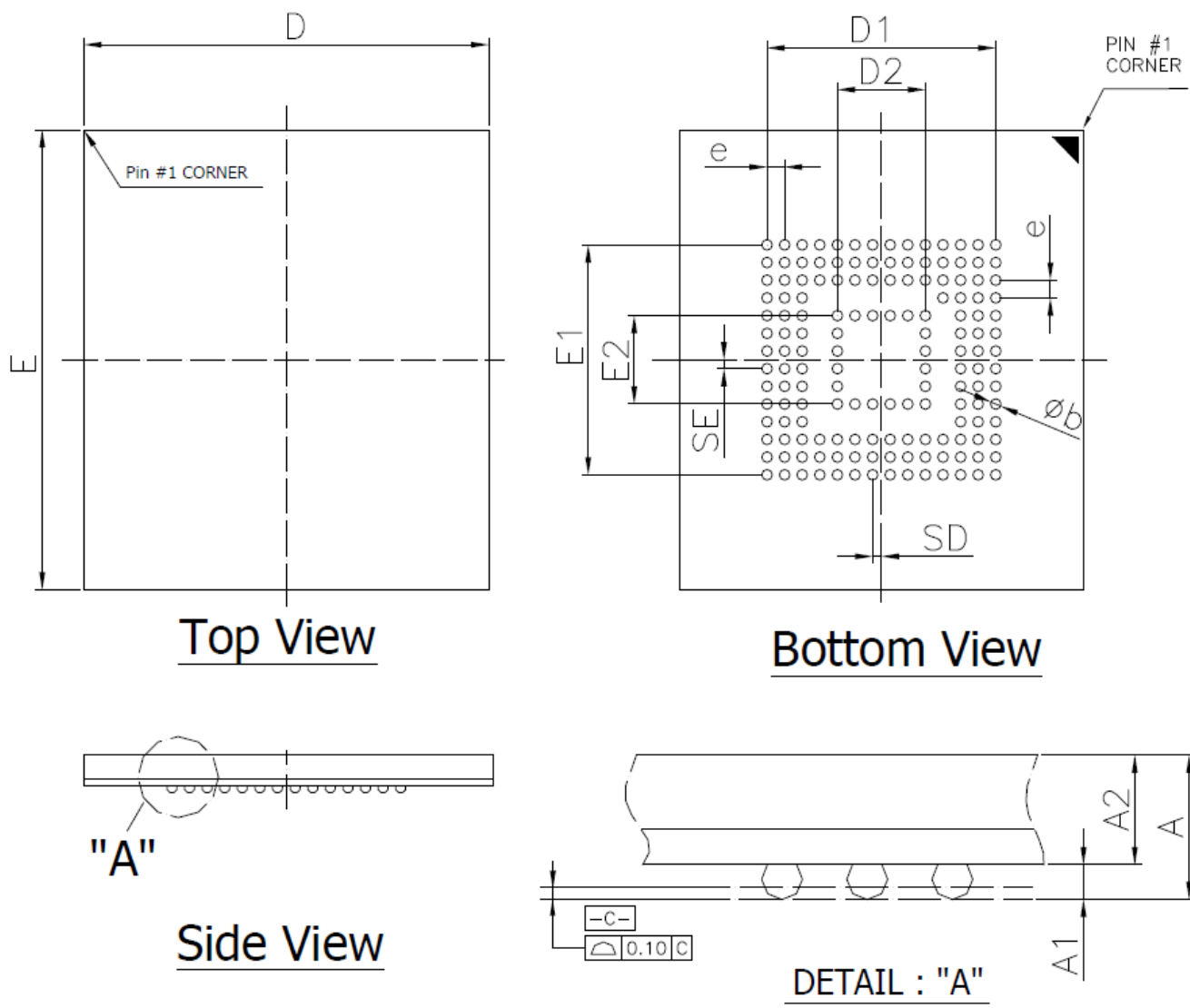


Figure 8-1. Package Outline Drawing Information