# 2Gb: x8, x16 DDR3 Synchronous DRAM (SDRAM)

**Product Preview (Rev. 1.0, Apr. /2026)**

## Features

- JEDEC Standard Compliant
- AEC-Q100 Compliant
- Standard Voltage: $V_{DD}$ & $V_{DDQ}$ = +1.5V ±0.075V
- Low Voltage: $V_{DD}$ & $V_{DDQ}$ = +1.35V (1.283V~1.45V)
  - Backward compatible to $V_{DD}$ & $V_{DDQ}$ = +1.5V ±0.075V
- Configuration: 256Mx8, 128Mx16
- Fast clock rate:
  - 1066MHz @ 2133Mbps (CL = 14)
  - 933MHz @ 1866Mbps (CL = 13)
  - 800MHz @ 1600Mbps (CL = 11)
  - 667MHz @ 1333Mbps (CL = 9)
- Operating temperature:
  - Commercial: $T_C$ = 0~95°C
  - Industrial: $T_C$ = -40~95°C
  - Automotive A3: $T_C$ = -40~95°C
  - Automotive A2: $T_C$ = -40~105°C
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- Auto Refresh and Self Refresh[1]
- Average refresh period
  - 8192 cycles/64ms (7.8us for $T_C \leqq 85°C$)
  - 8192 cycles/32ms (3.9us for $85°C < T_C \leqq 95°C$)
  - 8192 cycles/16ms (1.95us for $95°C < T_C \leqq 105°C$)
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- RoHS compliant
- Package: Pb Free and Halogen Free
  - 78-ball 7.5 x 10.5 x 1.0mm FBGA for x8
  - 96-ball 7.5 x 13 x 1.0mm FBGA for x16

Note 1. Not Support self refresh function with $T_C > 95°C$

## Table 1. Speed Grade Information

| Clock Frequency | Data Rate | CAS Latency | $t_{RCD}$ (ns) | $t_{RP}$ (ns) |
|---|---|---|---|---|
| 1066MHz | 2133Mbps/pin | 14 | 13.09 | 13.09 |
| 933MHz | 1866Mbps/pin | 13 | 13.91 | 13.91 |
| 800MHz | 1600Mbps/pin | 11 | 13.75 | 13.75 |
| 667MHz | 1333Mbps/pin | 9 | 13.5 | 13.5 |

## Table 2. Addressing

| Parameter | 256M x8 | 128M x16 |
|---|---|---|
| # of Bank | 8 | 8 |
| Row Addressing | A0 – A14 | A0 – A13 |
| Column Addressing | A0 – A9 | A0 – A9 |
| Bank Addressing | BA0 – BA2 | BA0 – BA2 |
| Page size | 1KB | 2KB |
| Auto Precharge | A10 / AP | A10 / AP |
| BL switch on the fly | A12 / BC# | A12 / BC# |

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## Table 3. Ordering Information (x8)

| Commercial Grade | | | | |
|---|---|---|---|---|
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD08EWAHK-09H | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-10H | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-12H | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-15H | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD08EWAHK-09H | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-10H | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-12H | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-15H | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Industrial Grade** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD08EWAHK-09IH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-10IH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-12IH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-15IH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD08EWAHK-09IH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-10IH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-12IH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-15IH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Automotive Grade3** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD08EWAHK-09AH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-10AH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-12AH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-15AH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD08EWAHK-09AH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-10AH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-12AH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-15AH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Automotive Grade2** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD08EWAHK-09BH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-10BH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-12BH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD08EWAHK-15BH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD08EWAHK-09BH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-10BH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-12BH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD08EWAHK-15BH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |

WAH: indicates 7.5 x 10.5 x 1.0mm FBGA package
K: indicates Generation Code
I: indicates Industrial Grade
A: indicates Automotive Grade3
B: indicates Automotive Grade2
H (last digit): indicates Pb and Halogen Free

## Table 4. Ordering Information (x16)

| Commercial Grade | | | | |
|---|---|---|---|---|
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD16EWBK-09H | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-10H | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-12H | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-15H | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD16EWBK-09H | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-10H | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-12H | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-15H | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Industrial Grade** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD16EWBK-09IH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-10IH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-12IH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-15IH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD16EWBK-09IH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-10IH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-12IH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-15IH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Automotive Grade3** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD16EWBK-09AH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-10AH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-12AH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-15AH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD16EWBK-09AH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-10AH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-12AH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-15AH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| **Automotive Grade2** | | | | |
| **Part Number** | **Clock Frequency** | **Data Rate** | **Power Supply** | **Package** |
| EM6GD16EWBK-09BH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-10BH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-12BH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6GD16EWBK-15BH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.5V, $V_{DDQ}$ 1.5V | FBGA |
| EM6HD16EWBK-09BH | 1066MHz | 2133Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-10BH | 933MHz | 1866Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-12BH | 800MHz | 1600Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |
| EM6HD16EWBK-15BH | 667MHz | 1333Mbps/pin | $V_{DD}$ 1.35V, $V_{DDQ}$ 1.35V | FBGA |

WB: indicates 7.5 x 13 x 1.0mm FBGA package
K: indicates Generation Code
I: indicates Industrial Grade
A: indicates Automotive Grade3
B: indicates Automotive Grade2
H (last digit): indicates Pb and Halogen Free

## Ball Assignment

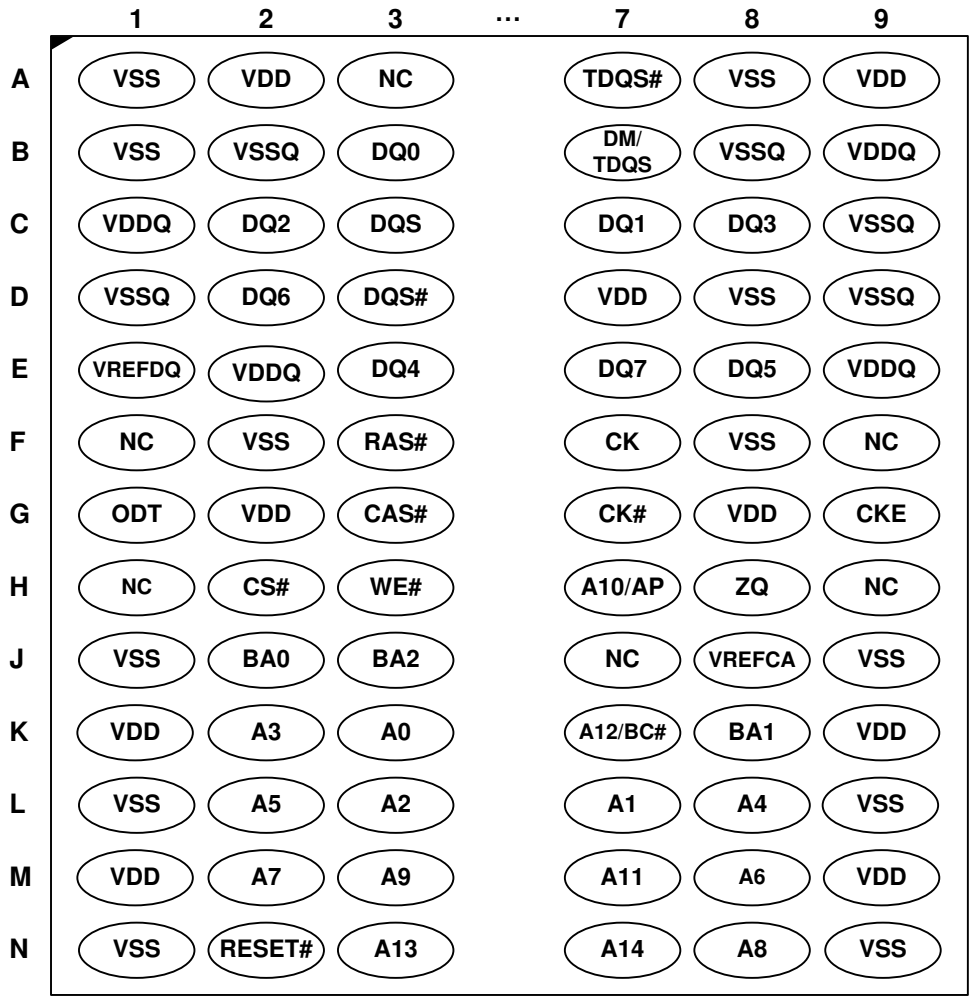



**Figure 1. 78-Ball (FBGA Top View) for x8**

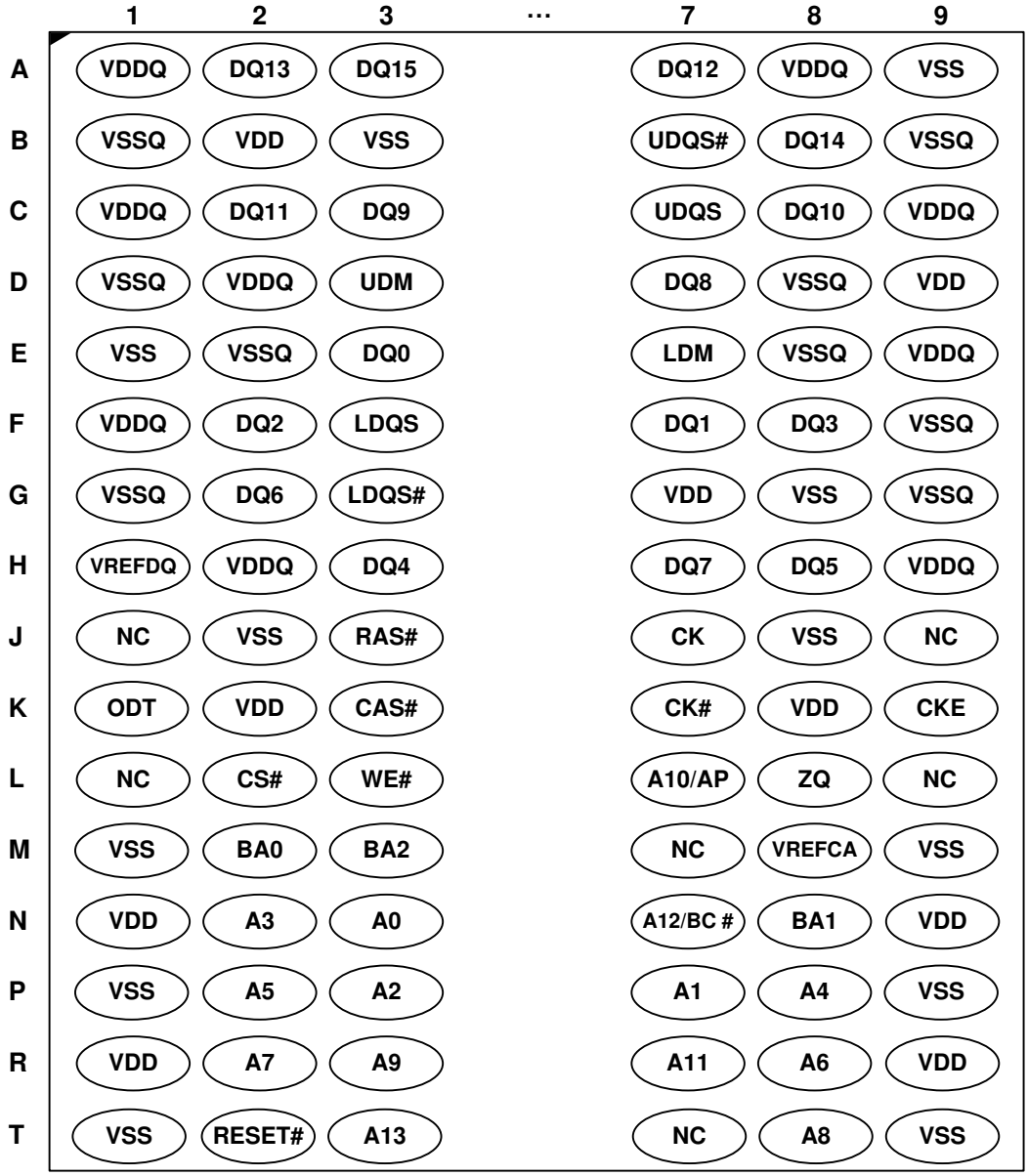



**Figure 2. 96-Ball (FBGA Top View) for x16**

## Functional Block Diagram

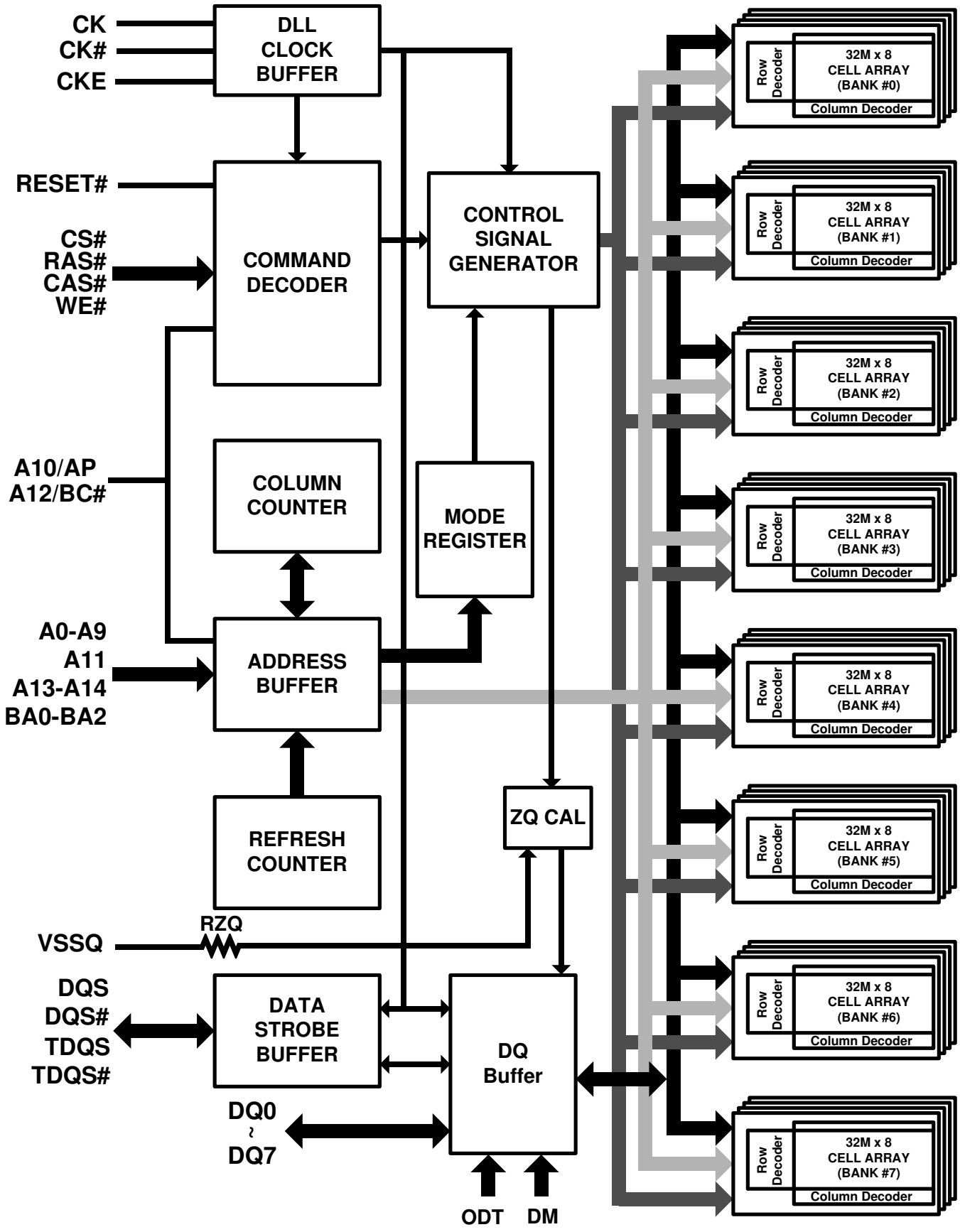



**Figure 3. Block Diagram for x8**

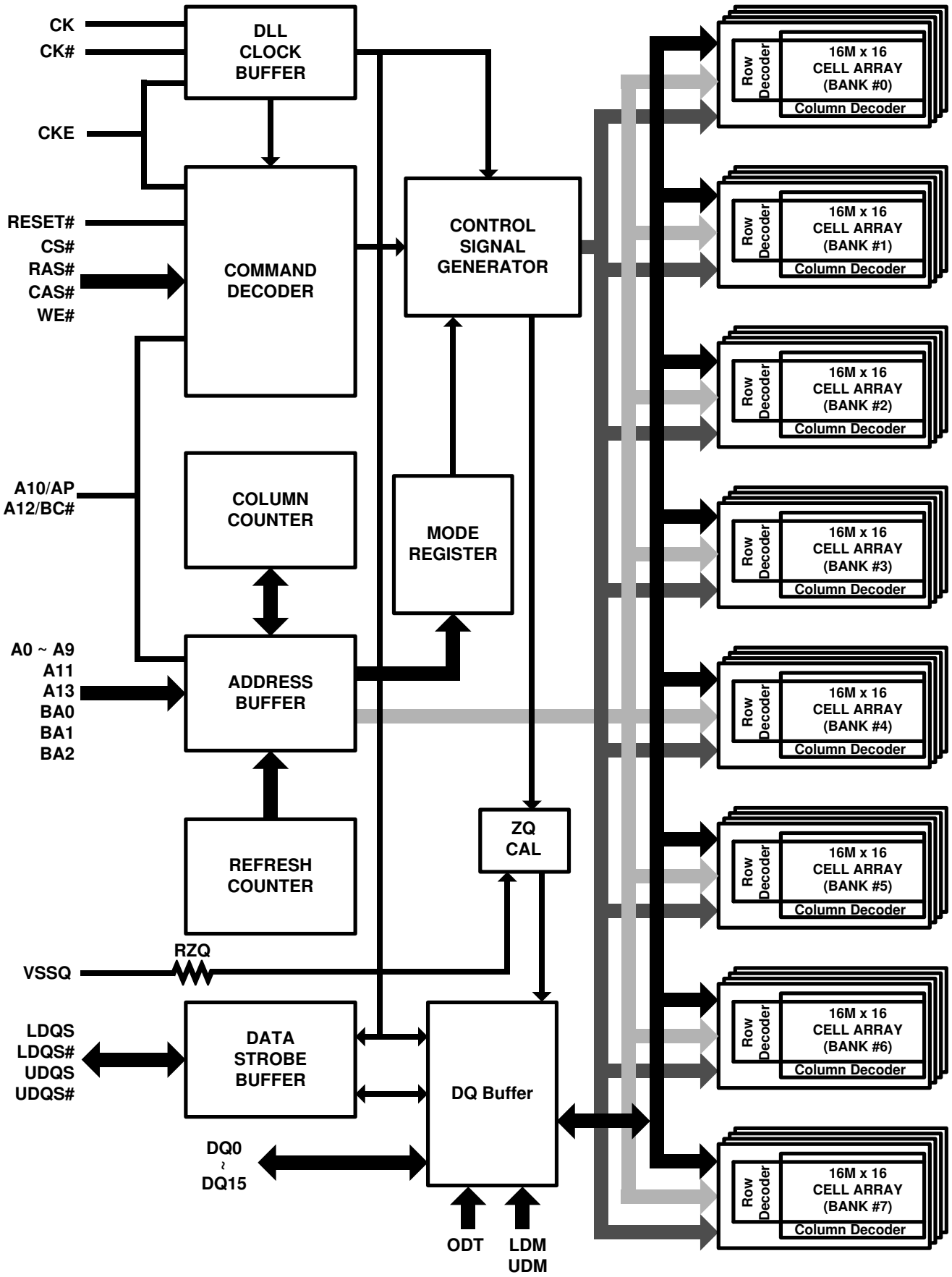



**Figure 4. Block Diagram for x16**

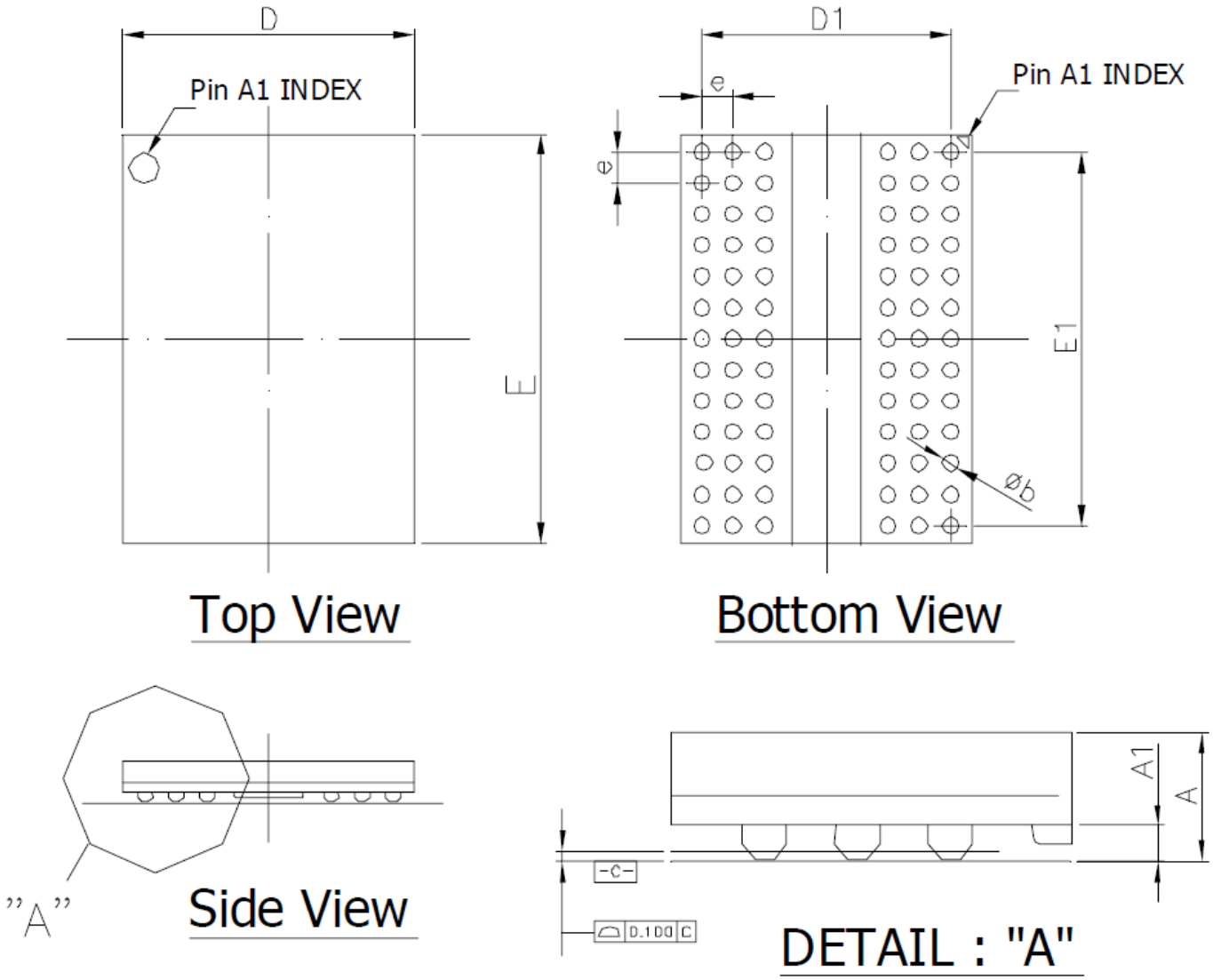
## Functional Description

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n Prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A14 select the row; refer to "Addressing" for specific requirements). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

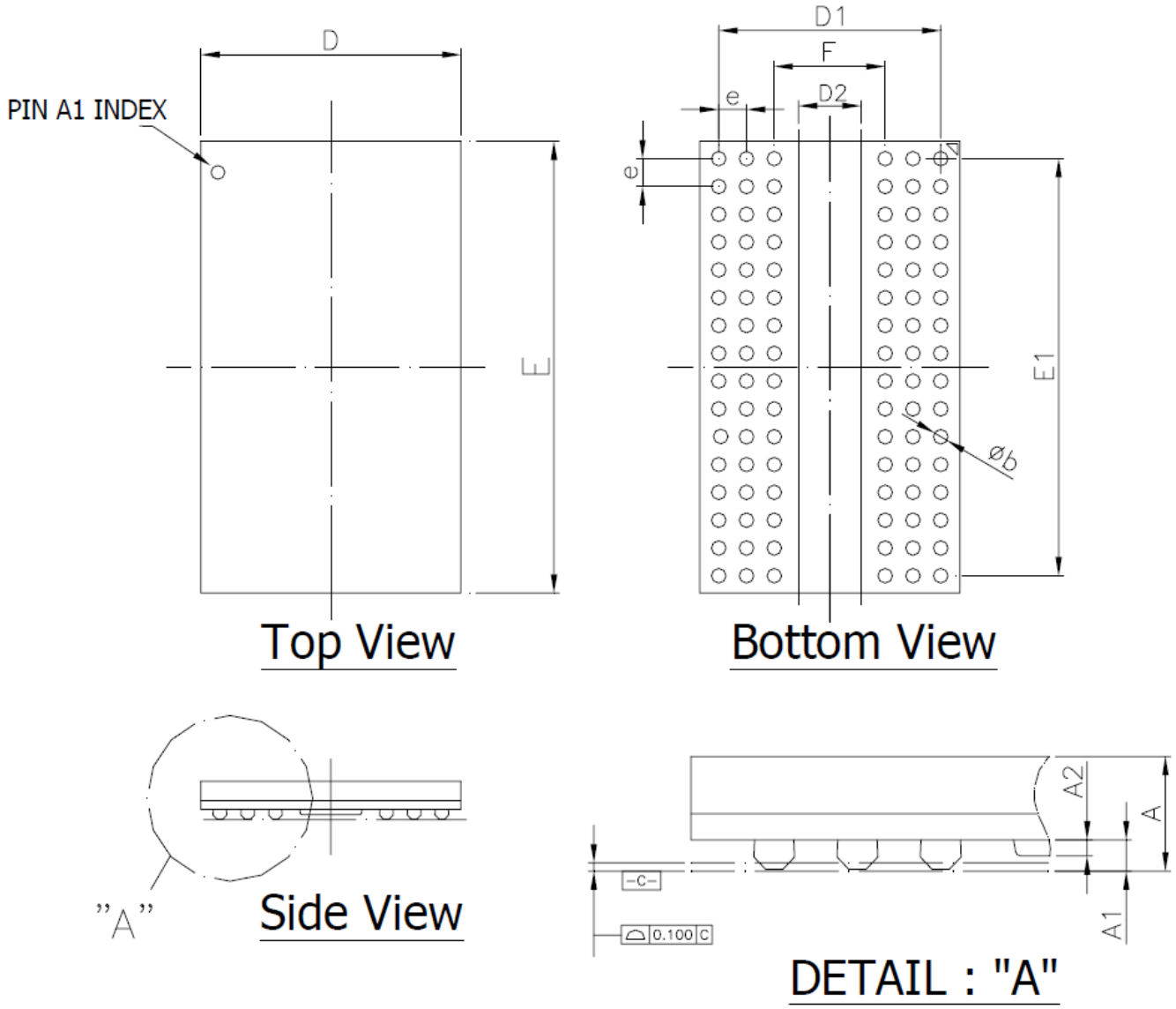
Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation. More detailed information can be found in JESD79-3F and JESD79-3-1A.

## Package Outline Drawing Information




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | -- | -- | 0.039 | -- | -- | 1.00 |
| A1 | 0.010 | -- | 0.016 | 0.25 | -- | 0.40 |
| D | 0.291 | 0.295 | 0.299 | 7.40 | 7.50 | 7.60 |
| E | 0.409 | 0.413 | 0.417 | 10.40 | 10.50 | 10.60 |
| D1 | -- | 0.252 | -- | -- | 6.40 | -- |
| E1 | -- | 0.378 | -- | -- | 9.60 | -- |
| e | -- | 0.031 | -- | -- | 0.80 | -- |
| b | 0.016 | 0.018 | 0.020 | 0.40 | 0.45 | 0.50 |

**Figure 6. 78-Ball FBGA Package 7.5x10.5x1.0mm(max) for x8**




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | -- | -- | 0.039 | -- | -- | 1.00 |
| A1 | 0.010 | -- | 0.016 | 0.25 | -- | 0.40 |
| A2 | -- | -- | 0.008 | -- | -- | 0.20 |
| D | 0.291 | 0.295 | 0.299 | 7.40 | 7.50 | 7.60 |
| E | 0.508 | 0.512 | 0.516 | 12.90 | 13.00 | 13.10 |
| D1 | -- | 0.252 | -- | -- | 6.40 | -- |
| E1 | -- | 0.472 | -- | -- | 12.00 | -- |
| F | -- | 0.126 | -- | -- | 3.20 | -- |
| e | -- | 0.031 | -- | -- | 0.80 | -- |
| b | 0.016 | 0.018 | 0.020 | 0.40 | 0.45 | 0.50 |
| D2 | -- | -- | 0.081 | -- | -- | 2.05 |

**Figure 7. 96-Ball FBGA Package 7.5x13x1.0mm(max) for x16**