4Gb LPDDR4X Synchronous DRAM (SDRAM)

Advance (Rev. 1.1, Dec. /2025)

Overview

The LPDDR4X SDRAM is organized with one channel per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

This LPDDR4X device uses a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock.

Features

- JEDEC standard Compliant
- Fast clock rate: 2133/1866/1600 MHz
- Low-voltage Core and I/O Power Supplies:
  - V_{DD1} = 1.8V (1.7V~1.95V)
  - V_{DD2} = 1.1V (1.06V~1.17V)
  - V_{DDQ} = 0.6V (0.57V~0.65V)
- Operating Temperature:
  - T_C = -25 ~ 85°C (Commercial)
- Supports JEDEC clock jitter specification
- Configuration:
  - 256 Meg x 16 (1 channels x16 I/O)
- 8 internal bank s per each channel
- 16n-bit prefetch architecture
- Single data rate (multiple cycles) CMD/ADR bus
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies
- Programmable and on-the-fly burst lengths
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Selectable output drive strength (DS)
- Dynamic ODT :
  - DQ ODT: VSSQ Termination
  - CA ODT: VSS Termination
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- Interface: LVSTL
- Internal VREF and VREF Training
- ZQ Calibration
- RoHS compliant
- 200-ball 10 x 14.5 x 1.1mm (max) FBGA Package
  - Pb and Halogen Free

Table 1. Ordering Information

Part Number	Configuration	Clock Frequency	Data Rate	Power Supply	Package
EM6PE16MBAJB-46H	256Mx16 (4Gb/Package)	2133MHz	4266Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PE16MBAJB-53H	256Mx16 (4Gb/Package)	1866MHz	3733Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA
EM6PE16MBAJB-62H	256Mx16 (4Gb/Package)	1600MHz	3200Mbps/pin	V_{DD1} 1.8V, V_{DD2} 1.1V, V_{DDQ} 0.6V	FBGA

BAJ: indicates 200-ball 10 x 14.5 x 1.1mm (max) FBGA Package

B: indicates Generation Code

H: indicates Pb and Halogen Free for FBGA Package

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Package Block Diagram

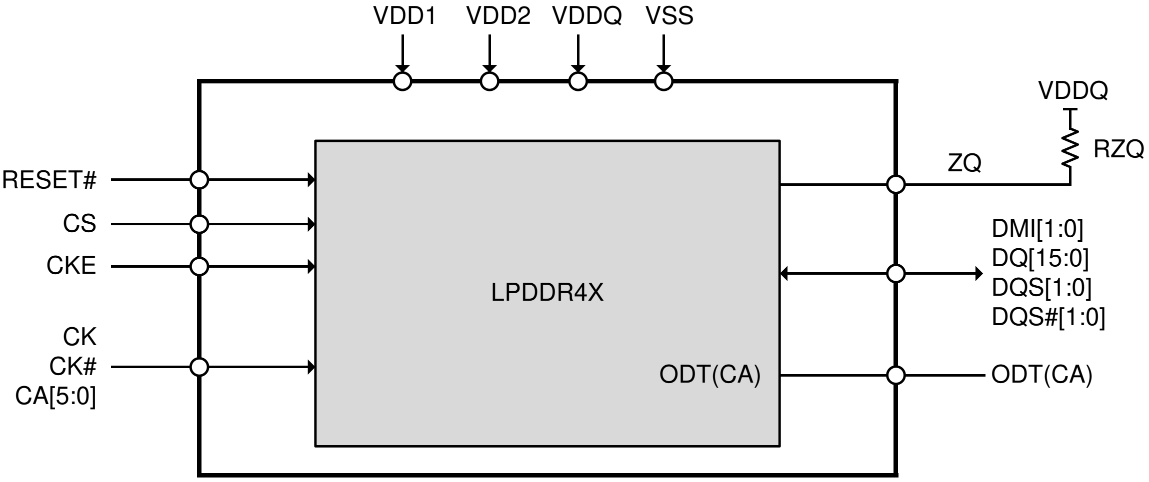
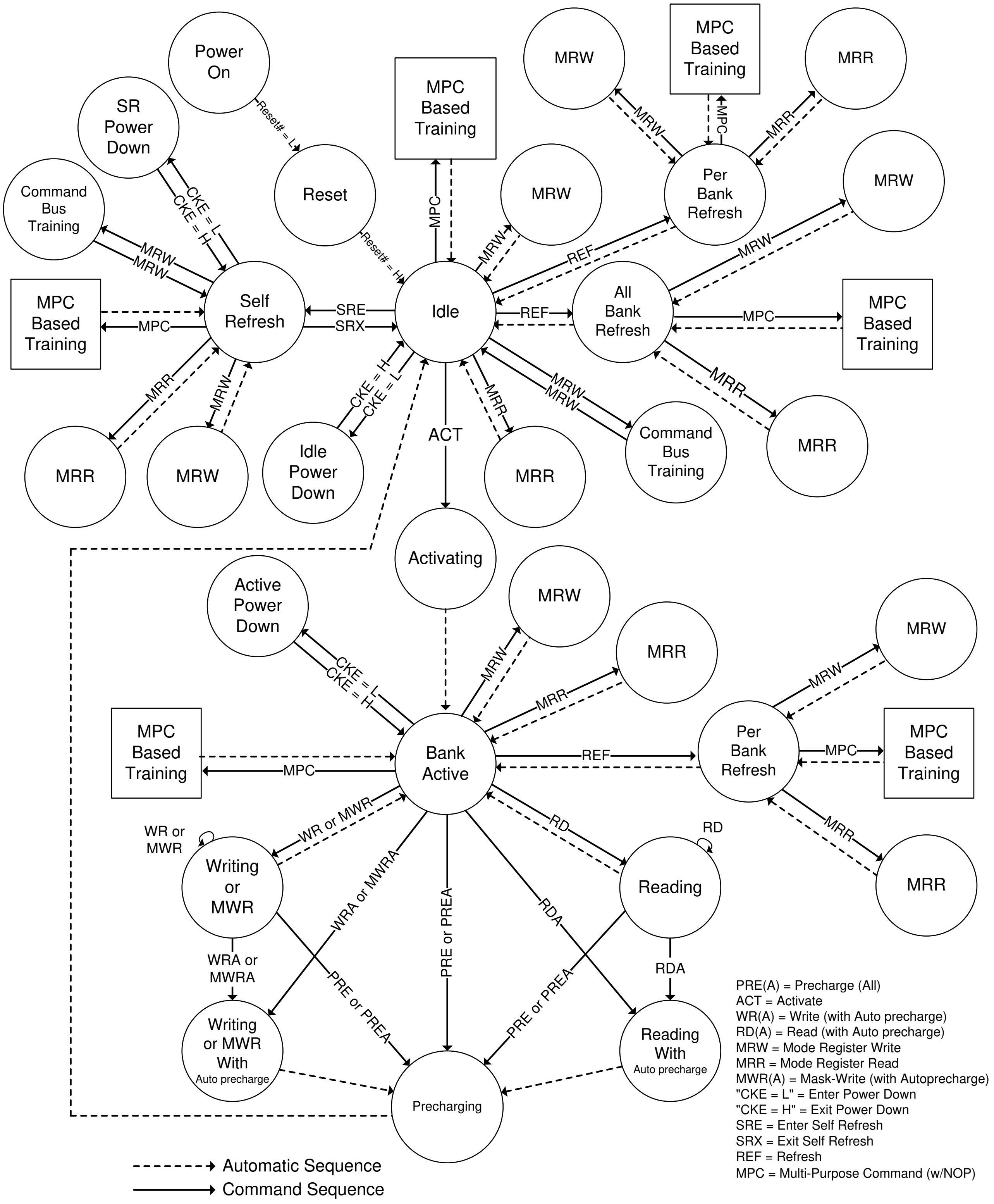


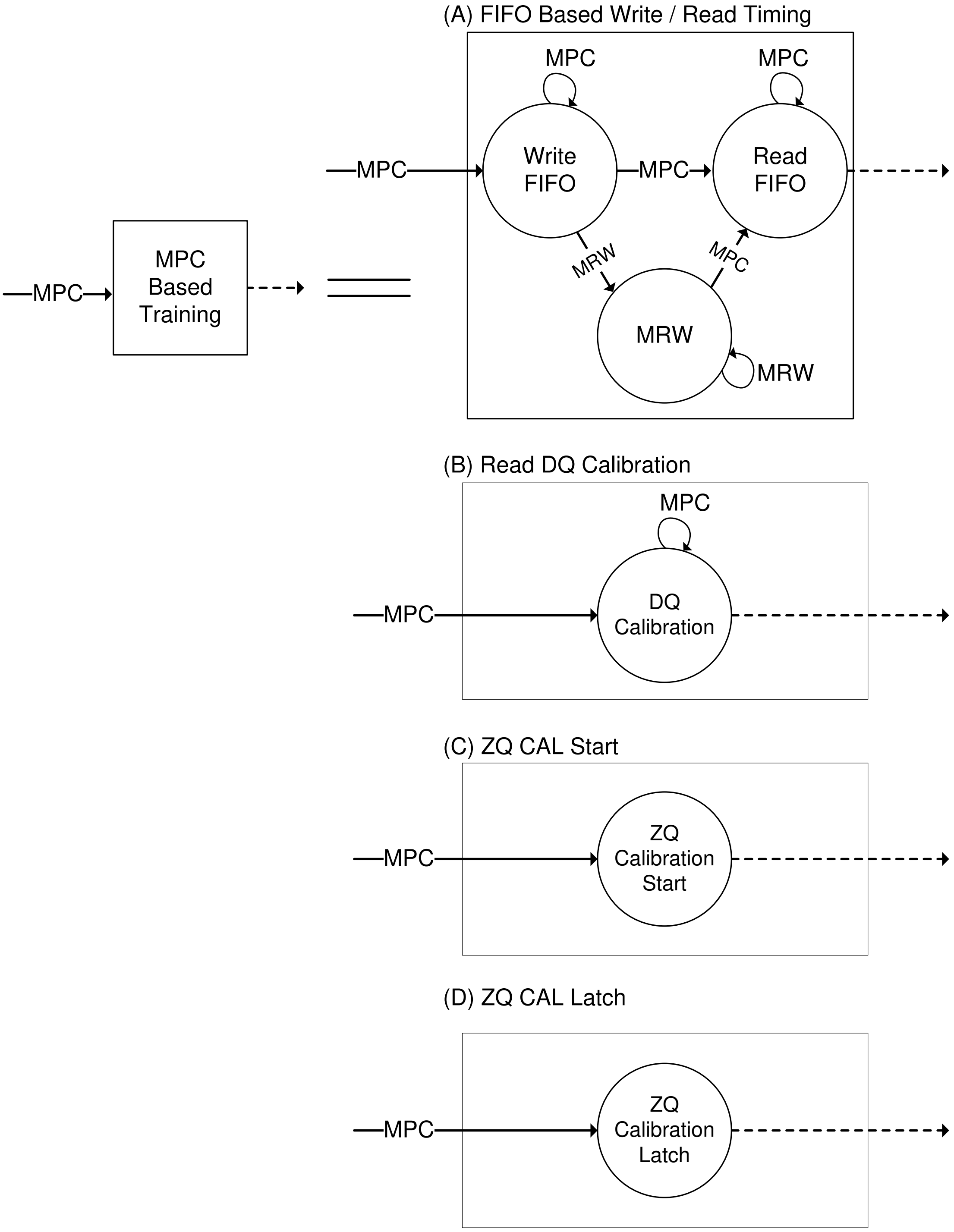
Figure 1. Single Channel Package Block Diagram (x16)

Simplified LPDDR4X State Diagram



PRE(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Auto precharge)
RD(A) = Read (with Auto precharge)
MRW = Mode Register Write
MRR = Mode Register Read
MWR(A) = Mask-Write (with Autoprecharge)
"CKE = L" = Enter Power Down
"CKE = H" = Exit Power Down
SRE = Enter Self Refresh
SRX = Exit Self Refresh
REF = Refresh
MPC = Multi-Purpose Command (w/NOP)

Figure 2. LPDDR4X: Simplified Bus Interface State Diagram - Sheet 1



NOTES:
1. From the Self Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the Self Refresh section for more information.
2. In IDLE state, all banks are precharged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the Mode Register Write (MRW) section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the Multi-Purpose Command (MPC) section for more information.
5. This simplified State Diagram is Intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return " and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET.

Figure 3. LPDDR4X: Simplified Bus Interface State Diagram - Sheet 2

Ball Assignment

	1	2	3	4	5	…	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ		NC	VDD2	VSS	NC	NC
B	NC	DQ0	VDDQ	DQ7	VDDQ		VDDQ	DQ15	VDDQ	DQ8	NC
C	VSS	DQ1	DMI0	DQ6	VSS		VSS	DQ14	DMI1	DQ9	VSS
D	VDDQ	VSS	DQS0	VSS	VDDQ		VDDQ	VSS	DQS1	VSS	VDDQ
E	VSS	DQ2	DQS0#	DQ5	VSS		VSS	DQ13	DQS1#	DQ10	VSS
F	VDD1	DQ3	VDDQ	DQ4	VDD2		VDD2	DQ12	VDDQ	DQ11	VDD1
G	VSS	ODT_CA	VSS	VDD1	VSS		VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0	NC	CS	VDD2		VDD2	CA2	CA3	CA4	VDD2
J	VSS	CA1	VSS	CKE	NC		CK	CK#	VSS	CA5	VSS
K	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
L											
M											
N	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
P	VSS	NC	VSS	NC	NC		NC	NC	VSS	NC	VSS
R	VDD2	NC	NC	NC	VDD2		VDD2	NC	NC	NC	VDD2
T	VSS	NC	VSS	VDD1	VSS		VSS	VDD1	VSS	RESET#	VSS
U	VDD1	NC	VDDQ	NC	VDD2		VDD2	NC	VDDQ	NC	VDD1
V	VSS	NC	NC	NC	VSS		VSS	NC	NC	NC	VSS
W	VDDQ	VSS	NC	VSS	VDDQ		VDDQ	VSS	NC	VSS	VDDQ
Y	VSS	NC	NC	NC	VSS		VSS	NC	NC	NC	VSS
AA	NC	NC	VDDQ	NC	VDDQ		VDDQ	NC	VDDQ	NC	NC
AB	NC	NC	VSS	VDD2	VSS		VSS	VDD2	VSS	NC	NC

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 Die pad VSS and VSSQ signals are combined to VSS package balls.

Figure 4. 200-Ball x16 (FBGA Top View)

Addressing

Table 2. LPDDR4X SDRAM Addressing

Memory Density		256Mx16 (4Gb/Package)
Organization		x16
Number of Channels		1
Number of Ranks		1
Density per channel		4Gb
Configuration		32Mb x 16DQ x 8 banks x 1 channel
Number of Banks (per Channel)		8
Array Pre-Fetch (Bits, per channel)		256
Number of Rows (per channel)		32,768
Number of Columns (fetch boundaries)		64
Page Size (Bytes)		2048
Bank Address		BA0-BA2
x16	Row Addresses	R0-R14
	Column Addresses	C0-C9
Burst Starting Address Boundary		64-bit

Note 1. The lower two column addresses (C0 - C1) are assumed to be "zero" and are not transmitted on the CA bus.
Note 2. Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.
Note 3. For non - binary memory densities, only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

Ball Descriptions

Table 3. Ball Details

Symbol	Type	Description
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. AC timings for CA parameters are referenced to CK.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code.
CS	Input	**Chip Select:** CS is part of the command code.
CA[5:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table.
DQ[15:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0], DQS#[1:0]	I/O	**Data Strobe:** DQS and DQS# are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair.
DMI[1:0]	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDD1, VDD2, VDDQ	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference.
RESET#	Input	**RESET:** When asserted LOW, the RESET# signal resets all channels of the die. There is one RESET# pad per die.
ODT_CA_A, ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
NC	-	**No connect**: Not internally connected.

Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.
CKE signal has to be held high when the commands listed in the command truth table input.

Table 4. Command Truth Table

	Command Pins	CA Pins							
Command	**CS**	**CA0**	**CA1**	**CA2**	**CA3**	**CA4**	**CA5**	**CK Edge**	**Notes**
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,2,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1~4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1~4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	L	R1	1,2
	L	V						R2	
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1~3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1~3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1~3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read- 2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write - 1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,2,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write- 2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,2,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read- 1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	V	R1	1~3,10
	L	BA0	BA1	BA2	V	R10	R11	R2	
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Note 1. All LPDDR4X commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.

Note 2. "V" means "H" or "L" (a defined logic level). "X" means don’t care in which case CA[5:0] can be floated.

Note 3. Bank addresses BA[2:0] determine which bank is to be operated upon.

Note 4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don’t care.

Note 5. Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).

Note 6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.

Note 7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".

Note 8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.

Note 9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.

Note 10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.

Note 11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.

Note 12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

Power-up, Initialization, and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as the table below.

Table 5. MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
VREF(CA) Setting	MR12 OP[6]	1_B	VREF(CA) Range[1] enabled
VREF(CA) Value	MR12 OP[5:0]	011101_B	Range1: 50.3% of VDDQ
VREF(DQ) Setting	MR14 OP[6]	1_B	VREF(DQ) Range[1] enabled
VREF(DQ) Value	MR14 OP[5:0]	011101_B	Range1: 50.3% of VDDQ

Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4X device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET# is recommended to be LOW (≤ 0.2 x VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET# is held LOW. Power supply voltage ramp requirements are provided in the table below. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

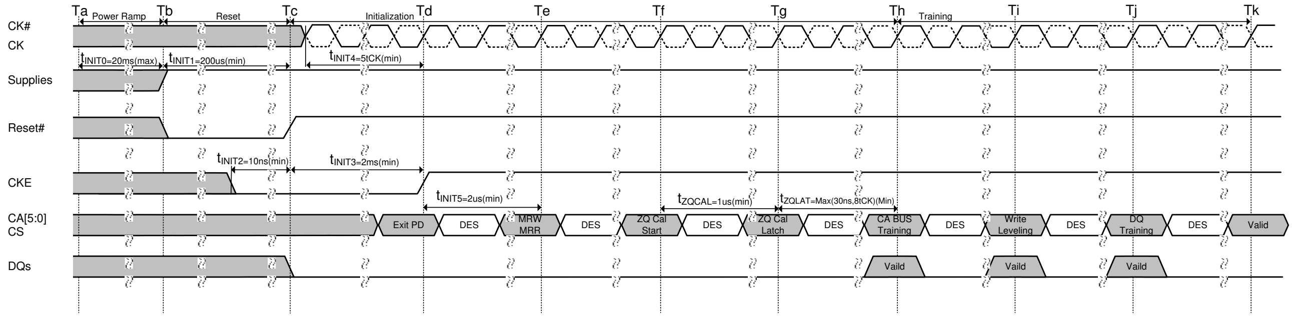
Table 6. Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200 mV

Note 1. Ta is the point when any power supply first reaches 300 mV.
Note 2. Voltage ramp conditions in Table 8 apply between Ta and power-off (controlled or uncontrolled).
Note 3. Tb is the point at which all supply and reference voltages are within their defined ranges.
Note 4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
Note 5. The voltage difference between any of VSS and VSSQ pins must not excess 100 mV.

2. Following the completion of the voltage ramp (Tb), RESET# must be maintained LOW. DQ, DMI, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CKE, CK, CK#, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET# must remain LOW for at least tINIT1 (Tc), after which RESET# can be deasserted to HIGH (Tc). At least 10ns before RESET# de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".



Note 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

Figure 5. Power Ramp and Initialization Sequence

4. After RESET# is de-asserted (Tc), wait at least tINIT3 before activating CKE. Clock (CK, CK#) is required to be started and stabilized for tINIT4 before CKE goes active (Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4X DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4X device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4X device will power-up with receivers configured for low-speed operations, and VREF (CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(DQ)(Tj). The device will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 7. Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage ramp time
t_{INIT1}	200	-	us	Minimum RESET# LOW time after completion of voltage ramp
t_{INIT2}	10	-	ns	Minimum CKE low time before RESET# high
t_{INIT3}	2	-	ms	Minimum CKE low time after RESET# high
t_{INIT4}	5	-	t_{CK}	Minimum stable clock before first CKE high
t_{INIT5}	2	-	us	Minimum idle time before first MRW/MRR command
t_{ZQCAL}	1	-	us	ZQ calibration time
t_{ZQLAT}	Max(30ns, 8t_{CK})	-	ns	ZQCAL latch quiet time
t_{CKb}	Note *1,2	Note *1,2	ns	Clock cycle time during boot

Note:

1. Min tCKb guaranteed by DRAM test is 18 ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET# below 0.2 x VDD2 anytime when reset is needed. RESET# needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET#.
2. Repeat steps 4 to 10 in Voltage Ramp section.

Table 8. Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
t_{PW_RESET}	100	-	ns	Minimum RESET# low Time for Reset Initialization with stable power

Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (0.2 × V_{DD2}) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. RESET#, CK, CK#, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 9. Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

The voltage difference between V_{SS}, V_{SSQ} must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/μs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 10. Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	t_{POFF}	-	2	s

Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) at a rising edge of CK.

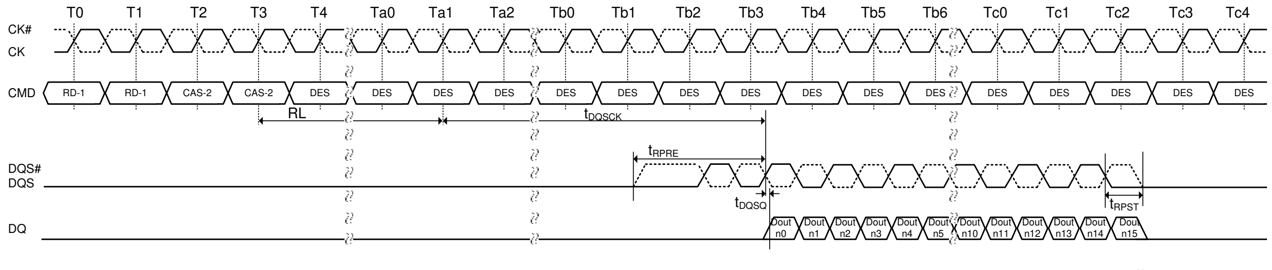
The LPDDR4X-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see Command Truth Table).

Read Preamble and Postamble

The DQS strobe for the LPDDR4X requires a pre-amble prior to the first latching edge (the rising edge of DQS with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

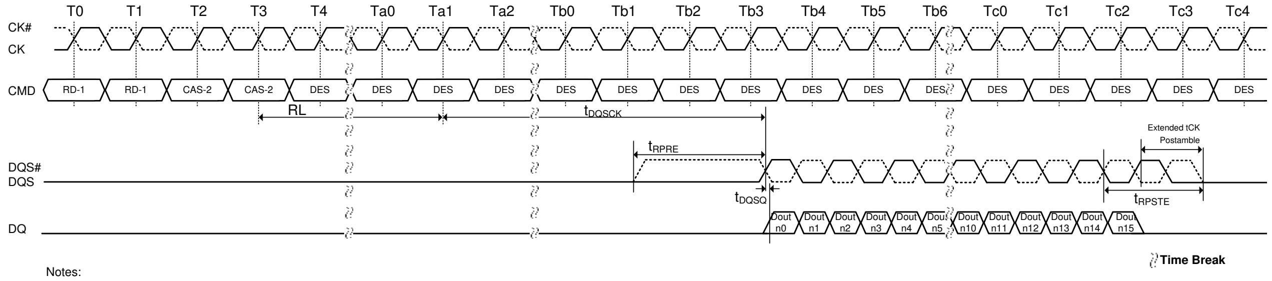
For Read operations the pre-amble is 2*tCK, but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4X will have a DQS Read post-amble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS postamble will be 0.5*tCK driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. The drawings below show examples of DQS Read post-amble for both standard (tRPST) and extended (tRPSTE) post-amble operation.



Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ.
3. DQS#/DQS is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS#/DQS can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 6. DQS Read Preamble and Postamble: Toggling Preamble and 0.5nCK Postamble

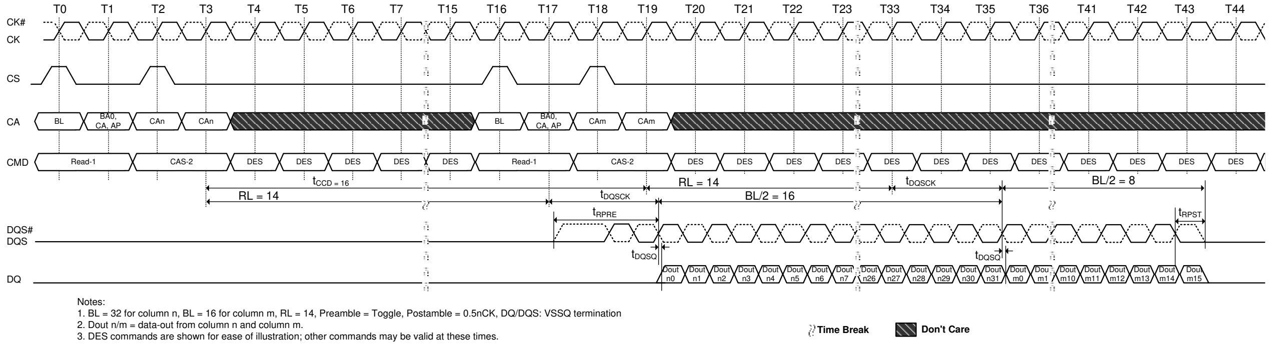


Notes:
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (Extended)
2. DQS and DQ terminated VSSQ.
3. DQS#/DQS is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS#/DQS can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 7. DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble

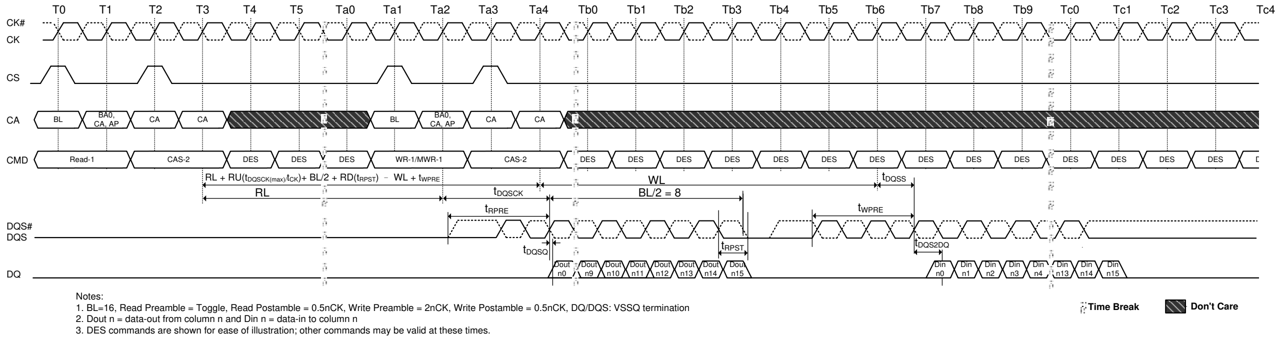
Burst Read Operation

A burst Read command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be "0", so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent data out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS and DQS#.



Notes:
1. BL = 32 for column n, BL = 16 for column m, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

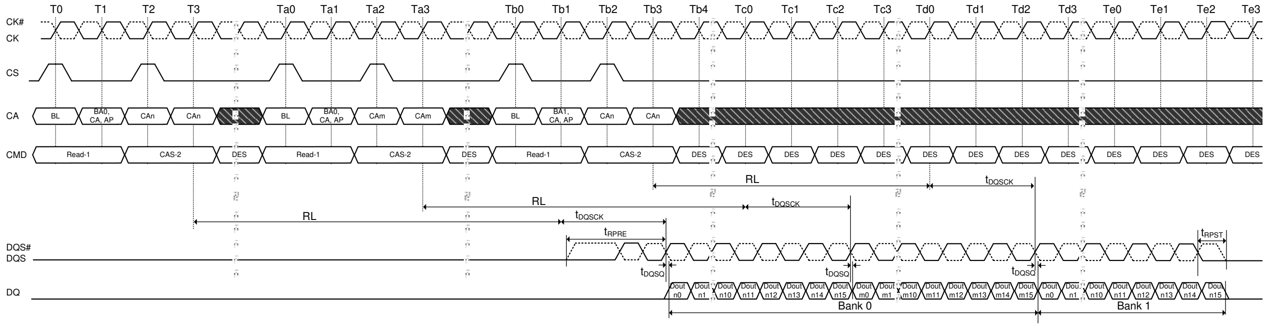
Figure 8. Burst Read Timing



Notes:
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 9. Burst Read followed by Burst Write or Burst Mask Write

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL).
Minimum Read-to-Write or Mask Write latency is RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE.



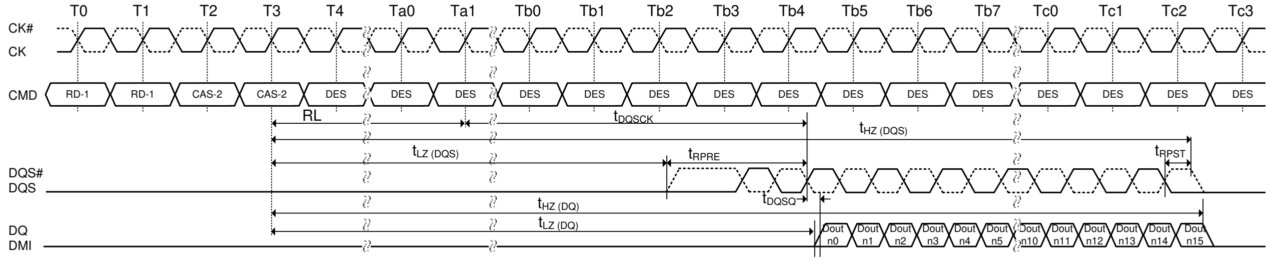
Notes:
1. BL = 16, tCCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Time Break ▨ **Don't Care**

Figure 10. Seamless Burst Read

The seamless Burst Read operation is supported by placing a Read command at every tCCD(Min) interval for BL16 (or every 2 x tCCD(Min) for BL32).

The seamless Burst Read can access any open bank.



Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS, DQ and DMI terminated VSSQ.
3. Output driver does not turn on before an end point of tLZ(DQS) and tLZ(DQ).
4. Output driver does not turn off before an end point of tHZ(DQS) and tHZ(DQ)

Time Break

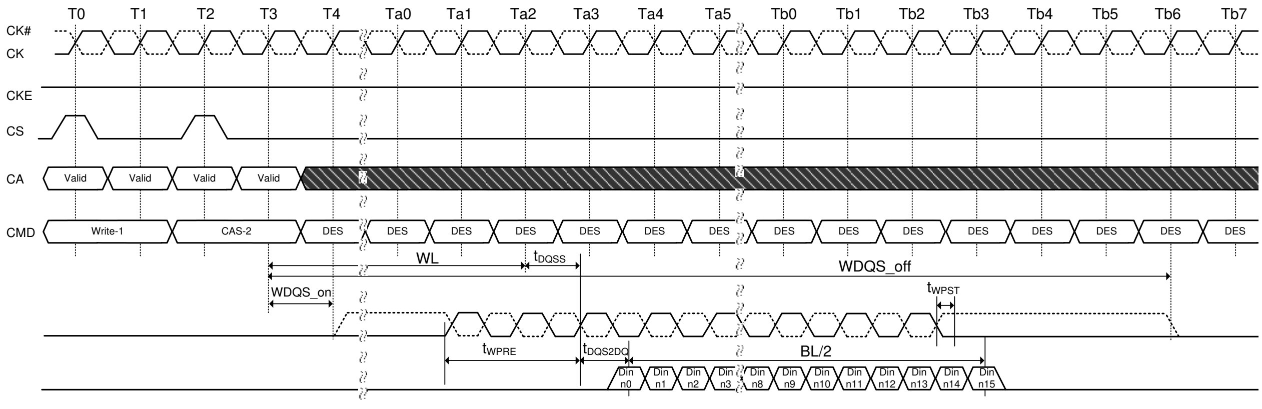
Figure 11. Read Timing

Write Preamble and Postamble

The DQS strobe for the LPDDR4X requires a pre-amble prior to the first latching edge (the rising edge of DQS with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

For Write operations, a 2*tCK pre-amble is required at all operating frequencies.

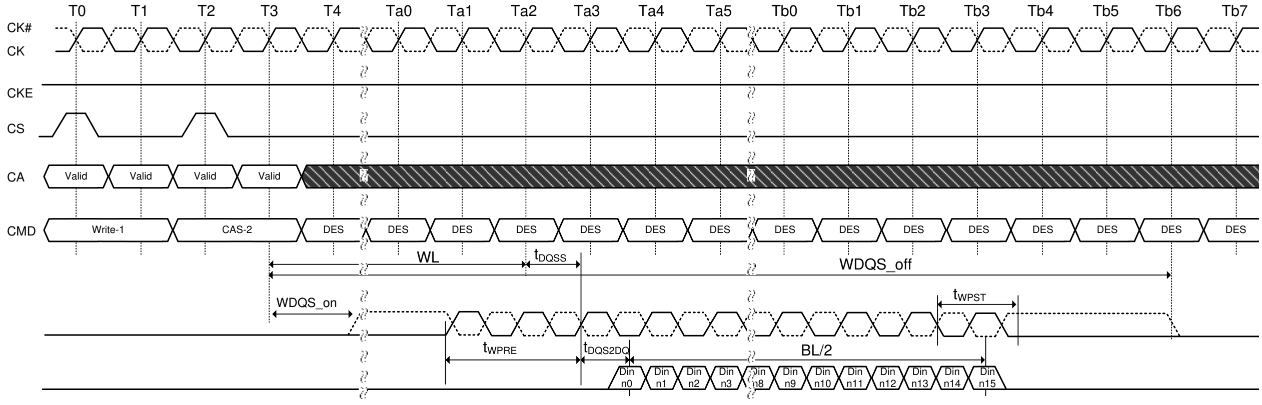
LPDDR4X will have a DQS Write post-amble of 0.5*tCK or extended to 1.5*tCK. Standard DQS post-amble will be 0.5*tCK driven by the memory controller for Writes. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Write post-amble. The drawings below show examples of DQS Write post-amble for both standard (tWPST) and extended (tWPSTE) post-amble operation.



Notes:
1. BL = 16, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ
3. DQS/DQS# is “don't care” prior to the start of tWPRE.
No transition of DQS is implied, as DQS/DQS# can be HIGH, LOW, or HI-Z prior to tWPRE.

Time Break ▨ Don't Care

Figure 13. DQS Write Preamble and Postamble: 0.5nCK Postamble



Notes:
1. BL = 16, Postamble = 1.5nCK
2. DQS and DQ terminated VSSQ
3. DQS/DQS# is “don't care” prior to the start of tWPRE.
No transition of DQS is implied, as DQS/DQS# can be HIGH, LOW, or HI-Z prior to tWPRE.

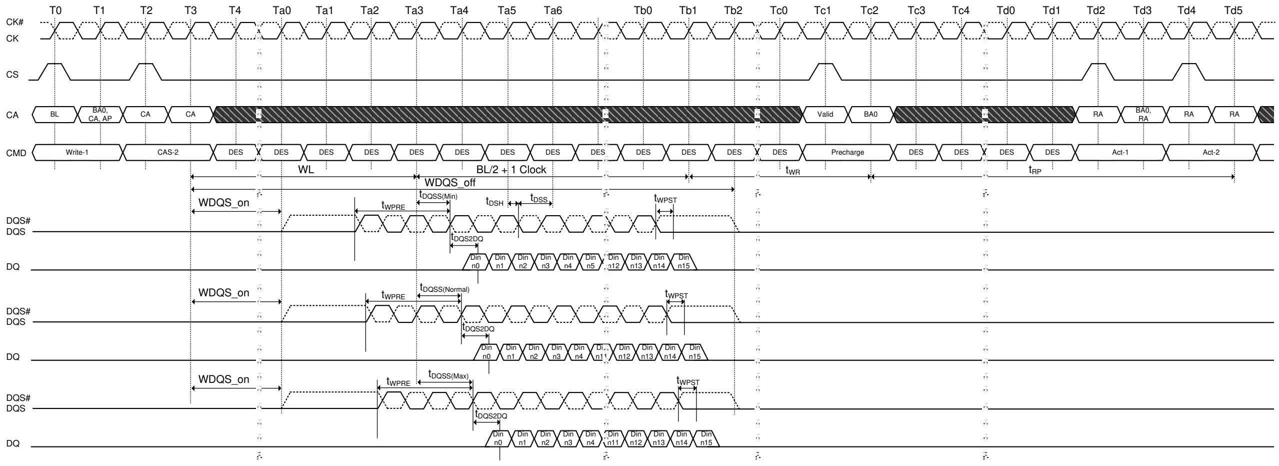
Time Break ▨ Don't Care

Figure 14. DQS Write Preamble and Postamble: 1.5nCK Postamble

Burst Write Operation

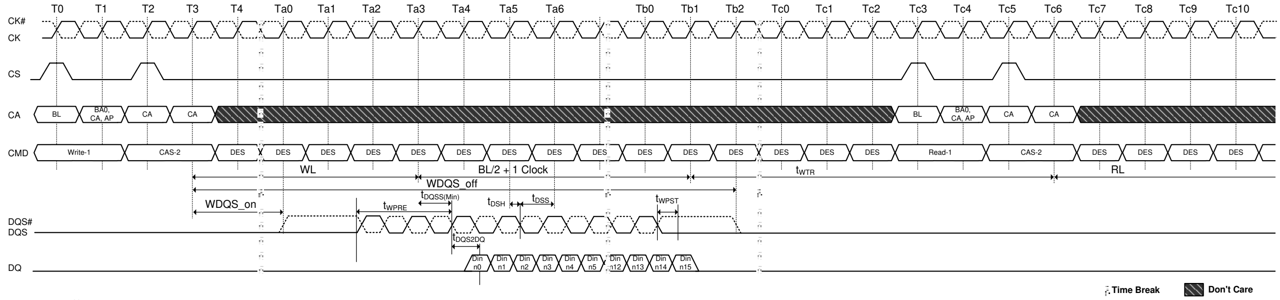
A burst Write command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst Write commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid "latching" edge of DQS must be driven WL * tCK + tDQSS after the rising edge of Clock that completes a write command.

The LPDDR4X-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE pre-amble is required to be 2 x tCK. The DQS strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (Write post-amble) after the completion of the burst Write. After a burst Write operation, tWR must be satisfied before a Precharge command to the same bank can be issued. Pin input timings are measured relative to the cross point of DQS and DQS#.



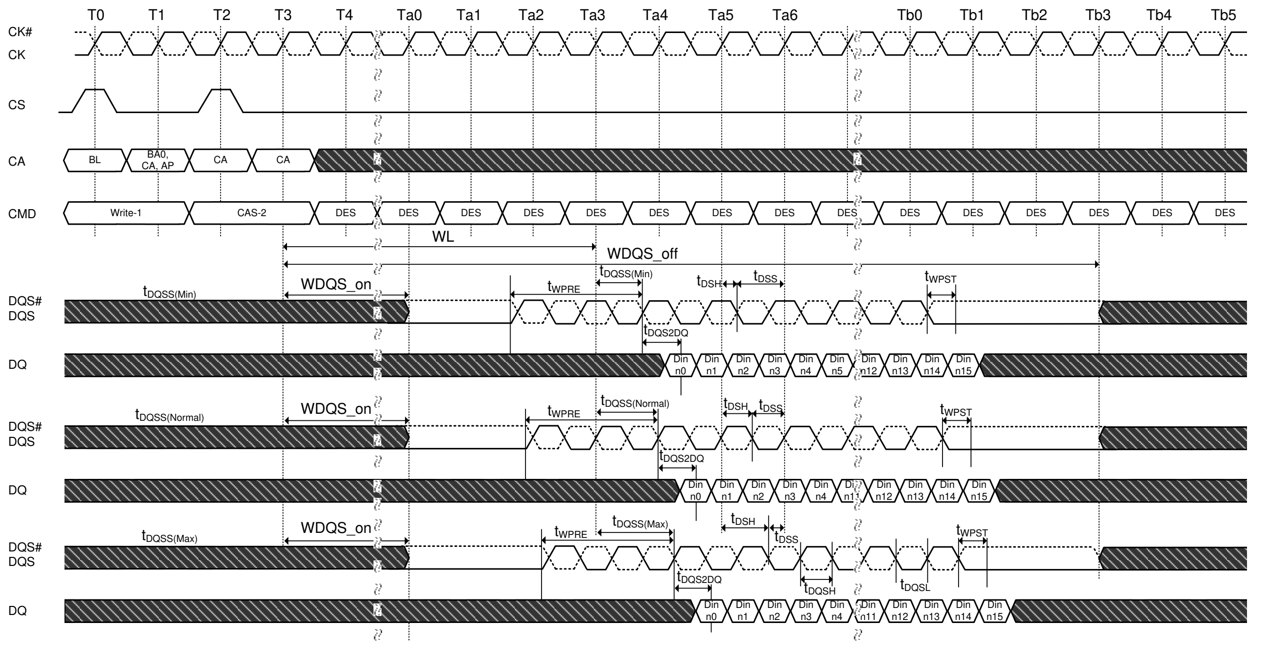
Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. The minimum number of clock cycles from the burst write command to the precharge command for same bank is [WL + 1 + BL/2 + RU(tWR/tCK)].
4. tWR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 15. Burst Write Operation



Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 16. Burst Write Followed by Burst Read



Notes:
1. BL=16, Write Postamble = 0.5nCK
2. Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

≀ **Time Break** ▨ **Don't Care**

Figure 17. Write Timing

Write and Masked Write operation DQS controls (WDQS Control)

LPDDR4X-SDRAMs support write and masked write operations with the following DQS controls. Before and after Write and Masked Write operations are issued, DQS/DQS# is required to have a sufficient voltage gap to make sure the write buffers operating normally without any risk of metastability.

The LPDDR4X-SDRAM is supported by either of two WDQS control modes below.
Mode 1: Read Based Control
Mode 2: WDQS_on / WDQS_off definition based control

Regardless of ODT enable/disable, WDQS related timing described here does not allow any change of existing command timing constraints for all read/write operations. In case of any conflict or ambiguity on the command timing constraints caused by the specification here, the specification defined in the Timing Constraints for Training Commands table should have higher priority than WDQS control requirements.

To prevent write preamble related failure, either of the two WDQS controls to the device should be supported.

WDQS Control Mode 1 - Read Based Control

The LPDDR4X-SDRAM needs to be guaranteed the differential WDQS, but the differential WDQS can be controlled as described below. WDQS control requirements here can be ignored while differential read DQS is operated or while DQS hands over from Read to Write and vice versa.

1. At the time a write / masked write command is issued, SoC makes the transition from driving DQS# high to driving differential DQS/DQS#, followed by normal differential burst on DQS pins.
2. At the end of post amble of write / masked write burst, SoC resumes driving DQS# high through the subsequent states except for DQS toggling and DQS turn around time of WT-RD and RD-WT as long as CKE is high.
3. When CKE is low, the state of DQS and DQS# is allowed to be “Don’t Care”.

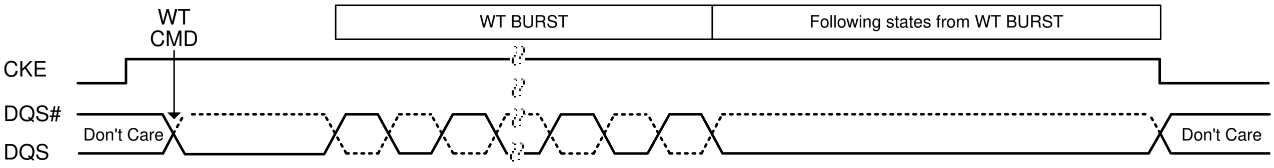


Figure 18. WDQS Control Mode 1 - Read Based Control

WDQS Control Mode 2 - WDQS_on/off

After write / masked write command is issued, DQS and DQS# required to be differential from WDQS_on, and DQS and DQS# can be "Don't Care" status from WDQS_off of write / masked write command. When ODT is enabled, WDQS_on and WDQS_off timing is located in the middle of the operations. When host disables ODT, WDQS_on and WDQS_off constraints conflict with tRTW. The timing does not conflict when ODT is enabled because WDQS_on and WDQS_off timing is covered in ODTLon and ODTLoff. However, regardless of ODT on/off, WDQS_on/off timing below does not change any command timing constraints for all read and write operations. In order to prevent the conflict, WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD). In addition, the period during DQS toggling caused by Read and Write can be counted as WDQS_on/off.

Parameters

- WDQS_on: the max delay from write / masked write command to differential DQS and DQS#.
- WDQS_off: the min delay for DQS and DQS# differential input after the last write / masked write command.
- WDQS_Exception: the period where WDQS_on and WDQS_off timing is overlapped with read operation or with DQS turn around (RD-WT, WT-RD).
  - WDQS_Exception @ ODT disable = max (WL - WDQS_on+ tDQSTA - tWPRE - n*tCK,0 tCK) where RD to WT command gap = tRTW(min)@ODT disable + n*tCK
  - WDQS_Exception @ ODT enable = tDQSTA

Table 11. WDQS_on / WDQS_off Definition

WL		nWR	nRTP	WDQS_on (Max)		WDQS_off (Min)		Lower Clock Frequency Limit (>)	Upper Clock Frequency Limit (≤)
Set A	Set B			Set A	Set B	Set A	Set B		
4	4	6	8	0	0	15	15	10	266
6	8	10	8	0	0	18	20	266	533
8	12	16	8	0	6	21	25	533	800
10	18	20	8	4	12	24	32	800	1066
12	22	24	10	4	14	27	37	1066	1333
14	26	30	12	6	18	30	42	1333	1600
16	30	34	14	6	20	33	47	1600	1866
18	34	40	16	8	24	36	52	1866	2133
nCK	nCK	nCK	nCK	nCK	nCK	nCK	nCK	MHz	MHz

Notes:

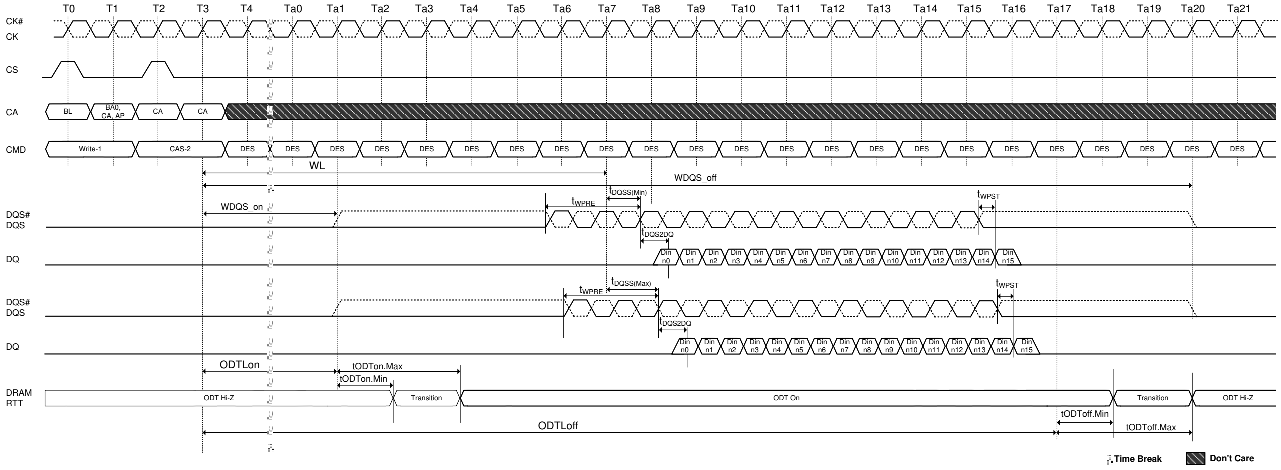
1. WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with read operation period including read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).
2. DQS toggling period caused by read and write can be counted as WDQS_on/off.

Table 12. WDQS_on / WDQS_off Allowable Variation Range

	Min	Max	Unit
WDQS_on	-0.25	0.25	tCK(avg)
WDQS_off	-0.25	0.25	tCK(avg)

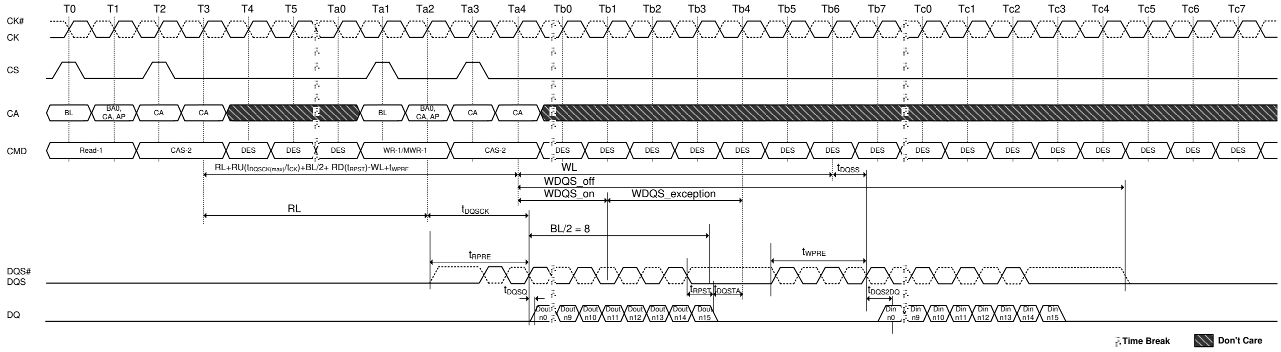
Table 13. DQS turn around parameter

Parameter	Description	Max	Unit	Note
t_{DQSTA}	Turn-around time RDQS to WDQS for WDQS control case	TBD	tCK(avg)	1



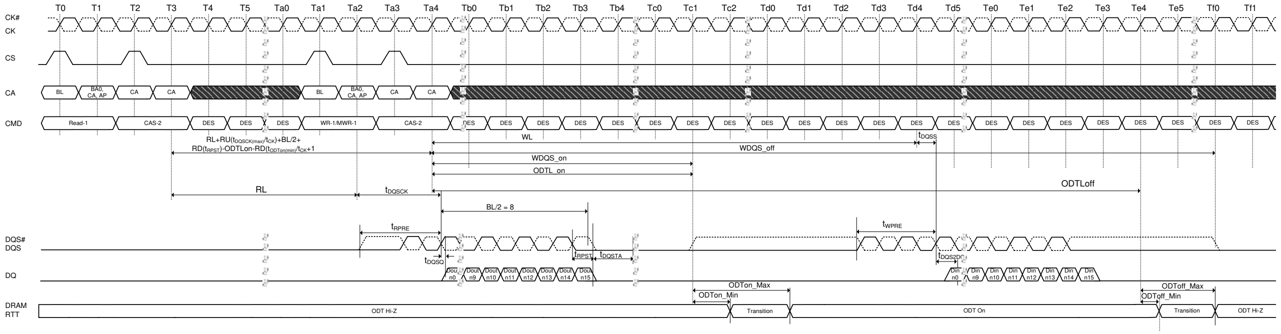
Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. DRAM RTT is only applied when ODT is enabled (MR11 OP[2:0] is not 000B)

Figure 19. Burst Write Operation



Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK
2. Dout n = data-out from column n and Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

Figure 20. Burst Read followed by Burst Write or Burst Mask Write (ODT Disable)



Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

Figure 21. Burst Read followed by Burst Write or Burst Mask Write (ODT Enable)

Pull Up/Pull Down Driver Characteristics and Calibration

Table 14. Pull-down Driver Characteristics, with ZQ Calibration

RONPD,nom	Resistor	Min	Nom	Max	Unit
40 Ohm	RON40PD	0.9	1	1.1	RZQ/6
48 Ohm	RON48PD	0.9	1	1.1	RZQ/5
60 Ohm	RON60PD	0.9	1	1.1	RZQ/4
80 Ohm	RON80PD	0.9	1	1.1	RZQ/3
120 Ohm	RON120PD	0.9	1	1.1	RZQ/2
240 Ohm	RON240PD	0.9	1	1.1	RZQ/1

Notes:

1. All value are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%.

Table 15. Pull-Up Characteristics, with ZQ Calibration

VOHPU,nom	VOH,nom(mV)	Min	Nom	Max	Unit
VDDQ x 0.5	300	0.9	1	1.1	VOH,nom
VDDQ x 0.6	360	0.9	1	1.1	VOH,nom

Notes:

1. All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%.
2. VOH,nom (mV) values are based on a nominal V_{DDQ} = 0.6V.

Table 16. Valid Calibration Points

VOHPU,nom	ODT Value					
	240	120	80	60	48	40
VDDQ x 0.5	VALID	VALID	VALID	VALID	VALID	VALID
VDDQ x 0.6	DNU	VALID	DNU	VALID	DNU	DNU

Notes:

1. Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2. If the VOH(nom) calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use

On Die Termination for Command/Address Bus

ODT (On-Die Termination) is a feature of the LPDDR4X SDRAM that allows the SDRAM to turn on/off termination resistance for CK, CK#, CS and CA[5:0] signals without the ODT control pin.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting.

A simple functional representation of the DRAM ODT feature is shown below.

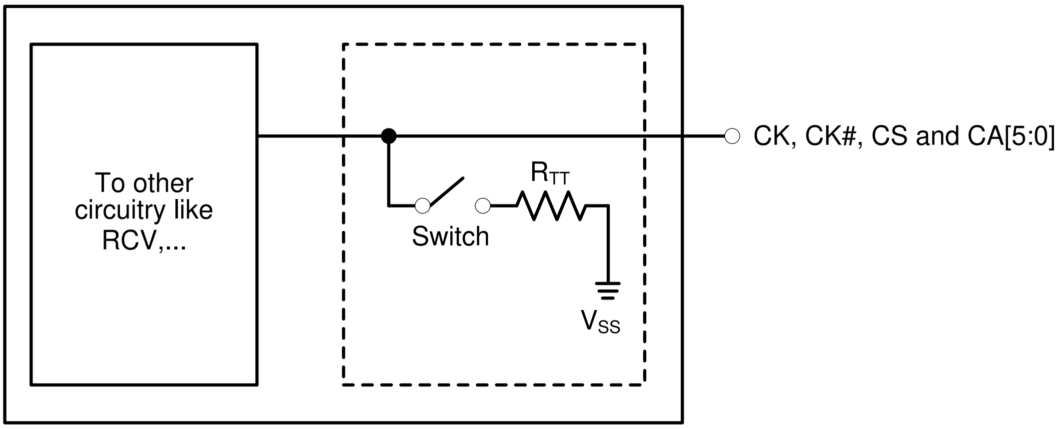


Figure 22. Functional Representation of CA ODT

ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK, CK#, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK, CK#, CS and CA[5:0] signals. Generally, only one termination load will be present even if multiple devices are sharing the command signals. In contrast to LPDDR4X where the ODT_CA input is used in combination with mode registers, LPDDR4X uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In a multi rank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

Table 17. Command Bus ODT State

ODTE-CA MR11[6:4]	**ODTD-CA MR22[5]**	**ODTF-CK MR22[3]**	**ODTF-CS MR22[4]**	**ODT State for CA**	**ODT State for CK/CK#**	**ODT State for CS**
Disabled[1]	Valid[2]	Valid[2]	Valid[2]	Off	Off	Off
Valid[2]	0	0	0	On	On	On
Valid[2]	0	0	1	On	On	Off
Valid[2]	0	1	0	On	Off	On
Valid[2]	0	1	1	On	Off	Off
Valid[2]	1	0	0	Off	On	On
Valid[2]	1	0	1	Off	On	Off
Valid[2]	1	1	0	Off	Off	On
Valid[2]	1	1	1	Off	Off	Off

Notes:

1. Default Value.
2. “Valid” means “0 or 1”.

ODT Mode Register and ODT Characteristics

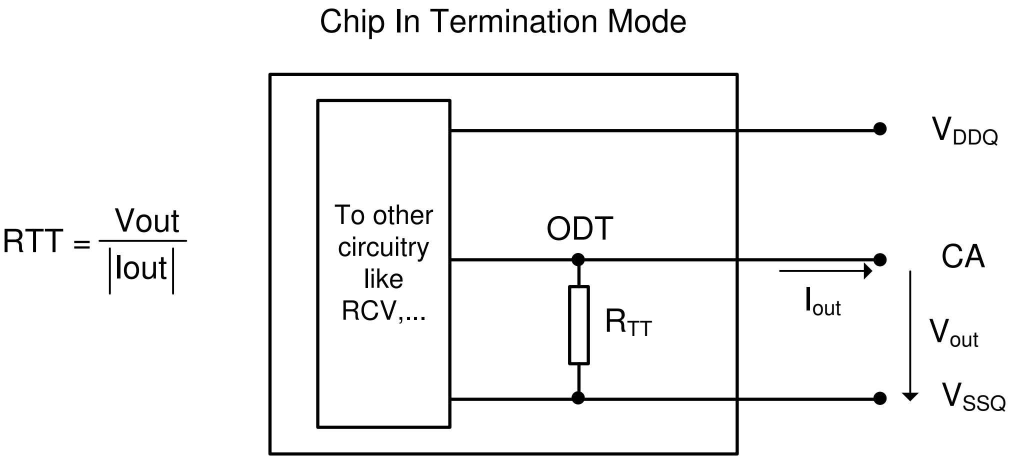


Figure 23. On Die Termination for CA

Table 18. ODT DC Electrical Characteristics for Command/Address Bus

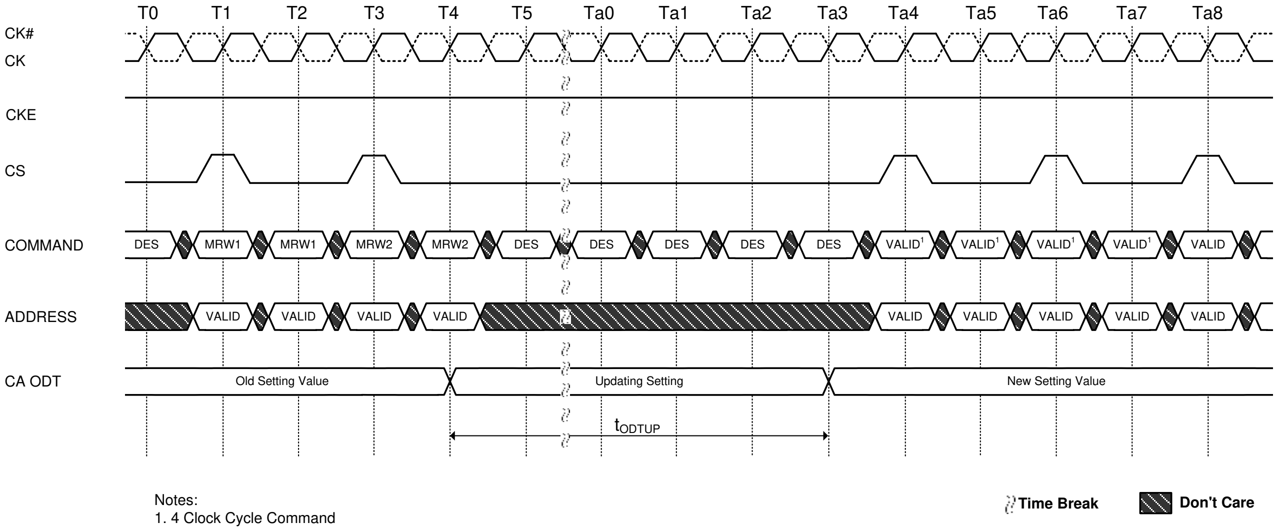
(Assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration)

MR11 OP[6:4]	RTT	Vout	Min.	Nom.	Max.	Unit	Note
001	240Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ	1,2
010	120Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/2	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/2	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/2	1,2
011	80Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/3	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/3	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/3	1,2
100	60Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/4	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/4	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/4	1,2
101	48Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/5	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/5	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/5	1,2
110	40Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/6	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/6	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/6	1,2
Mismatch CA-CA within clk group		$0.5 \times V_{DDQ}$	-	-	2	%	1,2,3

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.50 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75 x VDDQ and 0.2 x VDDQ.
3. CA to CA mismatch within clock group (CA, CS) variation for a given component including CK and CK# (characterized).

$$\text{CA - CA mismatch} = \frac{\text{RODT (max) - RODT (min)}}{\text{RODT (avg)}}$$



Notes:
1. 4 Clock Cycle Command

Figure 24. ODT for Command/Address setting update timing in 4 Clock Cycle Command

On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR4X SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write or Mask Write operation.

The ODT feature is off and cannot be supported in Power Down and Self Refresh modes.

A simple functional representation of the DRAM ODT feature is shown below.

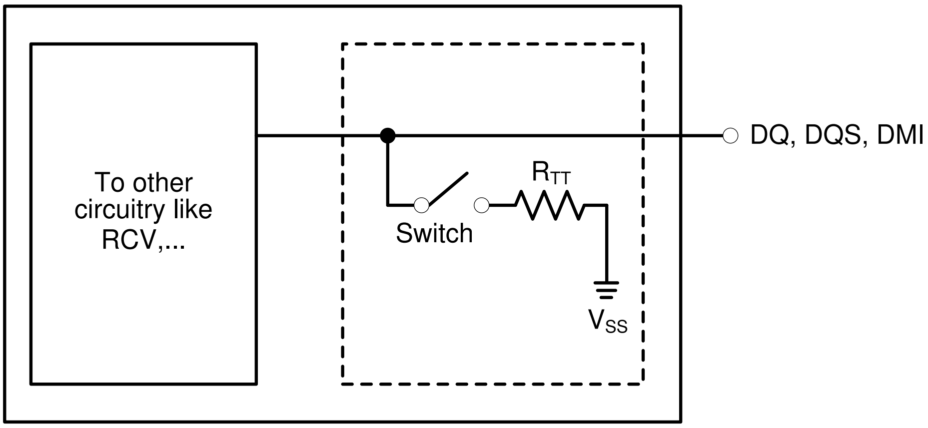


Figure 25. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the Write-1 or Mask Write-1 command and other mode register control information. The value of RTT is determined by the settings of Mode Register bits.

ODT Mode Register

The ODT Mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP[2:0] = 0.

Asynchronous ODT

When ODT Mode is enabled in MR11 OP[2:0], DRAM ODT is always Hi-Z. DRAM ODT feature is automatically turned ON asynchronously based on the Write-1 or Mask Write-1 command that DRAM samples. After the write burst is complete, DRAM ODT featured is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled:

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max

ODTLon is a synchronous parameter and it is the latency from CAS-2 command to tODTon reference.
ODTLon latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLon latency.

Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum RTT turn on time (tODTon,max) is the point in time when the ODT resistance is fully on.

tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from CAS-2 command.

ODTLoff is a synchronous parameter and it is the latency from CAS-2 command to tODToff reference.
ODTLoff latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLoff latency.

Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance.

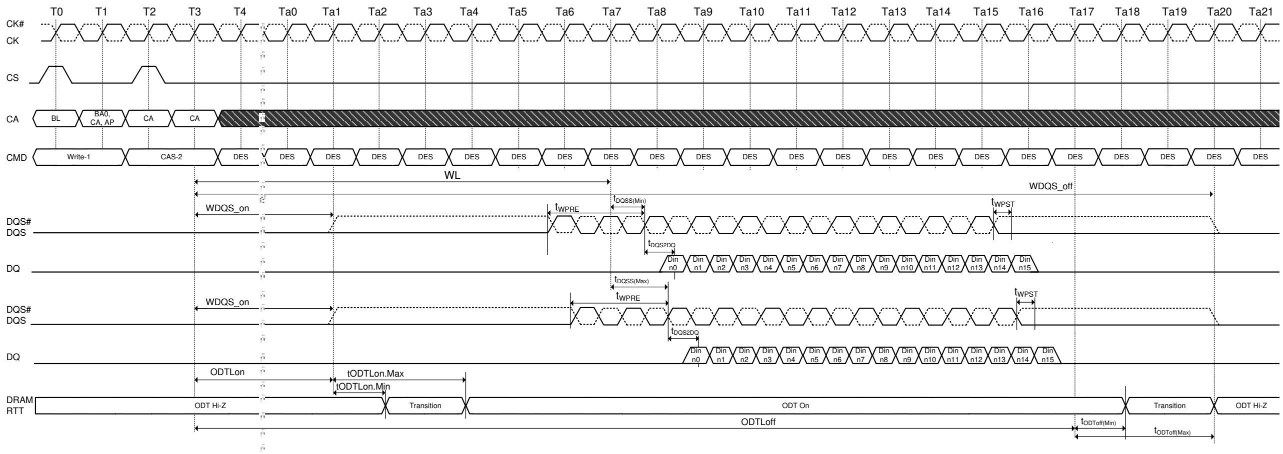
Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance.

tODToff,min and tODToff,max are measured once ODTLoff latency is satisfied from CAS-2 command.

Table 19. ODTLon and ODTLoff Latency

ODTLon Latency[1] tWPRE = 2tCK		ODTLoff Latency[2]		Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz] (≦)
WL Set “A”	WL Set "B"	WL Set "A"	WL Set "B"		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133
nCK	nCK	nCK	nCK	MHz	MHz

Notes:
1. ODTLon is referenced from CAS-2 command.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.



Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnm n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 26. Asynchronous ODTon/ODToff Timing

ODT during Write Leveling

If ODT is enabled in MR11 OP[2:0], in Write Leveling mode, DRAM always provides the termination on DQS/DQS# signals. DQ termination is always off in Write Leveling mode regardless.

Table 20. Termination Function in Write Leveling Mode

ODT Enabled in MR11	DQS/DQS# termination	DQ termination
Disabled	OFF	OFF
Enabled	ON	OFF

On Die Termination for DQ, DQS and DMI

On-Die Termination effective resistance RTT is defined by MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS and DQS# pins.

A functional representation of the on-die termination is shown below.

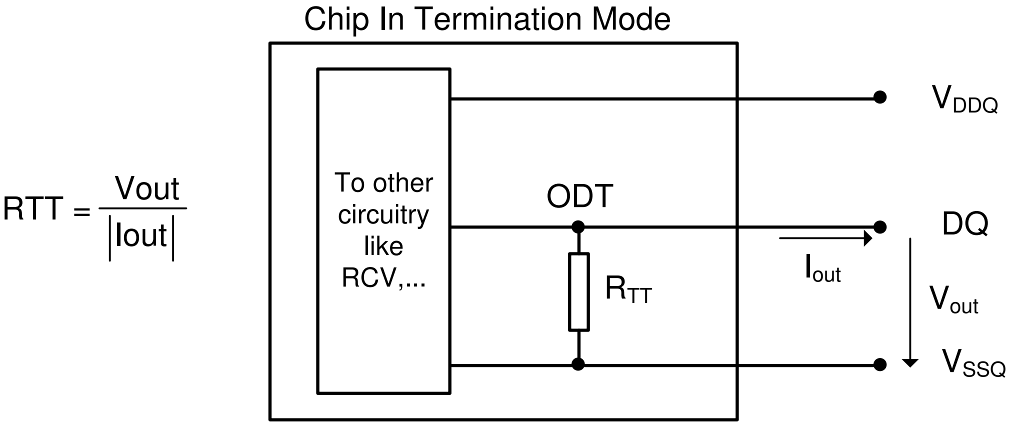


Figure 27. On Die Termination

Table 21. ODT DC Electrical Characteristics for DQ, DQS and DMI

(Assuming RZQ = 240 Ω ±1% over the entire operating temperature range after a proper ZQ calibration)

MR11 OP[2:0]	RTT	Vout	Min.	Nom.	Max.	Unit	Note
001	240Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ	1,2
010	120Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/2	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/2	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/2	1,2
011	80Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/3	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/3	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/3	1,2
100	60Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/4	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/4	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/4	1,2
101	48Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/5	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/5	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/5	1,2
110	40Ω	$V_{OL}dc = 0.2 \times V_{DDQ}$	0.8	1	1.1	RZQ/6	1,2
		$V_{OM}dc = 0.5 \times V_{DDQ}$	0.9	1	1.1	RZQ/6	1,2
		$V_{OH}dc = 0.75 \times V_{DDQ}$	0.9	1	1.3	RZQ/6	1,2
Mismatch DQ-DQ within byte		$0.5 \times V_{DDQ}$	-	-	2	%	1,2,3

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the section on voltage and temperature sensitivity.
2. Pull-down ODT resistors are recommended to be calibrated at 0.75 x VDDQ and 0.2 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75 x VDDQ and 0.1 x VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS and DQS# (characterized).

$$\text{DQ - DQ mismatch} = \frac{\text{RODT (max) - RODT (min)}}{\text{RODT (avg)}}$$

Output Driver and Termination Register Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits are widen according to the tables below.

Table 22. Output Driver and Termination Register Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
RONPD	0.5 x V_{DDQ}	90-(dRondT x |ΔT|)- (dRondV x |ΔV|)	110+(dRondT x |ΔT|)+ (dRondV x |ΔV|)	%	1,2
VOHPU	0.5 x V_{DDQ}	90-(dVOHdT x |ΔT|)- (dVOHdV x |ΔV|)	110+(dVOHdT x |ΔT|)+ (dVOHdV x |ΔV|)	%	1,2,5
RTT(I/O)	0.5 x V_{DDQ}	90-(dRondT x |ΔT|)- (dRondV x |ΔV|)	110+(dRondT x |ΔT|)+ (dRondV x |ΔV|)	%	1,2,3
RTT(In)	0.5 x V_{DDQ}	90-(dRondT x |ΔT|)- (dRondV x |ΔV|)	110+(dRondT x |ΔT|)+ (dRondV x |ΔV|)	%	1,2,4

Notes:

1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
2. dRONdT, dRONdV, dVOHdT, dVOHdV, dRTTdV, and dRTTdT are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI and the input pins such as CK, CA, and CS.
4. Refer to Pull Up/Pull Down Driver Characteristics for VOHPU.

Table 23. Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0	0.75	%/°C
dRONdV	RON Voltage Sensitivity	0	0.2	%/mV
dVOHdT	VOH Temperature Sensitivity	0	0.75	%/°C
dVOHdV	VOH Voltage Sensitivity	0	0.35	%/mV
dRTTdT	RTT Temperature Sensitivity	0	0.75	%/°C
dRTTdV	RTT Voltage Sensitivity	0	0.2	%/mV

Table 24. Asynchronous ODT Turn On and Turn Off Timing

Parameter	800 - 2133 MHz	Unit
tODTon, min	1.5	ns
tODTon, max	3.5	ns
tODToff, min	1.5	ns
tODToff, max	3.5	ns

Table 25. ODT CA AC Timing

Symbol	Parameter	Min	Max	Unit
tODTUP	ODT CA Value Update Time	RU(TBDns/tCK(AVG))	-	

Multi-Purpose Command (MPC)

LPDDR4X-SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW.

The following MPC commands must be followed by a CAS-2 command:
- Write FIFO
- Read FIFO
- Read DQ Calibration

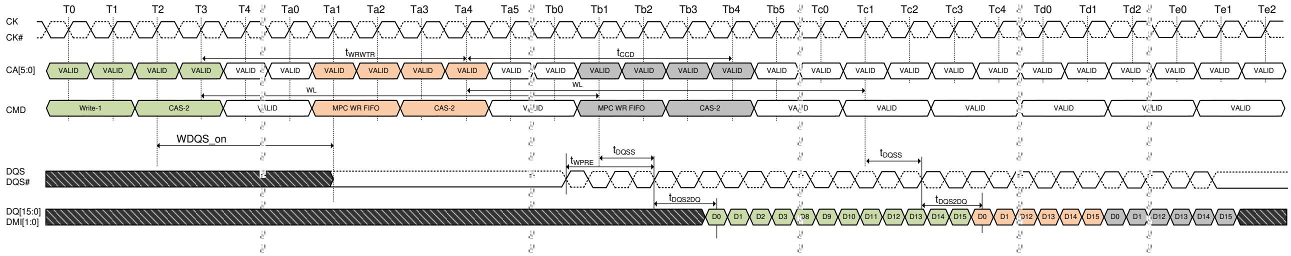
All other MPC-1 commands do not require a CAS-2 command, including:
- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

Table 26. MPC Command Definition

	Command Pins			**CA Pins**							
Command	**CKE**		**CS**	**CA0**	**CA1**	**CA2**	**CA3**	**CA4**	**CA5**	**CK Edge**	**Note**
	CK(n-1)	**CK(n)**									
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	R1	1,2
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2	

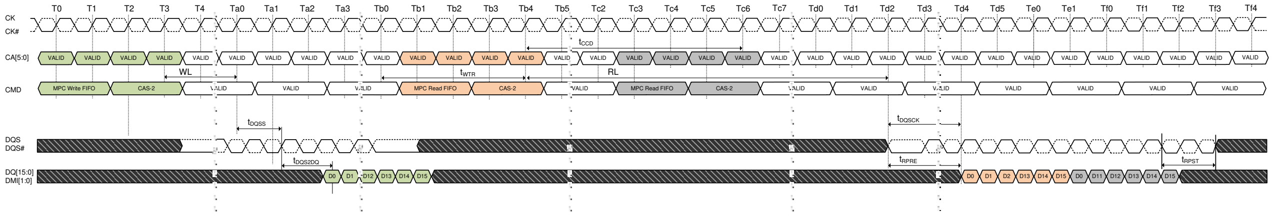
Function	**Operand**	**Data**	**Note**
Training Modes	OP[6:0]	0XXXXXXB: NOP 1000001B: RD FIFO: RD FIFO supports only BL16 operation 1000011B: RD DQ Calibration (MR32/MR40) 1000101B: RFU 1000111B: WR FIFO: WR FIFO supports only BL16 operation 1001001B: RFU 1001011B: Start DQS Osc 1001101B: Stop DQS Osc 1001111B: ZQCal Start 1010001B: ZQCal Latch All Others: Reserved	1,2,3

Notes:
1. See command truth table for more information.
2. MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.
3. Write FIFO and Read FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].



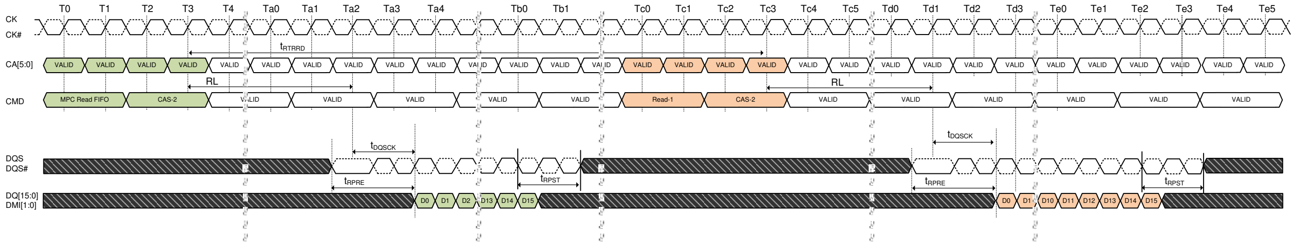
NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.
   The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR.
   See Write Training section for more information on FIFO pointer behavior.

Figure 28. MPC [Write FIFO] Operation : tWPRE=2nCK, tWPST=0.5nCK



NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC-1 [WR-FIFO] is tWRWTR.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to The 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data.
   See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers.
   See Write Training section for more information on DMI behavior.

Figure 29. MPC [RD FIFO] Read Operation: tWPRE=2nCK, tWPST=0.5nCK, tRPRE=toggling, tRPST=1.5nCK



NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC-1 [RD-FIFO] command to Read is tRTRRD.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to The 1st FIFO and continue advancing.
   If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data.
   See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

Figure 30. MPC [RD FIFO] Operation : tRPRE=toggling, tRPST=1.5nCK

Table 27. Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Note
WR/MWR	MPC [WR FIFO]	tWRWTR	nCK	1
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
RD/MRR	MPC [WR FIFO]	tRTRRD	nCK	3
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [WR FIFO]	WR/MWR	Not Allowed	-	2
	MPC [WR FIFO]	tCCD	nCK	
	RD/MRR	Not Allowed	-	2
	MPC [RD FIFO]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
	MPC [RD DQ Calibration]	Not Allowed	-	2
MPC [RD FIFO]	WR/MWR	tRTRRD	nCK	3
	MPC [WR FIFO]	tRTW	-	4
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	tCCD	nCK	
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [RD DQ Calibration]	WR/MWR	tRTRRD	nCK	3
	MPC [WR FIFO]	tRTRRD	nCK	3
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tCCD	nCK	

Notes:

1. tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + max(RU(7.5ns/tCK),8nCK)
2. No commands are allowed between MPC [WR FIFO] and MPC-1 [RD FIFO] except MRW commands related to training parameters.
3. tRTRRD = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) + max(RU(7.5ns/tCK),8nCK)
4. tRTW:
   - In Case of DQ ODT Disable MR11 OP[2:0] = 000B:
     RL+RU(tDQSCK(max)/ tCK) +BL/2- WL+tWPRE+RD(tRPST)
   - In Case of DQ ODT Enable MR11 OP[2:0] ≠ 000B:
     RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon,min/tCK) + 1

VREF Current Generator (VRCG)

LPDDR4X SDRAM VREF current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal VREF(DQ) and VREF(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown below.

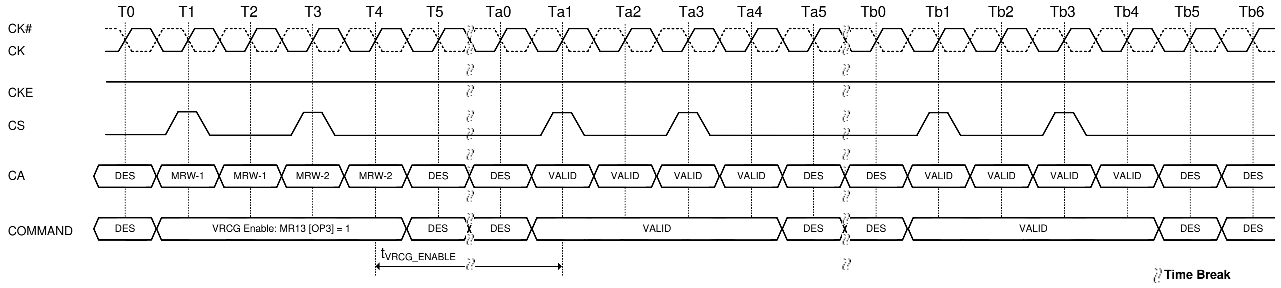


Figure 31. VRCG Enable timing

VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown below.

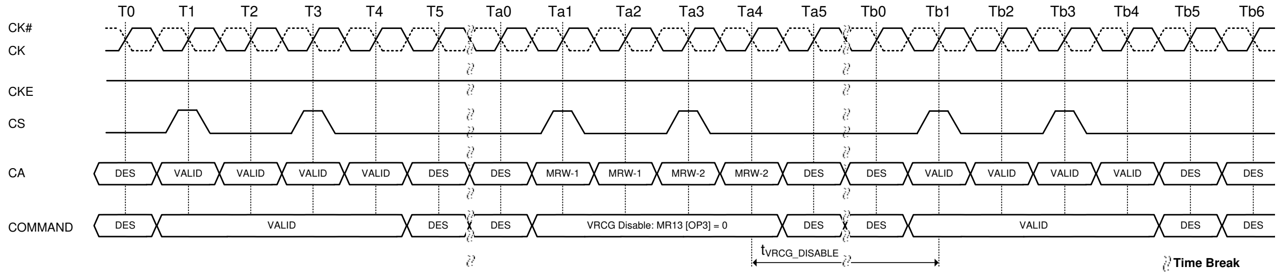


Figure 32. VRCG Disable timing

Note that LPDDR4X SDRAM devices support VREF(CA) and VREF(DQ) range and value changes without enabling VRCG high current mode.

Table 28. VRCG Enable/Disable Timing

Symbol	Parameter	Min	Max	Unit
tVRCG_ENABLE	VREF high current mode enable time	-	200	ns
tVRCG_DISABLE	VREF high current mode disable time	-	100	ns

CA VREF Training

The DRAM internal CA VREF specification parameters are voltage operating range, step size, VREF set tolerance, VREF step time and VREF valid level.

The voltage operating range specifies the minimum required VREF setting range for LPDDR4X DRAM devices. The minimum range is defined by VREFmax and VREFmin.

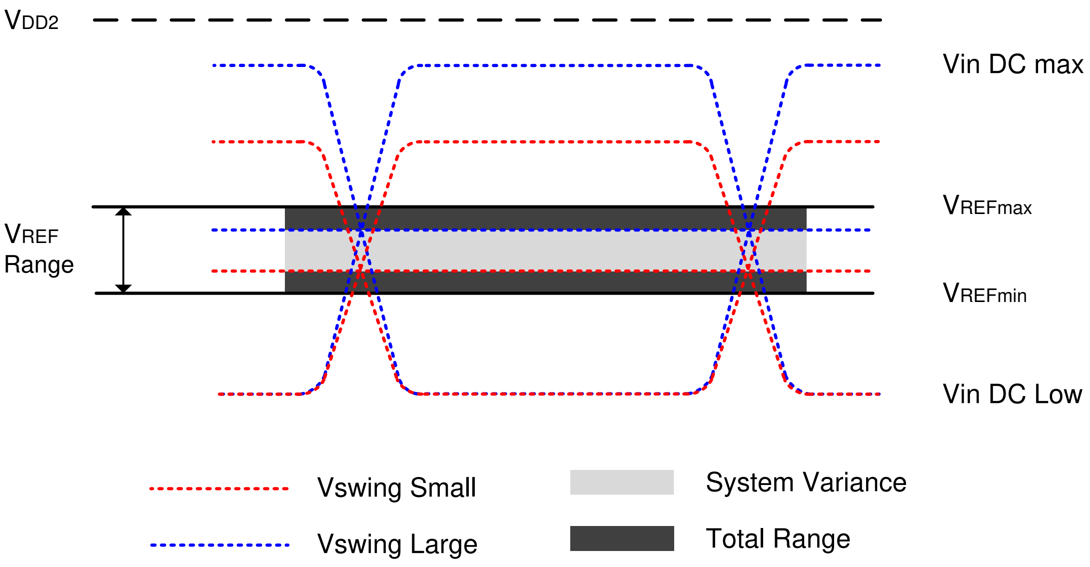


Figure 33. VREF operating range (VREFmin, VREFmax)

The VREF step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n.

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VREF values for a specified range.

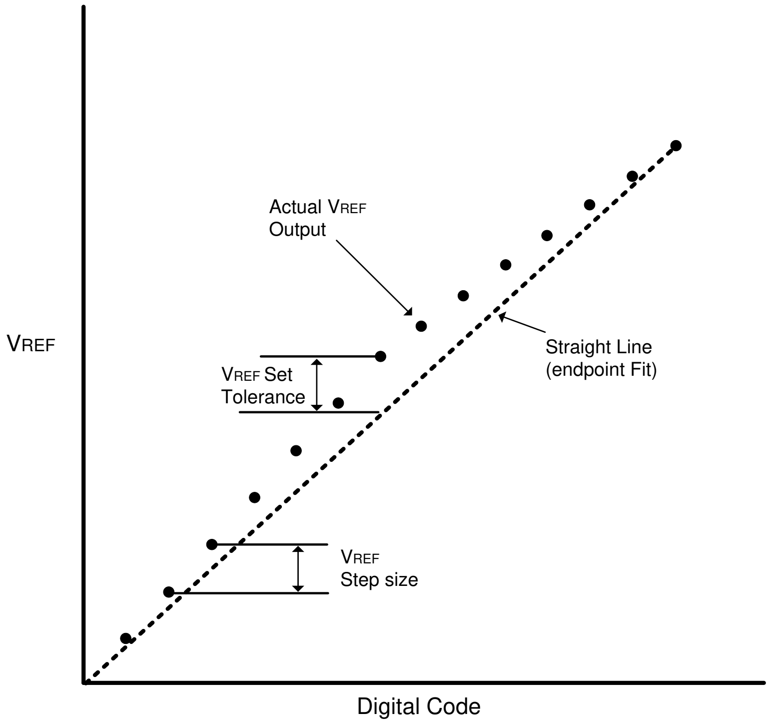


Figure 34. Example of VREF set tolerance (max case only shown) and step size

The VREF increment/decrement step times are define by VREF_time-short, Middle and long. The VREF_time-short, VREF_time-Middle and VREF_time-long is defined from TS to TE as shown below, where TE is referenced to when the VREF voltage is at the final DC level within the VREF valid tolerance(VREF_val_tol).

The VREF valid level is defined by VREF_val tolerance to qualify the step time TE (see the following figures). This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

VREF_time-Short is for a single step size increment/decrement change in VREF voltage.

VREF_time-Middle is at least 2 step sizes increment/decrement change within the same VREFCA range in VREF voltage.

VREF_time-Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.

TS - is referenced to MRS command clock
TE - is referenced to the VREF_val_tol

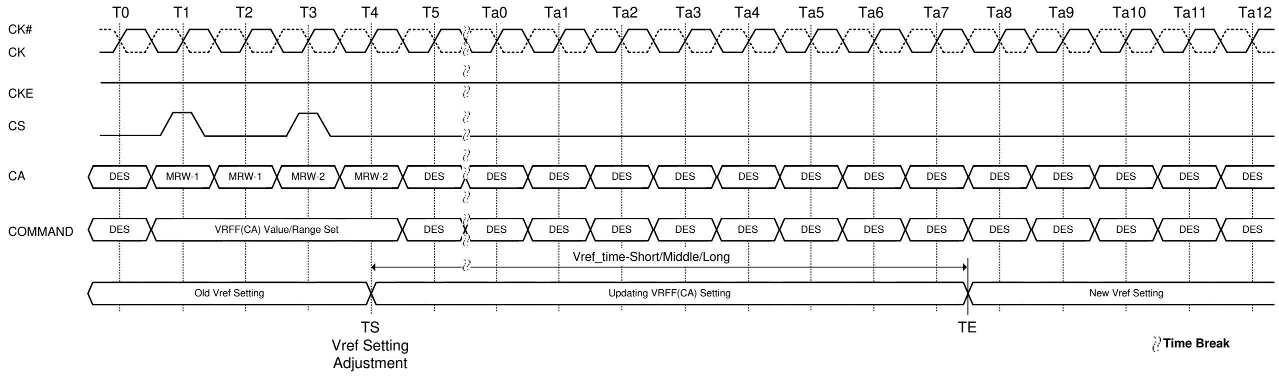


Figure 35. VREF_time for Short, Middle and Long Timing Diagram

The MRW command to the mode register bits are as follows.

MR12 OP[5:0] : VREF(CA) Setting
MR12 OP[6] : VREF(CA) Range

The minimum time required between two VREF MRS commands is VREF_time-short for single step and VREF_time-Middle for a full voltage range step.

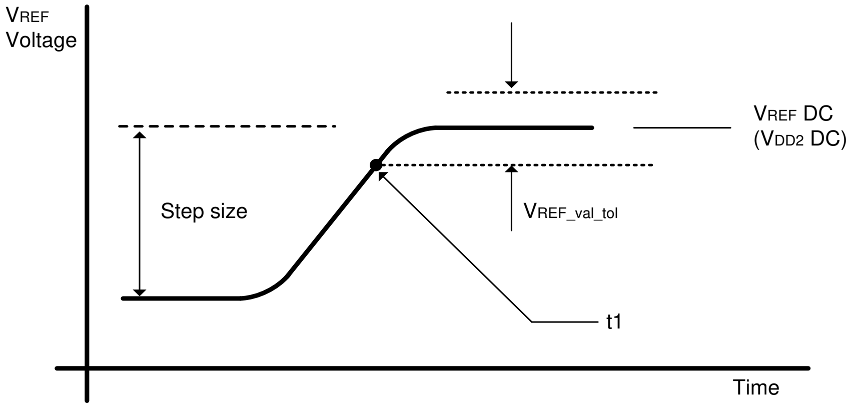


Figure 36. VREF step single step size increment case

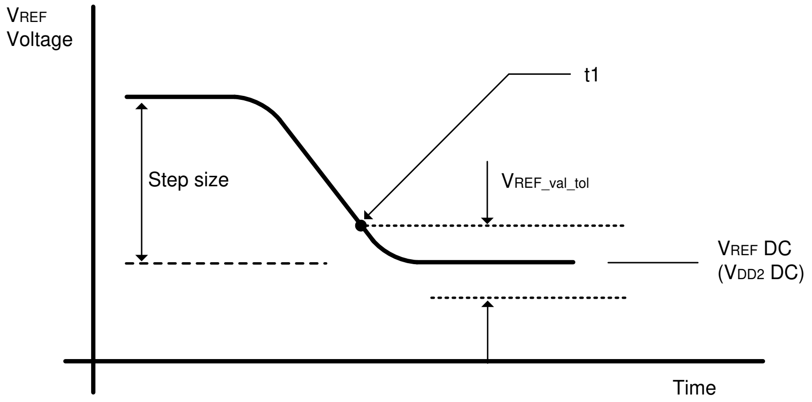


Figure 37. VREF step single step size decrement case

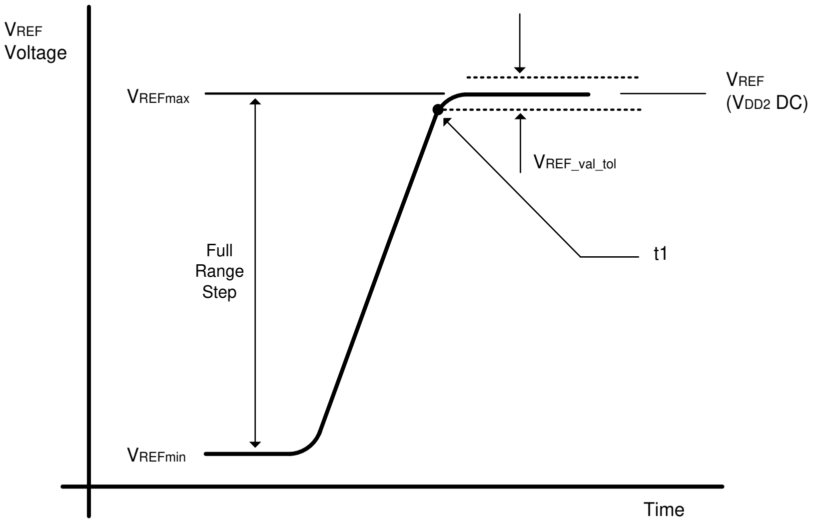


Figure 38. VREF full step from VREFmin to VREFmax case

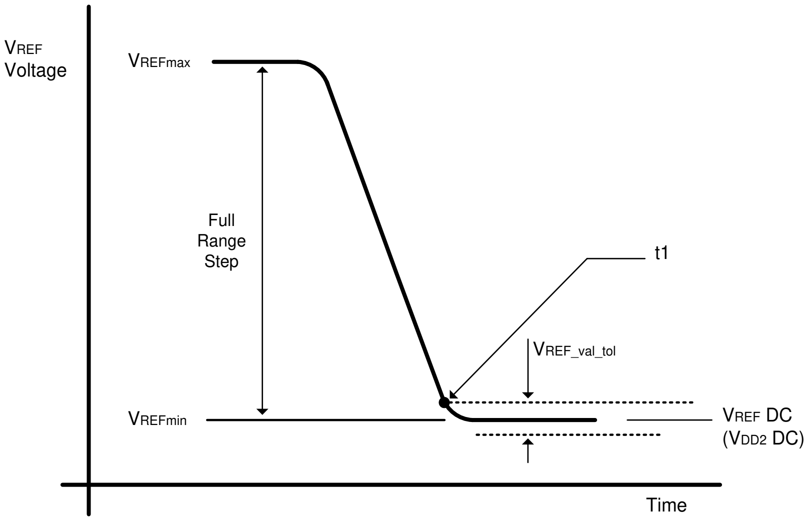


Figure 39. VREF full step from VREFmax to VREFmin case

The following table contains the CA internal VREF specification that will be characterized at the component level for compliance.

Table 29. CA Internal VREF Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
VREF_max_R0	VREF Max operating point Range0	-	-	44.9%	VDDQ	1,11
VREF_min_R0	VREF Min operating point Range0	15%	-	-	VDDQ	1,11
VREF_max_R1	VREF Max operating point Range1	-	-	62.9%	VDDQ	1,11
VREF_min_R1	VREF Min operating point Range1	32.9%	-	-	VDDQ	1,11
VREF_step	VREF Step size	0.5%	0.6%	0.7%	VDDQ	2
VREF_set_tol	VREF Set Tolerance	-11	0	11	mV	3,4,6
		-1.1	0	1.1	mV	3,5,7
VREF_time_Short	VREF Step Time	-	-	100	ns	8
VREF_time_Middle		-	-	200	ns	12
VREF_time_Long		-	-	250	ns	9
VREF_time_weak		-	-	1	ms	13,14
VREF_val_tol	VREF Valid tolerance	-0.1%	0%	0.1%	VDDQ	10

Notes:

1. VREF DC voltage referenced to VDD2_DC.
2. VREF step size increment/decrement range. VREF at DC level.
3. VREF_new = VREF_old + n x VREF_step; n= number of steps; if increment use "+"; if decrement use "-".
4. The minimum value of VREF setting tolerance = VREF_new – 11mV. The maximum value of VREF setting tolerance = VREF_new + 11mV. For n>4.
5. The minimum value of VREF setting tolerance = VREF_new – 11mV. The maximum value of VREF setting tolerance = VREF_new + 11mV. For n≤ 4.
6. Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
7. Measured by recording the min and max values of the VREF output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VREF output settings to that line.
8. Time from MRS command to increment or decrement one step size for VREF.
9. Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR12 OP[6].
12. Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFCA range.
13. Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.
14. VREF_time_weak covers all VREF(CA) Range and Value change conditions are applied to VREF_time_Short/Middle/Long.

DQ VREF Training

The DRAM internal DQ VREF specification parameters are voltage operating range, step size, VREF set tolerance, VREF step time and VREFvalid level.

The voltage operating range specifies the minimum required VREF setting range for LPDDR4X DRAM devices. The minimum range is defined by VREFmax and VREFmin.

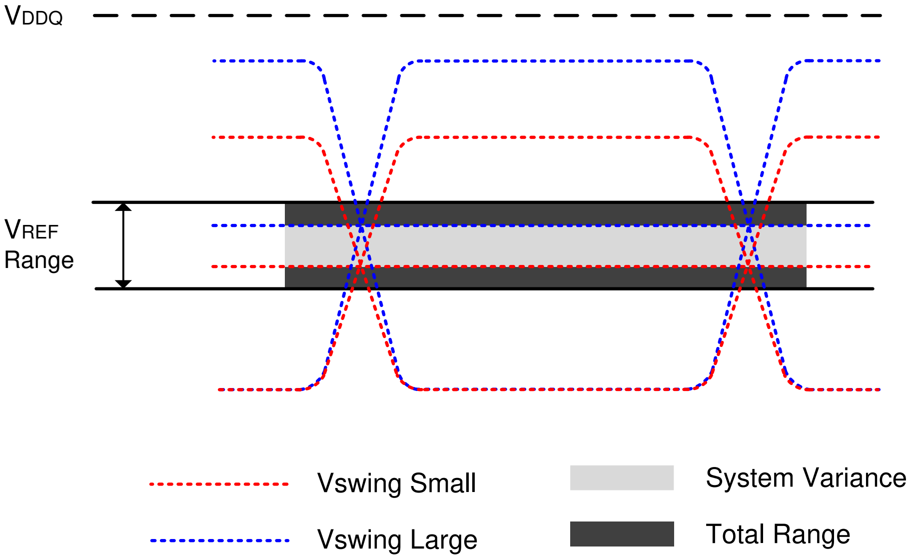


Figure 40. VREF operating range(VREFmin, VREFmax)

The VREF step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n.

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VREF values for a specified range.

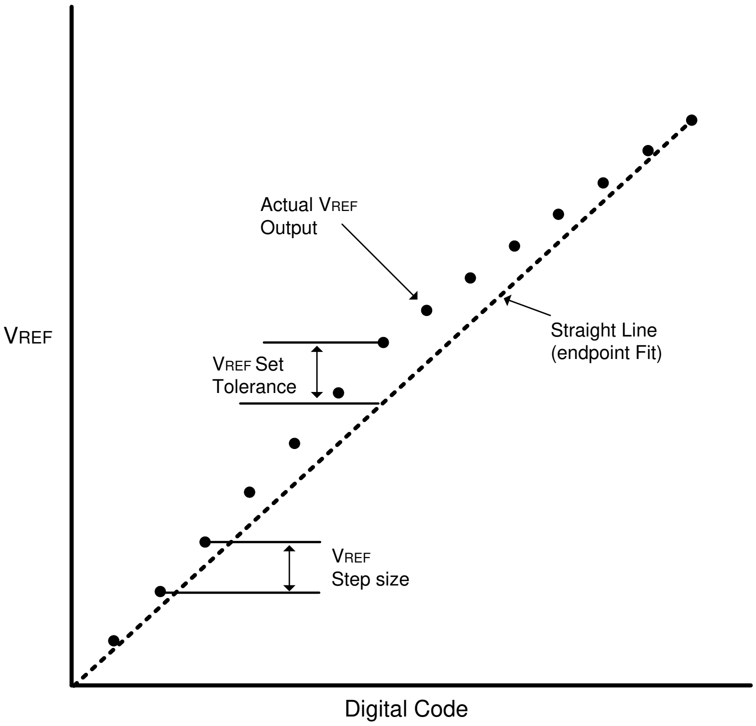


Figure 41. Example of VREF set tolerance (max case only shown) and step size

The VREF increment/decrement step times are define by VREF_time-short, Middle and long. The VREF_time-short, VREF_time-Middle and VREF_time-long is defined from TS to TE as shown below, where TE is referenced to when the VREF voltage is at the final DC level within the VREF valid tolerance(VREF_val_tol).

The VREF valid level is defined by VREF_val tolerance to qualify the step time TE (see the following figures). This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

VREF_time-Short is for a single step size increment/decrement change in VREF voltage.

VREF_time-Middle is at least 2 step sizes increment/decrement change within the same VREFCA range in VREF voltage.

VREF_time-Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFCA Range in VREF voltage.

TS - is referenced to MRS command clock
TE - is referenced to the VREF_val_tol

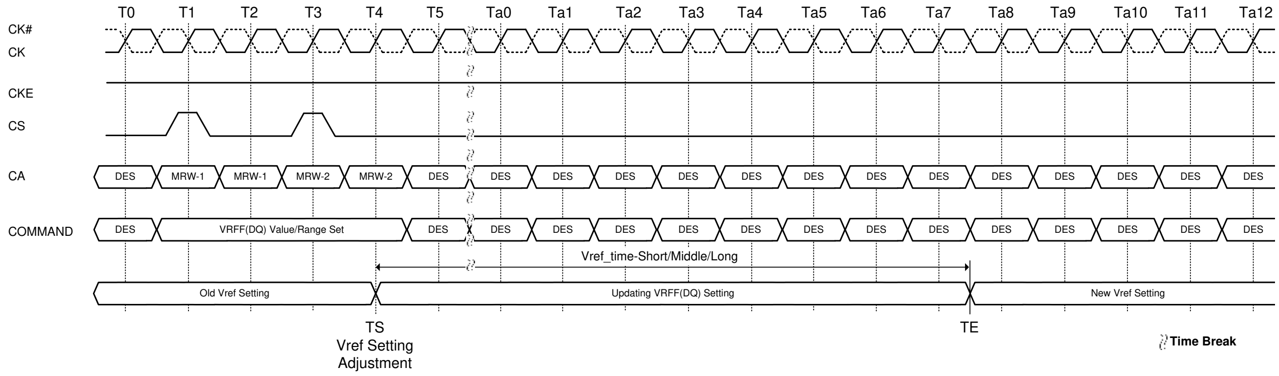


Figure 42. VREF_time for Short, Middle and Long Timing Diagram

The MRW command to the mode register bits are as follows.

MR14 OP[5:0] : VREF(DQ) Setting
MR14 OP[6] : VREF(DQ) Range

The minimum time required between two VREF MRS commands is VREF_time-short for single step and VREF_time-Middle for a full voltage range step.

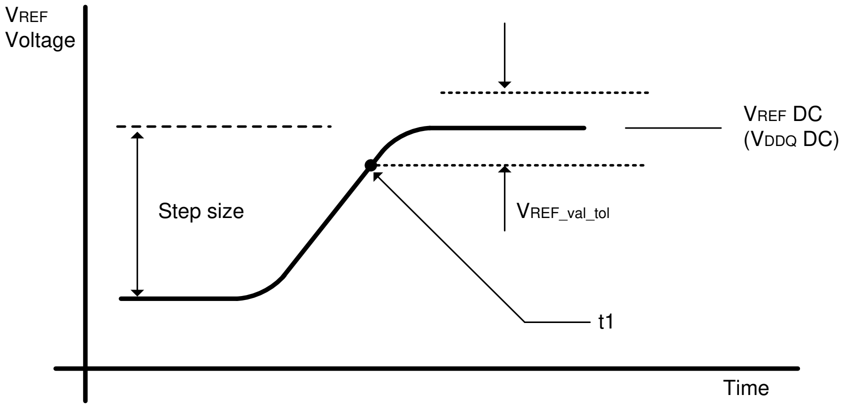


Figure 43. VREF step single step size increment case

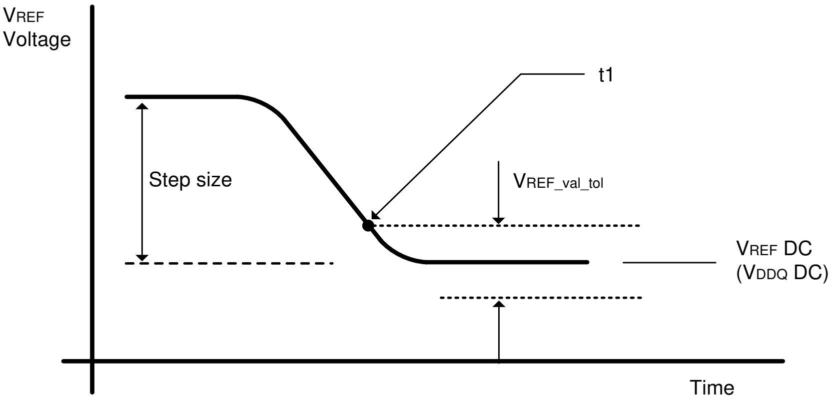


Figure 44. VREF step single step size decrement case

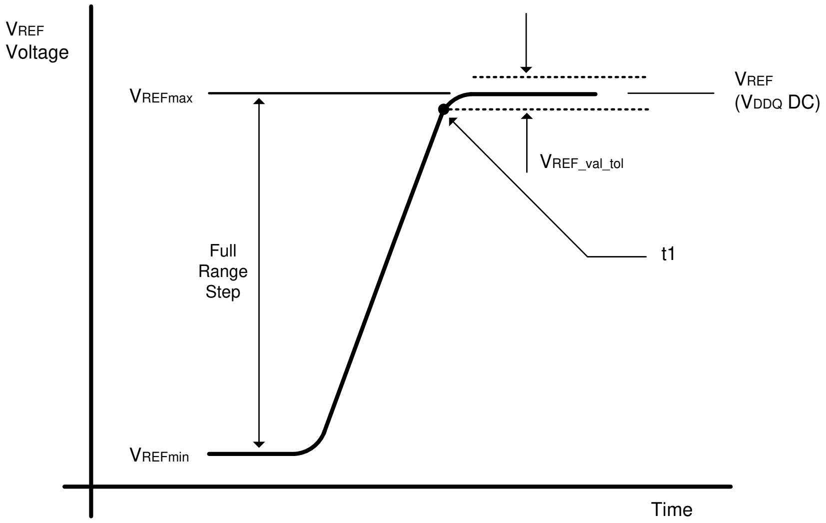


Figure 45. VREF full step from VREFmin to VREFmax case

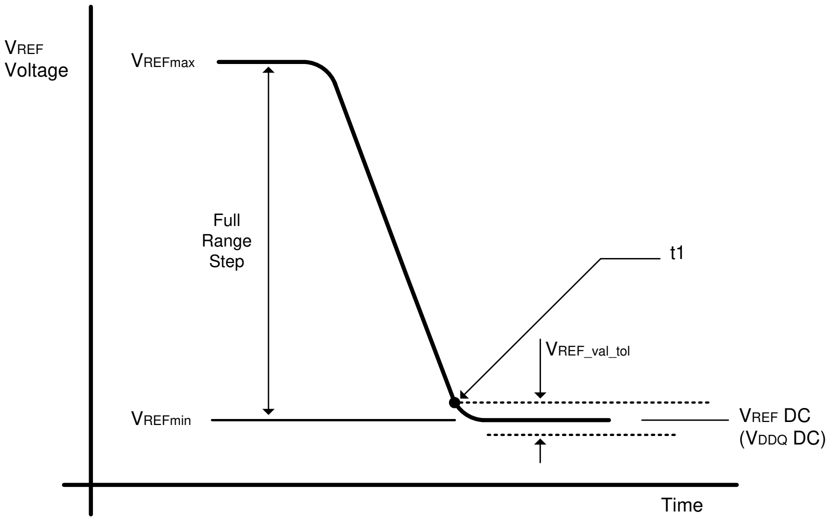


Figure 46. VREF full step from VREFmax to VREFmin case

The following table contains the DQ internal VREF specification that will be characterized at the component level for compliance.

Table 30. DQ Internal VREF Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
VREF_max_R0	VREF Max operating point Range0	-	-	44.9%	VDDQ	1,11
VREF_min_R0	VREF Min operating point Range0	15%	-	-	VDDQ	1,11
VREF_max_R1	VREF Max operating point Range1	-	-	62.9%	VDDQ	1,11
VREF_min_R1	VREF Min operating point Range1	32.9%	-	-	VDDQ	1,11
VREF_step	VREF Step size	0.5%	0.6%	0.7%	VDDQ	2
VREF_set_tol	VREF Set Tolerance	-11	0	11	mV	3,4,6
		-1.1	0	1.1	mV	3,5,7
VREF_time_Short	VREF Step Time	-	-	100	ns	8
VREF_time_Middle		-	-	200	ns	12
VREF_time_Long		-	-	250	ns	9
VREF_time_weak		-	-	1	ms	13,14
VREF_val_tol	VREF Valid tolerance	-0.1%	0%	0.1%	VDDQ	10

Notes:

1. VREF DC voltage referenced to VDDQ_DC.
2. VREF step size increment/decrement range. VREF at DC level.
3. VREF_new = VREF_old + n x VREF_step; n= number of steps; if increment use "+"; if decrement use "-".
4. The minimum value of VREF setting tolerance = VREF_new – 11mV. The maximum value of VREF setting tolerance = VREF_new + 11mV. For n>4.
5. The minimum value of VREF setting tolerance = VREF_new – 11mV. The maximum value of VREF setting tolerance = VREF_new + 11mV. For n≤ 4.
6. Measured by recording the min and max values of the VREF output over the range, drawing a straight line between those points and comparing all other VREF output settings to that line.
7. Measured by recording the min and max values of the VREF output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other VREF output settings to that line.
8. Time from MRS command to increment or decrement one step size for VREF.
9. Time from MRS command to increment or decrement VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. VREF valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR14 OP[6].
12. Time from MRS command to increment or decrement more than one step size up to a full range of VREF voltage within the same VREFDQ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.
14. VREF_time_weak covers all VREF(DQ) Range and Value change conditions are applied to VREF_time_Short/Middle/Long. gg

Mode Register Definition

The table listed below shows the mode registers for LPDDR4X SDRAM. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Mode Register Assignment and Definition

Table below shows the mode registers. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Table 31. Mode Register Assignments

MR#	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	CATR	RFU	RFU	RZQI		RFU	Latency	Refresh
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	Reserved							
6	Reserved							
7	Reserved							
8	IO Width		Density				Type	
9	Reserved							
10	RFU							ZQ-Reset
11	Reserved	CA ODT			Reserved	DQ ODT		
12	RFU	VR-CA	VREF(CA)					
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(DQ)	VREF(DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count - LSB							
19	DQS Oscillator Count - MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		
23	DQS interval timer run time setting							
24	TRR Mode	TRR Mode BAn			Unltd MAC	MAC Value		
25	PPR Resource							
26	RFU							
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing - SDRAM will ignore							
31	RFU							
32	DQ Calibration Pattern “A” (default = 5AH)							
33	RFU							
34	RFU							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							

Table 32. MR0 Register Information (MA[5:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CATR	RFU	RFU	RZQI		RFU	Latency	Refresh

Function	Type	Operand	Data	Notes
Refresh Mode	Read-only	OP[0]	0B : Both legacy & modified refresh mode supported 1B : Only modified refresh mode supported	
Latency Mode		OP[1]	0B : Device supports normal latency 1B : Reserved	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00B: RZQ Self-Test Not Supported 01B: ZQ pin may connect to VSSQ or float 10B: ZQ-pin may short to VDDQ 11B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ)	1~ 4
CATR (CA Terminating Rank)		OP[7]	0B: CA for this rank is not terminated 1B: Vendor specific	5

Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
   a. Completion of MPC ZQCAL Start command to either channel.
   b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.
   RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4X-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).
5. CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.

Table 33. MR1 Register Information (MA[5:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00B: BL=16 Sequential (default) 01B: BL=32 Sequential 10B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1
WR-PRE (WR Pre-amble Length)		OP[2]	0B: Reserved 1B: WR Pre-amble = 2 x tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0B: RD Pre-amble = Static (default) 1B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	000B: nWR = 6 (default) 001B: nWR = 10 010B: nWR = 16 011B: nWR = 20 100B: nWR = 24 101B: nWR = 30 110B: nWR = 34 111B: nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	0B: RD Post-amble = 0.5 x tCK (default) 1B: RD Post-amble = 1.5 x tCK	4,5,6

Notes:

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled. See Read and Write Latencies.
3. For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 34. Burst Sequence for Read

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes:

1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting burst address is on 64-bit (4n) boundaries.

Table 35. Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																														
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes:

1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting address is on 256-bit (16n) boundaries for Burst length 16.
3. The starting address is on 512-bit (32n) boundaries for Burst length 32.
4. C2-C3 shall be set to '0' for all Write operations.

Table 36. MR2 Register Information (MA[5:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Function	Type	Operand	Data	Notes
RL (Read latency)	Write-only	OP[2:0]	**RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0B)** 000B: RL=6, nRTP = 8 (Default) 001B: RL=10, nRTP = 8 010B: RL=14, nRTP = 8 011B: RL=20, nRTP = 8 100B: RL=24, nRTP = 10 101B: RL=28, nRTP = 12 110B: RL=32, nRTP = 14 111B: RL=36, nRTP = 16 **RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1B)** 000B: RL=6, nRTP = 8 001B: RL=12, nRTP = 8 010B: RL=16, nRTP = 8 011B: RL=22, nRTP = 8 100B: RL=28, nRTP = 10 101B: RL=32, nRTP = 12 110B: RL=36, nRTP = 14 111B: RL=40, nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	**WL Set "A" (MR2 OP[6]=0B)** 000B: WL=4 (Default) 001B: WL=6 010B: WL=8 011B: WL=10 100B: WL=12 101B: WL=14 110B: WL=16 111B: WL=18 **WL Set "B" (MR2 OP[6]=1B)** 000B: WL=4 001B: WL=8 010B: WL=12 011B: WL=18 100B: WL=22 101B: WL=26 110B: WL=30 111B: WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	0B: WL Set "A" (default) 1B: WL Set "B"	1,3,4
WR Lev (Write Leveling)		OP[7]	0B: Disabled (default) 1B: Enabled	2

Notes:

1. See Read and Write Latencies table for detail.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 37. Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit [MHz](>)	Upper Clock Frequency Limit [MHz](≦)	Notes
No DBI	w/DBI	Set A	Set B					
6	6	4	4	6	8	10	266	1,2,3, 4,5,6
10	12	6	8	10	8	266	533	
14	16	8	12	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	

Notes:

1. The device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3 OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set “A” and Set "B" is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set "A" should be used. When MR2 OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Pre- charge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Pre- charge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

Table 38. MR3 Register Information (MA[5:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	0B: VDDQ x 0.6 1B: VDDQ x 0.5 (default)	1,4
WR PST (WR Post-Amble Length)		OP[1]	0B: WR Post-amble = 0.5 x tCK (default) 1B: WR Post-amble = 1.5 x tCK	2,3,5
Post Package Repair Protection		OP[2]	0B: PPR protection disabled (default) 1B: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0B: Disabled (default) 1B: Enabled	2,3

Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. 1.5 x tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

Table 39. MR4 Register Information (MA[5:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000B: Low temperature operating limit exceeded 001B: 4x refresh 010B: 2x refresh 011B: 1x refresh (default) 100B: 0.5x refresh 101B: 0.25x refresh, no de-rating 110B: 0.25x refresh, with de-rating 111B: High temperature operating limit exceeded	1-4, 7-9
SR Abort (Self Refresh Abort)	Write	OP[3]	0B: Disable (default) 1B: Enable	9,10
PPRE (Post-package repair entry/exit)	Write	OP[4]	0B: Exit PPR mode (default) 1B: Enter PPR mode	5, 9
Thermal Offset (Vender Specific Function)	Write	OP[6:5]	00B: No offset, 0~5°C gradient (default) 01B: 5°C offset, 5~10°C gradient 10B: 10°C offset, 10~15°C gradient 11B: Reserved	
TUF (Temperature Update Flag)	Read	OP[7]	0B: No change in OP[2:0] since last MR4 read (default) 1B: Change in OP[2:0] since last MR4 read	6-8

Notes:

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011B corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1B, the device temperature is greater than 85 °C.
2. At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR4X- SDRAM will set OP[2:0]=110B.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000B or 111B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).
8. See the section on “temperature Sensor” for information on the recommended frequency of reading MR4.
9. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10. Self Refresh abort feature is available for higher density devices starting with 12Gb device.

MR5~7 (Reserved) (MA[5:0] = 05H-07H)

Table 40. MR8 Register Information (MA[5:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
IO Width		Density				Type	

Function	Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000B: 4Gb dual channel die / 2Gb single channel die 0001B: 6Gb dual channel die / 3Gb single channel die 0010B: 8Gb dual channel die / 4Gb single channel die 0011B: 12Gb dual channel die / 6Gb single channel die 0100B: 16Gb dual channel die / 8Gb single channel die 0101B: 24Gb dual channel die / 12Gb single channel die 0110B: 32Gb dual channel die / 16Gb single channel die 1100B: 2Gb dual channel die / 1Gb single channel die All Others: Reserved	
IO Width		OP[7:6]	00B: x16 (per channel) All Others: Reserved	

MR9 (Reserved) (MA[5:0] = 09H)

Table 41. MR10 Register Information (MA[5:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ-Reset

Function	Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	0B: Normal Operation (Default) 1B: ZQ Reset	1, 2

Notes:
1. See ZQCal Timing Parameters for calibration latency and timing.
2. If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

Table 42. MR11 Register Information (MA[5:0] = 0BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved	CA ODT			Reserved	DQ ODT		

Function	Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3

Notes:
1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 43. MR12 Register Information (MA[5:0] = 0CH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR-CA	VREF(CA)					

Function	Type	Operand	Data	Notes
VREF(CA) (VREF(CA) Setting)	Read / Write	OP[5:0]	000000B - 110010B: See table below All Others: Reserved	1,2,3, 5,6
VR-CA (VREF(CA) Range)		OP[6]	0B: VREF(CA) Range[0] enabled 1B: VREF(CA) Range[1] enabled (default)	1,2,4, 5,6

Notes:

1. This register controls the VREF(CA) levels. Refer to VREF Settings for Range[0] and Range[1] for actual voltage of VREF(CA).
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(CA) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(CA) training for more information.
4. A write to OP[6] switches the LPDDR4X-SDRAM between two internal VREF(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 44. VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR12	OP[5:0]	000000B: 15.0%	011010B: 30.5 %	000000B: 32.9%	011010B: 48.5%	1,2,3
		000001B: 15.6%	011011B: 31.1%	000001B: 33.5%	011011B: 49.1%	
		000010B: 16.2%	011100B: 31.7%	000010B: 34.1%	011100B: 49.7%	
		000011B: 16.8%	011101B: 32.3%	000011B: 34.7%	011101B: 50.3% (default)	
		000100B: 17.4%	011110B: 32.9%	000100B: 35.3%	011110B: 50.9%	
		000101B: 18.0%	011111B: 33.5%	000101B: 35.9%	011111B: 51.5%	
		000110B: 18.6%	100000B: 34.1%	000110B: 36.5%	100000B: 52.1%	
		000111B: 19.2%	100001B: 34.7%	000111B: 37.1%	100001B: 52.7%	
		001000B: 19.8%	100010B: 35.3%	001000B: 37.7%	100010B: 53.3%	
		001001B: 20.4%	100011B: 35.9%	001001B: 38.3%	100011B: 53.9%	
		001010B: 21.0%	100100B: 36.5%	001010B: 38.9%	100100B: 54.5%	
		001011B: 21.6%	100101B: 37.1%	001011B: 39.5%	100101B: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101B: 22.8%	100111B: 38.3%	001101B: 40.7%	100111B: 56.3%	
		001110B: 23.4%	101000B: 38.9%	001110B: 41.3%	101000B: 56.9%	
		001111B: 24.0%	101001B: 39.5%	001111B: 41.9%	101001B: 57.5%	
		010000B: 24.6%	101010B: 40.1%	010000B: 42.5%	101010B: 58.1%	
		010001B: 25.1%	101011B: 40.7%	010001B: 43.1%	101011B: 58.7%	
		010010B: 25.7%	101100B: 41.3%	010010B: 43.7%	101100B: 59.3%	
		010011B: 26.3%	101101B: 41.9%	010011B: 44.3%	101101B: 59.9%	
		010100B: 26.9%	101110B: 42.5%	010100B: 44.9%	101110B: 60.5%	
		010101B: 27.5%	101111B: 43.1%	010101B: 45.5%	101111B: 61.1%	
		010110B: 28.1%	110000B: 43.7%	010110B: 46.1%	110000B: 61.7%	
		010111B: 28.7%	110001B: 44.3%	010111B: 46.7%	110001B: 62.3%	
		011000B: 29.3%	110010B: 44.9%	011000B: 47.3%	110010B: 62.9%	
		011001B: 29.9%	All Others: Reserved	011001B: 47.9%	All Others: Reserved	

Notes:

1. These values may be used for MR12 OP[5:0] to set the VREF(CA) levels in the LPDDR4X-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.

Table 45. MR13 Register Information (MA[5:0] = 0DH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	0B: Normal Operation (default) 1B: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training)		OP[1]	0B: Disable (default) 1B: Enable	
VRO (VREF Output)		OP[2]	0B: Normal operation (default) 1B: Output the VREF(CA) and VREF(DQ) values on DQ bits	2
VRCG (VREF Current Generator)		OP[3]	0B: Normal Operation (default) 1B: VREF Fast Response (high current) mode	3
RRO Refresh rate option		OP[4]	0B: Disable codes 001 and 010 in MR4 OP[2:0] 1B: Enable all codes in MR4 OP[2:0]	4, 5
DMD (Data Mask Disable)		OP[5]	0B: Data Mask Operation Enabled (default) 1B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point [1]	8

Notes:

1. A write to set OP[0]=1 causes the LPDDR4X-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the LPDDR4X-SDRAM will output the VREF(CA) and VREF(DQ) voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. The DQ pins used for VREF output are vendor specific.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4X devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4X devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), masked write command is illegal. See LPDDR4X Data Mask (DM) and Data Bus Inversion (DBIdc) Function.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to Frequency Set Point section.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to Frequency Set Point section.

Table 46. MR14 Register Information (MA[5:0] = 0EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR(DQ)	VREF(DQ)					

Function	Type	Operand	Data	Notes
VREF(DQ) (VREF(DQ) Setting)	Read / Write	OP[5:0]	000000B - 110010B: See table below All Others: Reserved	1,2,3, 5,6
VR(DQ) (VREF(DQ) Range)		OP[6]	0B: VREF(DQ) Range[0] enabled 1B: VREF(DQ) Range[1] enabled (default)	1,2,4, 5,6

Notes:

1. This register controls the VREF(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See the MRR Operation section.
3. A write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(DQ) to reach the set level depends on the step size from the current level to the new level. See the VREF(DQ) training section.
4. A write to OP[6] switches the LPDDR4X-SDRAM between two internal VREF(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 47. VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR14	OP[5:0]	000000B: 15.0%	011010B: 30.5 %	000000B: 32.9%	011010B: 48.5%	1,2,3
		000001B: 15.6%	011011B: 31.1%	000001B: 33.5%	011011B: 49.1%	
		000010B: 16.2%	011100B: 31.7%	000010B: 34.1%	011100B: 49.7%	
		000011B: 16.8%	011101B: 32.3%	000011B: 34.7%	011101B: 50.3% (default)	
		000100B: 17.4%	011110B: 32.9%	000100B: 35.3%	011110B: 50.9%	
		000101B: 18.0%	011111B: 33.5%	000101B: 35.9%	011111B: 51.5%	
		000110B: 18.6%	100000B: 34.1%	000110B: 36.5%	100000B: 52.1%	
		000111B: 19.2%	100001B: 34.7%	000111B: 37.1%	100001B: 52.7%	
		001000B: 19.8%	100010B: 35.3%	001000B: 37.7%	100010B: 53.3%	
		001001B: 20.4%	100011B: 35.9%	001001B: 38.3%	100011B: 53.9%	
		001010B: 21.0%	100100B: 36.5%	001010B: 38.9%	100100B: 54.5%	
		001011B: 21.6%	100101B: 37.1%	001011B: 39.5%	100101B: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101B: 22.8%	100111B: 38.3%	001101B: 40.7%	100111B: 56.3%	
		001110B: 23.4%	101000B: 38.9%	001110B: 41.3%	101000B: 56.9%	
		001111B: 24.0%	101001B: 39.5%	001111B: 41.9%	101001B: 57.5%	
		010000B: 24.6%	101010B: 40.1%	010000B: 42.5%	101010B: 58.1%	
		010001B: 25.1%	101011B: 40.7%	010001B: 43.1%	101011B: 58.7%	
		010010B: 25.7%	101100B: 41.3%	010010B: 43.7%	101100B: 59.3%	
		010011B: 26.3%	101101B: 41.9%	010011B: 44.3%	101101B: 59.9%	
		010100B: 26.9%	101110B: 42.5%	010100B: 44.9%	101110B: 60.5%	
		010101B: 27.5%	101111B: 43.1%	010101B: 45.5%	101111B: 61.1%	
		010110B: 28.1%	110000B: 43.7%	010110B: 46.1%	110000B: 61.7%	
		010111B: 28.7%	110001B: 44.3%	010111B: 46.7%	110001B: 62.3%	
		011000B: 29.3%	110010B: 44.9%	011000B: 47.3%	110010B: 62.9%	
		011001B: 29.9%	All Others: Reserved	011001B: 47.9%	All Others: Reserved	

Notes:

1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4X-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.

Table 48. MR15 Register Information (MA[5:0] = 0FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-Byte Invert Register for DQ Calibration							

Function	Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2,3

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the “true” data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 49. MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

Table 50. MR16 Register Information (MA[5:0] = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Bank Mask							

Function	Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0B: Bank Refresh enabled (default) : Unmasked 1B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:

1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

Table 51. MR17 Register Information (MA[5:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Segment Mask							

Function	Type	Operand	Data
PASR Segment Mask	Write-only	OP[7:0]	0B: Segment Refresh enabled (default) 1B: Segment Refresh disabled

Segment	OP[n]	Segment Mask	4Gb per channel
			R14:R12
0	0	xxxxxxx1	000B
1	1	xxxxxx1x	001B
2	2	xxxxx1xx	010B
3	3	xxxx1xxx	011B
4	4	xxx1xxxx	100B
5	5	xx1xxxxx	101B
6	6	x1xxxxxx	110B
7	7	1xxxxxxx	111B

Notes:

1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.

Table 52. MR18 Register Information (MA[5:0] = 12H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count - LSB							

Function	Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	1~3

Notes:

1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

Table 53. MR19 Register Information (MA[5:0] = 13H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count - MSB							

Function	Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM DQS Oscillator Count	1~3

Notes:

1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

Table 54. MR20 Register Information (MA[5:0] = 14H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-Byte Invert Register for DQ Calibration							

Function	Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55H	1,2

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 55. MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR21 (Reserved) (MA[5:0] = 15H)

Table 56. MR22 Register Information (MA[5:0] = 16H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Function	Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 (illegal if MR3 OP[0] = 0B) 010B: RZQ/2 011B: RZQ/3 (illegal if MR3 OP[0] = 0B) 100B: RZQ/4 101B: RZQ/5 (illegal if MR3 OP[0] = 0B) 110B: RZQ/6 (illegal if MR3 OP[0] = 0B) 111B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non- terminating rank)		OP[3]	ODT bond PAD is ignored 0B: ODT-CK Enable (Default) 1B: ODT-CK Disable	2,3
ODTE-CS (CS ODT enable for non- terminating rank)		OP[4]	ODT bond PAD is ignored 0B: ODT-CS Enable (Default) 1B: ODT-CS Disable	2,3
ODTD-CA (CA ODT termination disable)		OP[5]	ODT bond PAD is ignored 0B: ODT-CA Enable (default) 1B: ODT-CA Disable	2,3

Notes:

1. All values are “typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 57. MR23 Register Information (MA[5:0] = 17H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run time setting							

Function	Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	00000000B: DQS interval timer stop via MPC Command (Default) 00000001B: DQS timer stops automatically at 16th clocks after timer start 00000010B: DQS timer stops automatically at 32nd clocks after timer start 00000011B: DQS timer stops automatically at 48th clocks after timer start 00000100B: DQS timer stops automatically at 64th clocks after timer start ------- Thru ------- 00111111B: DQS timer stops automatically at (63X16) th clocks after timer start 01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start 10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start 11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start	1,2

Notes:

1. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

Table 58. MR24 Register Information (MA[5:0] = 18H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR Mode	TRR Mode BAn			Unltd MAC	MAC Value		

Function	Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000B: Unknown when bit OP3=0 (Note 1) Unlimited when bit OP3=1 (Note 2) 001B: 700K 010B: 600K 011B: 500K 100B: 400K 101B: 300K 110B: 200K 111B: Reserved	
Unlimited MAC		OP[3]	0B: OP[2:0] define MAC value 1B: Unlimited MAC value (Note 2, Note 3)	
TRR Mode BAn	Write-only	OP[6:4]	000B: Bank 0 001B: Bank 1 010B: Bank 2 011B: Bank 3 100B: Bank 4 101B: Bank 5 110B: Bank 6 111B: Bank 7	
TRR Mode		OP[7]	0B: Disabled (default) 1B: Enabled	

Notes:

1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

Table 59. MR25 Register Information (MA[5:0] = 19H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0

Function	Type	Operand	Data
PPR Resource	Read-only	OP[7:0]	0B: PPR Resource is not available 1B: PPR Resource is available

MR26~29 (Reserved) (MA[5:0] = 1AH-1DH)

Table 60. MR30 Register Information (MA[5:0] = 1EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR31 (Reserved) (MA[5:0] = 1FH)

Table 61. MR32 Register Information (MA[5:0] = 20H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern “A” (default = 5AH)							

Function	Type	Operand	Data
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: An MPC command with OP[6:0]= 1000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern “5AH”is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)

MR33~38 (Reserved) (MA[5:0] = 21H-26H)

Table 62. MR39 Register Information (MA[5:0] = 27H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

Table 63. MR40 Register Information (MA[5:0] = 28H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern “B” (default = 3CH)							

Function	Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write-only	OP[7:0]	XB: A default pattern “3CH” is loaded at power- up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3

Notes:

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized “little endian” such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H , then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Table 64. Refresh Requirement Parameters

Refresh Requirements		Symbol	4Gb	Units
Density per Channel			4Gb	
Number of banks per channel			8	
Refresh Window (TCASE ≤ 85°C)		tREFW	32	ms
Refresh Window (1/2 Rate Refresh)		tREFW	16	ms
Refresh Window (1/4 Rate Refresh)		tREFW	8	ms
Required Number of Refresh Commands in a tREFW window		R	8192	-
Average Refresh Interval (1x Refresh)[2]	REFAB	tREFI	3.904	us
	REFPB	tREFIpb	488	ns
Refresh Cycle Time (All Banks)		tRFCab	180	ns
Refresh Cycle Time (Per Bank)		tRFCpb	90	ns
Per-bank Refresh to Per-bank Refresh different bank Time		tpbR2pbR	90	ns

Notes:

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. 1x refresh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[2:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.
3. Refer to MR4 OP[2:0] for detailed Refresh Rate and its multipliers.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 65. Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units	Notes
VDD1	VDD1 supply voltage relative to Vss	-0.4	2.1	V	1
VDD2	VDD2 supply voltage relative to Vss	-0.4	1.5	V	1
VDDQ	VDDQ supply voltage relative to VSSQ	-0.4	1.5	V	1
VIN, VOUT	Voltage on any ball except VDD1 relative to Vss	-0.4	1.5	V	
TSTG	Storage Temperature	-55	125	°C	2

Notes:

1. See “Power-Ramp” for relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2.

Table 66. Operating Temperature Range

Symbol	Parameter	Min	Max	Units	Notes
TOPER	Standard	-25	85	°C	1~2

Notes:

1. Operating Temperature is the case surface temperature on the center-top side of the device. For the measurement conditions, please refer to JESD51-2.
2. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

AC and DC Operating Conditions

Table 67. Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD1	Core 1 Power	1.70	1.80	1.95	V	1,2
VDD2	Core 2 Power/Input Buffer Power	1.06	1.10	1.17	V	1,2,3
VDDQ	I/O Buffer Power	0.57	0.6	0.65	V	2-5

Notes:

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.
4. VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 MHz.
5. Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

Table 68. Input Leakage Current

Symbol	Parameter	Min	Max	Units	Notes
IL	Input Leakage current	-4	4	uA	1,2

Notes:

1. For CK, CK#, CKE, CS, CA, ODT_CA and RESET#. Any input 0V ≦ VIN ≦ VDD2 (All other pins not under test = 0V).
2. CA ODT is disabled for CK, CK#, CS, and CA.

Table 69. Input/Output Leakage Current

Symbol	Parameter	Min	Max	Units	Notes
IOZ	Input/Output Leakage current	-5	5	uA	1,2

Notes:

1. For DQ, DQS, DQS# and DMI. Any I/O 0V ≦ VOUT ≦ VDDQ.
2. I/Os status are disabled: High Impedance and ODT Off.

Table 70. Input/output capacitance

Symbol	Parameter	Min	Max	Units	Notes
CCK	Input capacitance, CK and CK#	0.5	0.9	pF	1,2
CDCK	Input capacitance delta, CK and CK#	0	0.09	pF	1,2,3
CI	Input capacitance, All other input-only pins	0.5	0.9	pF	1,2,4
CDI	Input capacitance delta, All other input-only pins	-0.1	0.1	pF	1,2,5
CIO	Input/output capacitance, DQ, DMI, DQS, DQS#	0.7	1.3	pF	1,2,6
CDDQS	Input/output capacitance delta, DQS,DQS#	0	0.1	pF	1,2,7
CDIO	Input/output capacitance delta, DQ, DMI	-0.1	0.1	pF	1,2,8
CZQ	Input/output capacitance, ZQ pin	0	5	pF	1,2

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK, CCK#.
4. CI applieds to CS, CKE, CA0~CA5.
5. CDI = CI - 0.5 x (CCK + CCK#)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS and CDQS#.
8. CDIO = CIO - 0.5 x (CDQS + CDQS#) in byte-lane.

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:
LOW: VIN ≤ VIL(DC) MAX
HIGH: VIN ≥ VIH(DC) MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: Please refer to the following two tables below:

Table 71. Definition of Switching for CA Input Signals

Switching for CA								
CK Edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:
1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 72. CA pattern for IDD4R for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes:
1. BA[2:0] = 010, C[9:4] = 000000 or 111111, Burst Order C[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 (JESD209-3): CA pins are kept low with DES CMD to reduce ODT current.

Table 73. CA pattern for IDD4W for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Notes:

1. BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W).
2. Difference from LPDDR3 (JESD209-3): 1)-No burst ordering, and 2) CA pins are kept low with DES CMD to reduce ODT current.

Table 74. Data Pattern for IDD4W (DBI off) for BL=16

	DBI OFF Case									**No. of 1's**
	DQ[7]	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 75. Data Pattern for IDD4R (DBI off) for BL=16

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Notes:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 76. Data Pattern for IDD4W (DBI On) for BL=16

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Notes:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, and BL28.

Table 77. Data Pattern for IDD4R (DBI On) for BL=16

	DBI ON Case									No. of 1's
	DQ[7]	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Notes:

1. DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL20, BL26, and BL30.

Table 78. CA pattern for IDD4R for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note: BA[2:0] = 010, C[9:4] = 00000 or 11111, Burst Order C[4:2] = 000 or 111.

Table 79. CA pattern for IDD4W for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note: BA[2:0] = 010, CA[9:5] = 00000 or 11111

Table 80. Data Pattern for IDD4W (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	1	1	1	1	1	1	0	0	0	6
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8

BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1’s	32	32	32	32	32	32	32	32		

Note: Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 81. Data Pattern for IDD4R (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2

BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1’s	32	32	32	32	32	32	32	32		

Note: Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 82. Data Pattern for IDD4W (DBI On) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	0	0	0	0	0	0	1	1	1	3
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1

BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

Note: DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL32, BL38, BL40, BL46, BL48, BL54, BL58, and BL60.

Table 83. Data Pattern for IDD4R (DBI On) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2

BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1’s	16	16	16	16	16	16	32	32	16	

Note: DBI enabled burst: BL0, BL6, BL8, BL14, BL16, BL22, BL26, BL28, BL34, BL36, BL42, BL44, BL48, BL52, BL58, and BL62.

IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Table 84. IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCKmin;CKE is LOW;CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable,ODT disabled	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non-power-down standby current with clock stopped: CK=LOW; CK#=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop: CK=LOW, CK#=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped: CK=LOW, CK#=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All bank REFRESH Burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4
All bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
Per bank REFRESH Average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PBQ	VDDQ	4
Power Down Self Refresh current: CK=LOW, CK#=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self Refresh Rate; ODT disabled	IDD61	VDD1	6,7,9
	IDD62	VDD2	6,7,9
	IDD6Q	VDDQ	4,6,7,9

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 Ω.
6. This is the general definition that applies to full array Self Refresh.
7. Supplier data sheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
8. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9. IDD6 25°C is the typical; IDD6 at 85°C represents the maximum value in the distribution of the arithmetic mean.

Table 85. IDD Specification Parameters

(T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Parameter	Supply	4Gb x16	Unit
IDD01	VDD1	13	mA
IDD02	VDD2	43	mA
IDD0Q	VDDQ	0.2	mA
IDD2P1	VDD1	0.4	mA
IDD2P2	VDD2	1.3	mA
IDD2PQ	VDDQ	0.1	mA
IDD2PS1	VDD1	0.4	mA
IDD2PS2	VDD2	1.3	mA
IDD2PSQ	VDDQ	0.1	mA
IDD2N1	VDD1	1.6	mA
IDD2N2	VDD2	25	mA
IDD2NQ	VDDQ	0.1	mA
IDD2NS1	VDD1	1.6	mA
IDD2NS2	VDD2	7.7	mA
IDD2NSQ	VDDQ	0.1	mA
IDD3P1	VDD1	2.3	mA
IDD3P2	VDD2	4.9	mA
IDD3PQ	VDDQ	0.1	mA
IDD3PS1	VDD1	2.2	mA
IDD3PS2	VDD2	4.8	mA
IDD3PSQ	VDDQ	0.1	mA
IDD3N1	VDD1	2.3	mA
IDD3N2	VDD2	30	mA
IDD3NQ	VDDQ	0.2	mA
IDD3NS1	VDD1	2.3	mA
IDD3NS2	VDD2	13	mA
IDD3NSQ	VDDQ	0.2	mA
IDD4R1	VDD1	14	mA
IDD4R2	VDD2	283	mA
IDD4RQ	VDDQ	90	mA
IDD4W1	VDD1	14	mA
IDD4W2	VDD2	300	mA
IDD4WQ	VDDQ	0.3	mA
IDD51	VDD1	27	mA
IDD52	VDD2	56	mA
IDD5Q	VDDQ	0.2	mA
IDD5AB1	VDD1	3.1	mA
IDD5AB2	VDD2	32	mA
IDD5ABQ	VDDQ	0.1	mA
IDD5PB1	VDD1	3.7	mA
IDD5PB2	VDD2	32	mA
IDD5PBQ	VDDQ	0.1	mA

Table 86. IDD6 specification

(T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Temperature	Parameter	Supply	Full-Array Self Refresh Current	Unit
25°C	IDD61	VDD1	3	mA
	IDD62	VDD2	3	mA
	IDD6Q	VDDQ	0.1	mA
85°C	IDD61	VDD1	3	mA
	IDD62	VDD2	4	mA
	IDD6Q	VDDQ	0.1	mA

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the device.

Definitions for $t_{CK(avg)}$ and nCK:

$t_{CK(avg)}$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\mathrm{tCK(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCK}_j\right) / \mathrm{N}$$

Where N=200

Unit '$t_{CK(avg)}$' represents the actual clock average $t_{CK(avg)}$) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
$t_{CK(avg)}$ may change by up to ±1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

Definitions for $t_{CK(abs)}$:

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $t_{CK(abs)}$ is not subject to production test.

Definitions for $t_{CH(avg)}$ and $t_{CL(avg)}$:

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$\mathrm{tCH(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCH}_j\right) / \left(\mathrm{N} \times \mathrm{tCK(avg)}\right)$$

Where N=200

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\mathrm{tCL(avg)} = \left(\sum_{j=1}^{N} \mathrm{tCL}_j\right) / \left(\mathrm{N} \times \mathrm{tCK(avg)}\right)$$

Where N=200

Definitions for $t_{CH(abs)}$ and $t_{CL(abs)}$:

$t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
$t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
Both $t_{CH(abs)}$ and $t_{CL(abs)}$ are not subject to production test.

Definitions for $t_{JIT(per)}$:

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.
$t_{JIT(per)}$ = Min/max of {t_{CKi} - $t_{CK(avg)}$ where i = 1 to 200}.
$t_{JIT(per),act}$ is the actual clock jitter for a given system.
$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

Definitions for $t_{JIT(cc)}$:

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$t_{JIT(cc)}$ = Max of |{$t_{CK(i+1)}$ - $t_{CK(i)}$}|.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

Electrical Characteristics and AC Timing

Table 87. AC Timing (T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Symbol	Parameter	Data Rate						Unit	Note
		4266		3733		3200			
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock Timing									
$t_{CK(avg)}$	Average clock period	0.468	100	0.535	100	0.625	100	ns	
$t_{CH(avg)}$	Average High pulse width	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	
$t_{CL(avg)}$	Average Low pulse width	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	
$t_{CK(abs)}$	Absolute clock period	**Min:** $t_{CK(avg)min}$ + $t_{JIT(per),min}$						ns	
$t_{CH(abs)}$	Absolute High clock pulse width	0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}	
$t_{CL(abs)}$	Absolute Low clock pulse width	0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}	
$t_{JIT(per)}$	Clock period jitter	-30	30	-34	34	-40	40	ps	
$t_{JIT(cc)}$	Maximum Clock Jitter between consecutive cycles	-	60	-	68	-	80	ps	
Core Parameters									
t_{RC}	Activate-to-Activate command period (same bank)	**Min:** t_{RAS} + t_{RPab} (with all bank precharge) t_{RAS} + t_{RPpb} (with per bank precharge)						ns	
t_{SR}	Minimum Self Refresh Time (Entry to Exit)	**Min:** max(15ns, 3nCK)						ns	
t_{XSR}	Self Refresh exit to next valid command delay	**Min:** max(t_{RFCab} + 7.5ns, 2nCK)						ns	
t_{XP}	Exit Power-Down to next valid command delay	**Min:** max(7.5ns, 5nCK)						ns	3
t_{CCD}	CAS-to-CAS delay	**Min:** 8						t_{CK}	
t_{RTP}	Internal Read to Precharge command delay	**Min:** max(7.5ns, 8nCK)						ns	
t_{RCD}	RAS-to-CAS delay	**Min:** max(18ns, 4nCK)						ns	
t_{RPpb}	Row precharge time (single bank)	**Min:** max(18ns, 4nCK)						ns	
t_{RPab}	Row precharge time (all banks)	**Min:** max(21ns, 4nCK)						ns	
t_{RAS}	Row active time	**Min:** max(42ns, 3nCK)						ns	
		Max: min(9 x t_{REFI} x Refresh Rate, 70.2)						us	4
t_{WR}	Write recovery time	**Min:** max(18ns, 6nCK)						ns	
t_{WTR}	Write-to-Read delay	**Min:** max(10ns, 8nCK)						ns	
t_{RRD}	Active bank-A to active bank-B	max (7.5ns, 4nCK)	-	max (10ns, 4nCK)	-	max (10ns, 4nCK)	-	ns	2
t_{PPD}	Precharge to Precharge Delay	**Min:** 4						t_{CK}	1
t_{FAW}	Four-bank Activate window	30	-	40	-	40	-	ns	2
Read output timings (Unit UI = tCK(avg)min/2)									
t_{DQSQ}	DQS,DQS# to DQ Skew total, per group,per access (DBI-Disabled)	-	0.18	-	0.18	-	0.18	UI	
t_{QH}	DQ output hold time total from DQS, DQS# (DBI Disabled)	**Min:** min(t_{QSH}, t_{QSL})						UI	
t_{QW_total}	DQ output window timetotal, per pin (DBI-Disabled)	0.7	-	0.7	-	0.7	-	UI	7
t_{DQSQ_DBI}	DQS,DQS# to DQSkew total, per group,per access (DBI-Enabled)	-	0.18	-	0.18	-	0.18	UI	
t_{QH_DBI}	DQ output hold time total from DQS, DQS# (DBI-Enabled)	**Min:** min(t_{QSH_DBI}, t_{QSL_DBI})						UI	
$t_{QW\_total\_DBI}$	DQ output window timetotal, per pin (DBI-Enabled)	0.7	-	0.7	-	0.7	-	UI	7
t_{QSL}	DQS, DQS# differential output low time (DBI-Disabled)	**Min:** $t_{CL(abs)}$-0.05						t_{CK}	7,8
t_{QSH}	DQS, DQS# differential output high time (DBI-Disabled)	**Min:** $t_{CH(abs)}$-0.05						t_{CK}	7,9
t_{QSL_DBI}	DQS, DQS# differential output low time (DBI-Enabled)	**Min:** $t_{CL(abs)}$-0.045						t_{CK}	8,10
t_{QSH_DBI}	DQS, DQS# differential output high time (DBI-Enabled)	**Min:** $t_{CH(abs)}$-0.045						t_{CK}	9,10
Read AC Timing (Unit UI = tCK(avg)min/2)									
t_{RPRE}	Read preamble	1.8	-	1.8	-	1.8	-	t_{CK}	
t_{RPST}	0.5 tCK Read postamble	0.4	-	0.4	-	0.4	-	t_{CK}	

t_{RPST}	1.5 tCK Read postamble	1.4	-	1.4	-	1.4	-	t_{CK}	
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#	**Min:** (RL x t_{CK}) + $t_{DQSCK(min)}$ - 200ps						ps	
$t_{HZ(DQ)}$	DQ high impedance time from CK, CK#	**Max:** (RL x t_{CK}) + $t_{DQSCK(max)}$ + $t_{DQSQ(max)}$ + (BL/2xt_{CK}) - 100ps						ps	
$t_{LZ(DQS)}$	DQS# low-impedance time from CK, CK#	**Min:** (RL x t_{CK}) + $t_{DQSCK(min)}$ - ($t_{RPRE(max)}$ x t_{CK}) - 200ps						ps	
$t_{HZ(DQS)}$	DQS# high impedance time from CK, CK#	**Max:** (RL x t_{CK}) + $t_{DQSCK(max)}$ +(BL/2 x t_{CK}) + ($t_{RPST(max)}$ x t_{CK}) - 100ps						ps	
t_{DQSQ}	DQS-DQ skew	-	0.18	-	0.18	-	0.18	UI	
tDQSCK Timing									
t_{DQSCK}	DQS Output Access Time from CK/CK#	1.5	3.5	1.5	3.5	1.5	3.5	ns	11-13
t_{DQSCK_temp}	DQS Output Access Time from CK/CK# - Temperature Variation	-	4	-	4	-	4	ps/°C	11-13
t_{DQSCK_volt}	DQS Output Access Time from CK/CK# - Voltage Variation	-	7	-	7	-	7	ps/mV	11-13
$t_{DQSCK\_rank2rank}$	CK to DQS Rank to Rank variation	-	1.0	-	1.0	-	1.0	ns	14,15
Write AC Timing									
t_{DQSS}	Write command to 1st DQS latching	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
t_{DQSH}	DQS input high-level	0.4	-	0.4	-	0.4	-	t_{CK}	
t_{DQSL}	DQS input low-level width	0.4	-	0.4	-	0.4	-	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time	0.2	-	0.2	-	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK	0.2	-	0.2	-	0.2	-	t_{CK}	
t_{WPRE}	Write preamble	1.8	-	1.8	-	1.8	-	t_{CK}	
t_{WPST}	0.5 tCK Write postamble	0.4	-	0.4	-	0.4	-	t_{CK}	16
t_{WPST}	1.5 tCK Write postamble	1.4	-	1.4	-	1.4	-	t_{CK}	16
Write Leveling Timing									
$t_{WLDQSEN}$	DQS/DQS# delay after write leveling mode is programmed	20	-	20	-	20	-	t_{CK}	
t_{WLWPRE}	Write preamble for Write Leveling	20	-	20	-	20	-	t_{CK}	
t_{WLMRD}	First DQS/DQS# edge after write leveling mode is programmed	40	-	40	-	40	-	t_{CK}	
t_{WLO}	Write leveling output delay	0	20	0	20	0	20	ns	
t_{MRD}	Mode register set command delay	**Min:** max(14ns, 10nCK)						ns	
$t_{CKPRDQS}$	Valid Clock Requirement before DQS Toggle	**Min:** max(7.5ns, 4nCK)						-	
$t_{CKPSTDQS}$	Valid Clock Requirement after DQS Toggle	**Min:** max(7.5ns, 4nCK)						-	
t_{WLH}	Write leveling hold time	50	-	60	-	75	-	ps	
t_{WLS}	Write leveling setup time	50	-	60	-	75	-	ps	
t_{WLIVW}	Write leveling input valid window	90	-	100	-	120	-	ps	
Power-Down AC Timing									
t_{CKE}	CKE minimum pulse width (HIGH and LOW pulse width)	**Min:** max(7.5ns, 4nCK)						-	
t_{CMDCKE}	Delay from valid command to CKE input LOW	**Min:** max(1.75ns, 3nCK)						ns	17
t_{CKELCK}	Valid Clock Requirement after CKE Input low	**Min:** max(5ns, 5nCK)						ns	17
t_{CSCKE}	Valid CS Requirement before CKE Input Low	**Min:** 1.75						ns	
t_{CKELCS}	Valid CS Requirement after CKE Input low	**Min:** max(5ns, 5nCK)						ns	
t_{CKCKEH}	Valid Clock Requirement before CKE Input High	**Min:** max(1.75ns, 3nCK)						ns	17
t_{XP}	Exit power- down to next valid command delay	**Min:** max(7.5ns, 5nCK)						ns	17
t_{CSCKEH}	Valid CS Requirement before CKE Input High	**Min:** 1.75						ns	
t_{CKEHCS}	Valid CS Requirement after CKE Input High	**Min:** max(7.5ns, 5nCK)						ns	
$t_{MRWCKEL}$	Valid Clock and CS Requirement after CKE Input low after MRW Command	**Min:** max(14ns, 10nCK)						ns	17
t_{ZQCKE}	Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	**Min:** max(1.75ns, 3nCK)						ns	17
Mode Register Read/Write AC timing									

t_{MRRI}	Additional time after t_{XP} has expired until MRR command may be issued	**Min:** t_{RCD} + 3nCK						-	
t_{MRR}	Mode Register Read command period	**Min:** 8						nCK	
t_{MRW}	Mode Register Write command period	**Min:** max(10ns, 10nCK)						-	
t_{MRD}	Mode register set command delay	**Min:** max(14ns, 10nCK)						-	
Asynchronous ODT Timing									
t_{ODTon}	Asynchronous ODT Turn On	1.5	3.5	1.5	3.5	1.5	3.5	ns	
t_{ODToff}	Asynchronous ODT Turn Off	1.5	3.5	1.5	3.5	1.5	3.5	ns	
Self-Refresh Timing Parameters									
t_{ESCKE}	Delay from SRE command to CKE Input low	**Min:** max(1.75ns, 3tCK)						ns	18
t_{SR}	Minimum Self Refresh Time	**Min:** max(15ns, 3tCK)						ns	18
t_{XSR}	Exit Self Refresh to Valid commands	**Min:** max(tRFCab + 7.5ns, 2tCK)						ns	18,19
Command Bus Training AC Timing									
t_{CKELCK}	Valid Clock Requirement after CKE Input low	**Min:** max(5ns, 5nCK)						-	
$t_{DStrain}$	Data Setup for VREF Training Mode	2	-	2	-	2	-	ns	
$t_{DHtrain}$	Data Hold for VREF Training Mode	2	-	2	-	2	-	ns	
t_{ADR}	Asynchronous Data Read	-	20	-	20	-	20	ns	
t_{CACD}	CA Bus Training Command to CA Bus Training Command Delay	**Min:** RU(tADR/tCK)						t_{CK}	21
t_{DQSCKE}	Valid Strobe Requirement before CKE Low	10	-	10	-	10	-	ns	20
t_{CAENT}	First CA Bus Training Command Following CKE Low	250	-	250	-	250	-	ns	
t_{VREFCA_LONG}	VREF Step Time – multiple steps	-	250	-	250	-	250	ns	
t_{VREFCA_SHORT}	Vref Step Time -one step	-	80	-	80	-	80	ns	
$t_{CKPRECS}$	Valid Clock Requirement before CS High	**Min:** 2tCK + tXP						-	
$t_{CKPSTCS}$	Valid Clock Requirement after CS High	**Min:** max(7.5ns, 5nCK)						-	
t_{CS_VREF}	Minimum delay from CS to DQS toggle in command bus training	2	-	2	-	2	-	t_{CK}	
$t_{CKEHDQS}$	Minimum delay from CKE High to Strobe High Impedance	10	-	10	-	10	-	ns	
t_{CKCKEH}	Valid Clock Requirement before CKE input High	**Min:** max(1.75ns, 3nCK)						-	
t_{MRZ}	CA Bus Training CKE High to DQ Tri-state	1.5	-	1.5	-	1.5	-	ns	
$t_{CKELODTon}$	ODT turn-on Latency from CKE	20	-	20	-	20	-	ns	
$t_{CKELODToff}$	ODT turn-off Latency from CKE	20	-	20	-	20	-	ns	
t_{XCBT_Short}	Exit Command Bus Training Mode to next valid command delay	**Min:** max(5nCK, 200ns)						-	22
t_{XCBT_Middle}		**Min:** max(5nCK, 200ns)						-	22
t_{XCBT_Long}		**Min:** max(5nCK, 250ns)						-	22
VRCG Enable/Disable Timing									
t_{VRCG_Enable}	VREF high current mode enable time	-	200	-	200	-	200	ns	
$t_{VRCG\_Disable}$	VREF high current mode disable time	-	100	-	100	-	100	ns	
MPC Write FIFO Timing									
t_{MPCWR}	Additional time after tXP has expired until MPC [Write FIFO] command may be issued	**Min:** tRCD + 3nCK							
DQS Interval Oscillator AC Timing									
t_{OSCO}	Delay time from OSC stop to Mode Register Readout	**Min:** max(40ns, 8nCK)						ns	23
Read Preamble Training Timing									
t_{SDO}	Delay from MRW command to DQS Driven	**Max:** max(12nCK, 20ns)						ns	
ZQ Calibration Timing									
t_{ZQCAL}	ZQ Calibration Time	**Min:** 1						us	
t_{ZQLAT}	ZQ Calibration Latch Time	**Min:** max(30ns, 8nCK)						ns	
$t_{ZQRESET}$	ZQ Calibration Reset Time	**Min:** max(50ns, 3nCK)						ns	

ODT CA Timing									
t_{ODTUP}	ODT CA Value Update Time	**Min:** RU(TBDns/tCK(avg))							
Frequency Set Point Timing									
t_{FC_Short}	Frequency Set Point Switching Time	200	-	200	-	200	-	ns	6
t_{FC_Middle}	Minimum Self Refresh Time	200	-	200	-	200	-	ns	6
t_{FC_Long}	Exit Self Refresh to Valid command	250	-	250	-	250	-	ns	6
t_{CKFSPE}	Valid Clock Requirement after Entering FSP Change	max(7.5ns, 4nCK)						-	
t_{CKFSPX}	Valid Clock Requirement before 1st Valid Command after FSP change	max(7.5ns, 4nCK)						-	

Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. Devices supporting 4267 Mbps specification shall support these timings at lower data rates.
3. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
4. Refresh Rate is specified by MR4, OP[2:0]
5. The deterministic component of the total timing. Measurement method tbd.
6. Frequency Set Point Switching Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range:MR12 OP[6] of FSP-OP 0 and 1. Additionally change of Frequency Set Point may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.
7. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
8. tQSL describes the instantaneous differential output low pulse width on DQS – DQS#, as it measured the next rising edge from an arbitrary falling edge.
9. tQSH describes the instantaneous differential output high pulse width on DQS – DQS#, as it measured the next rising edge from an arbitrary falling edge.
10. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
11. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies> 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
12. tDQSCK_temp max delay variation as a function of Temperature.
13. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1- tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.
14. The same voltage and temperature are applied to tDQS2CK_rank2rank.
15. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
16. The length of Write Postamble depends on MR3 OP1 setting.
17. Delay time has to satisfy both analog time(ns) and clock count(nCK).
18. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 x tCK) and 1.75ns has transpired.
19. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.
20. DQS has to retain a low level during tDQSCKE period, as well as DQS# has to retain a high level.
21. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
22. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.
23. Start DQS OSC command is prohibited until tOSCO(Min) is satisfied.

Single Ended Output Slew Rate

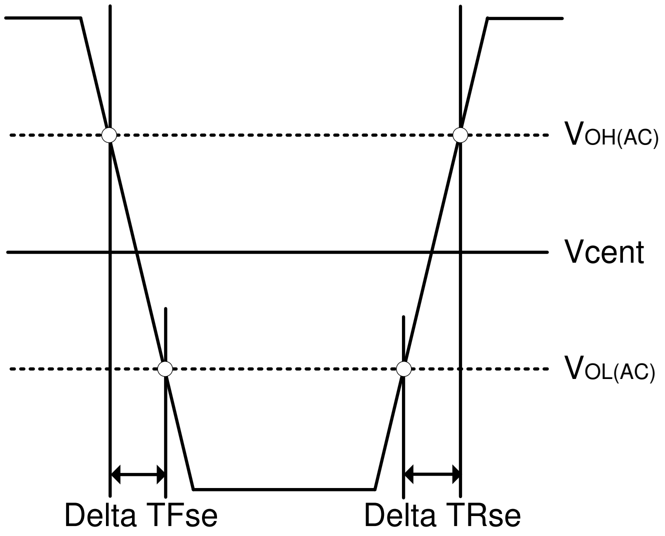


Figure 47. Single Ended Output Slew Rate Definition

Table 88. Output Slew Rate (Single-ended)

Symbol	Parameter	Value		Unit
		Min.	Max.	
SRQse	Single-ended Output Slew Rate ($V_{OH} = V_{DDQ}$ x 0.5)	3.0	9	V/ns
-	Output slew-rate matching Ratio (Rise to Fall)	0.8	1.2	-

Notes:

1. Description:
   SR: Slew Rate
   Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
   se: Single-ended Signals
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
5. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate

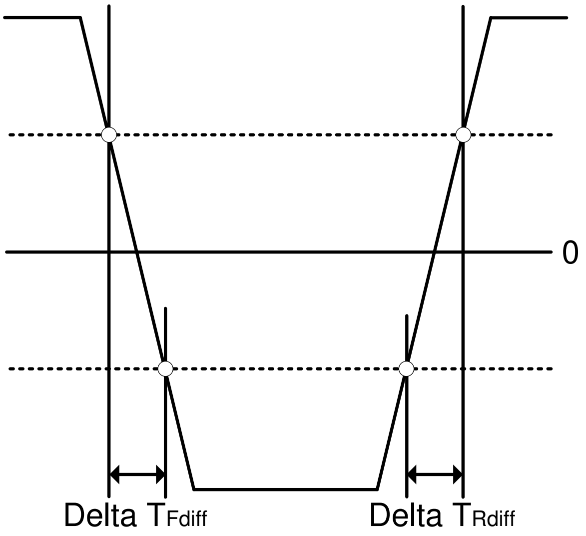


Figure 48. Differential Output Slew Rate Definition

Table 89. Differential Output Slew Rate

Symbol	Parameter	Value		Unit
		Min.	Max.	
SRQdiff	Differential Output Slew Rate ($V_{OH} = V_{DDQ}$ x 0.5)	6	18	V/ns

Notes:

1. Description:
   SR: Slew Rate
   Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
   diff: Differential Signals
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ = -0.8 x $V_{OH(DC)}$ and $V_{OH(AC)}$ = 0.8 x $V_{OH(DC)}$.
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

AC and DC Input/Output Measurement Levels

1.1 V High speed LVCMOS (HS_LLVCMOS)

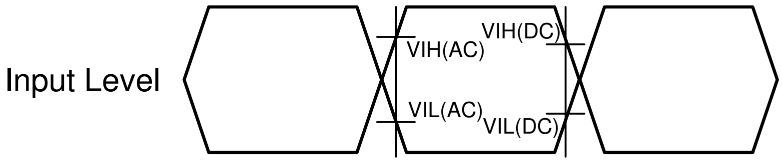
Standard specifications: All voltages are referenced to ground except where noted.

DC electrical characteristics

Table 90. Input Level for CKE

Symbol	Parameter	Value		Unit	Note
		Min.	Max.		
VIH(AC)	Input high level (AC)	0.75 x V_{DD2}	V_{DD2} + 0.2	V	1
VIL(AC)	Input low level (AC)	-0.2	0.25 x V_{DD2}	V	1
VIH(DC)	Input high level (DC)	0.65 x V_{DD2}	V_{DD2} + 0.2	V	
VIL(DC)	Input low level (DC)	-0.2	0.35 x V_{DD2}	V	

Notes:
1. Refer AC Overshoot and Undershoot.



Note:
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

▨ **Don't Care**

Figure 49. Input AC timing definition for CKE

Table 91. Input Level for Reset# and ODT_CA

Symbol	Parameter	Value		Unit	Note
		Min.	Max.		
VIH	Input high level	0.8 x V_{DD2}	V_{DD2} + 0.2	V	1
VIL	Input low level	-0.2	0.2 x V_{DD2}	V	1

Notes:

1. Refer AC Overshoot and Undershoot.

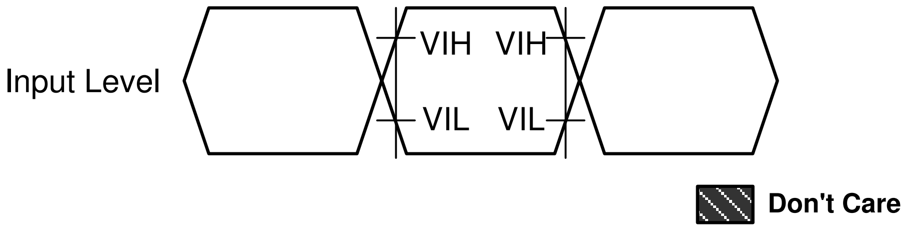


Figure 50. Input AC timing definition for Reset# and ODT_CA

Differential Input Voltage

Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK/2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK/2 is max and min peak voltage from 0V.

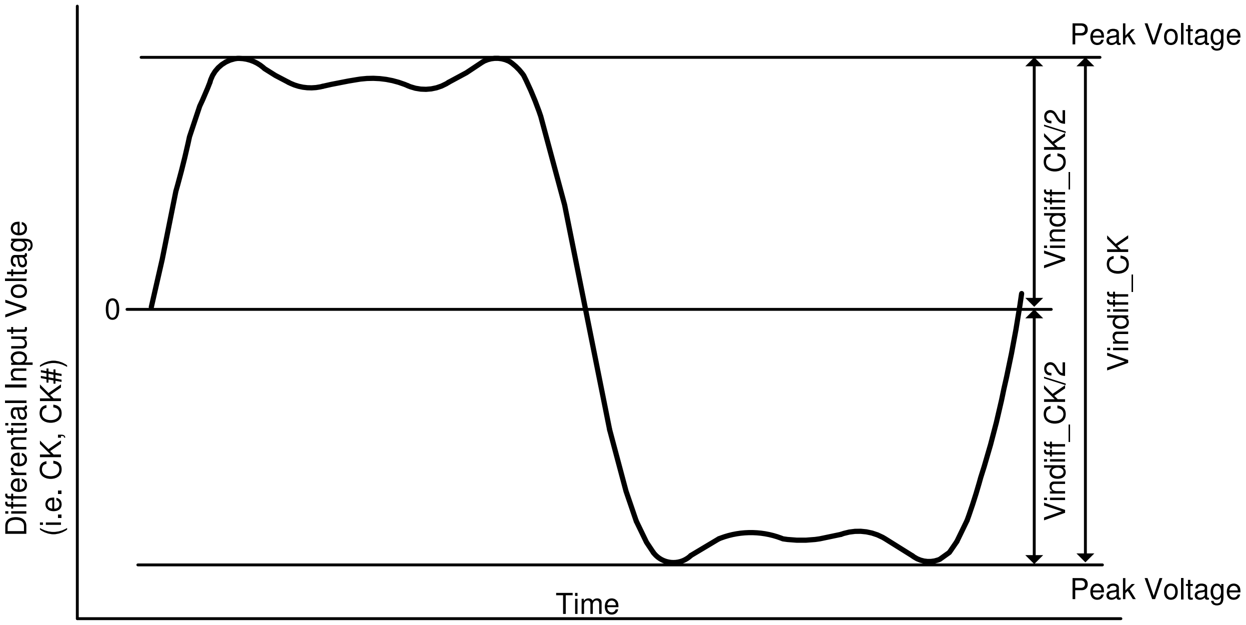


Figure 51. CK Differential Input Voltage

Table 92. CK Differential Input Voltage

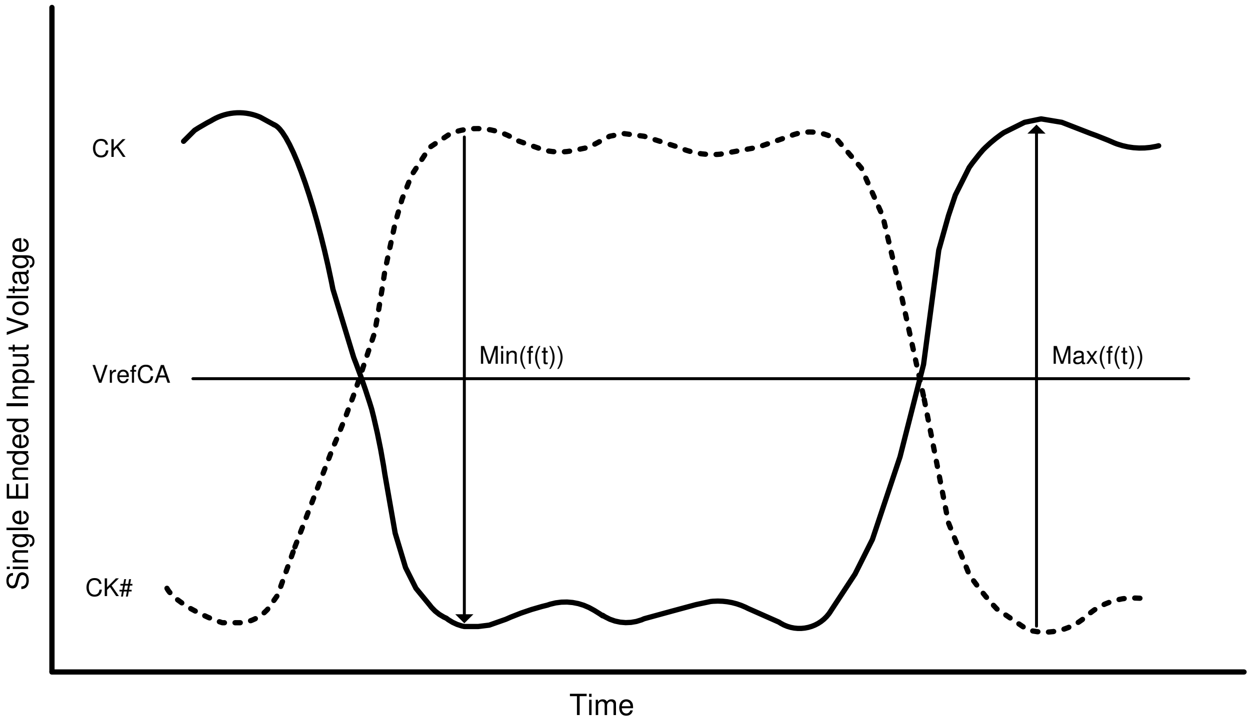
Symbol	Parameter	4266/3733		3200		Unit	Note
		Min.	Max.	Min.	Max.		
Vindiff_CK	CK differential input voltage	360	-	380	-	mV	1

Notes:

1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VCK – VCK#

Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in the following equation.
VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK – VCK#

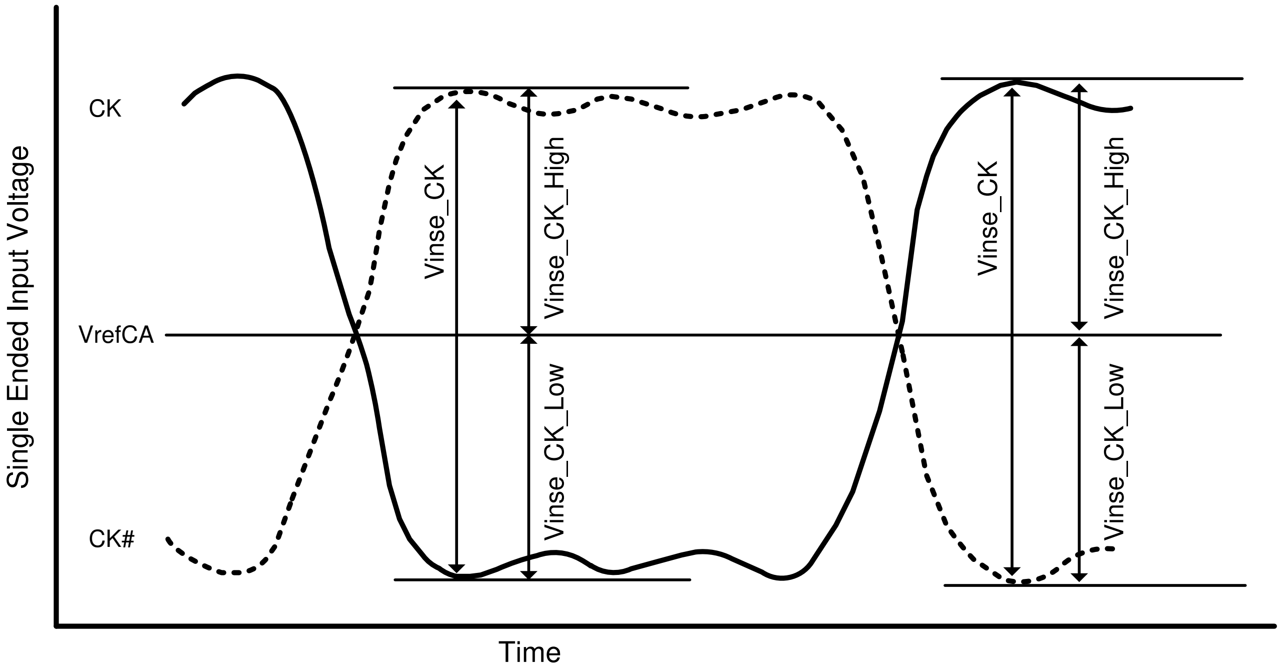


NOTES : 1. VREFCA is device internal setting value by VREF Training.

Figure 52. Definition of differential Clock Peak Voltage

Single-Ended Input Voltage for Clock

The minimum input voltage needs to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.



NOTES : 1. VREFCA is device internal setting value by VREF Training

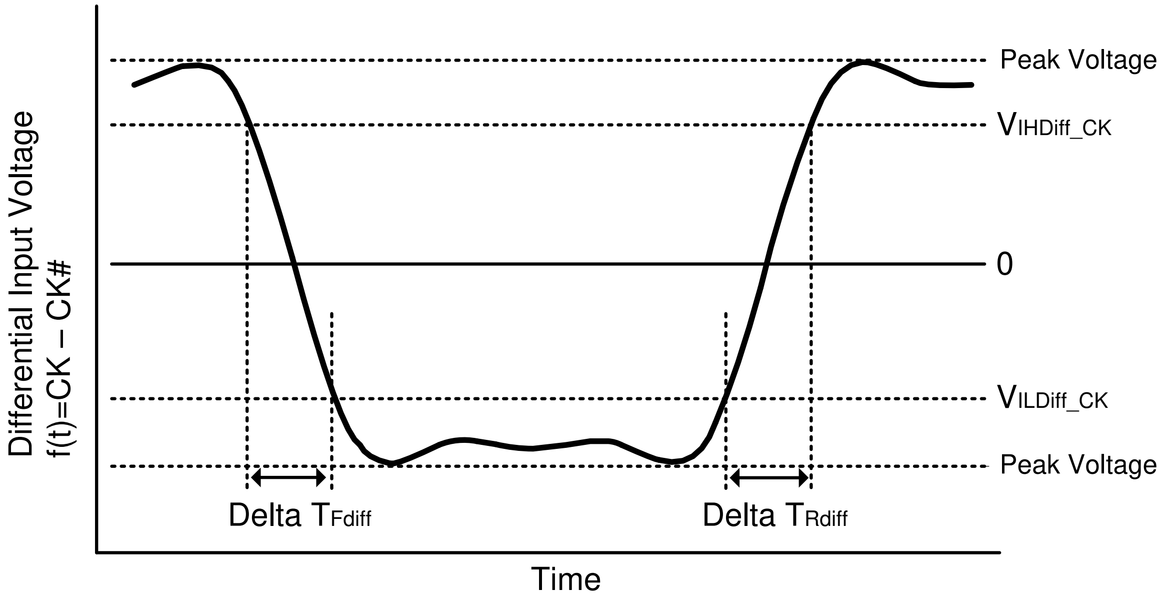
Figure 53. Clock Single-Ended Input Voltage

Table 93. Clock Single-Ended Input Voltage

Symbol	Parameter	4266/3733		3200		Unit
		Min.	Max.	Min.	Max.	
Vinse_CK	Clock Single-Ended input voltage	180	-	190	-	mV
Vinse_CK_High	Clock Single-Ended input voltage High from V_{REFDQ}	90	-	95	-	mV
Vinse_CK_Low	Clock Single-Ended input voltage High from V_{REFDQ}	90	-	95	-	mV

Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK, CK#) are defined and measured as shown below in figure and the tables.



NOTE 1. Differential signal rising edge from VILDiff_CK to VIHDiff_CK must be monotonic slope.
NOTE 2. Differential signal falling edge from VIHDiff_CK to VILDiff_CK must be monotonic slope.

Figure 54. Differential Input Slew Rate Definition for CK, CK#

Table 94. Differential Input Slew Rate Definition for CK, CK#

Description	From	To	Defined by
Differential input slew rate for rising edge (CK – CK#)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge (CK – CK#)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTFdiff

Table 95. Differential Input Level for CK, CK#

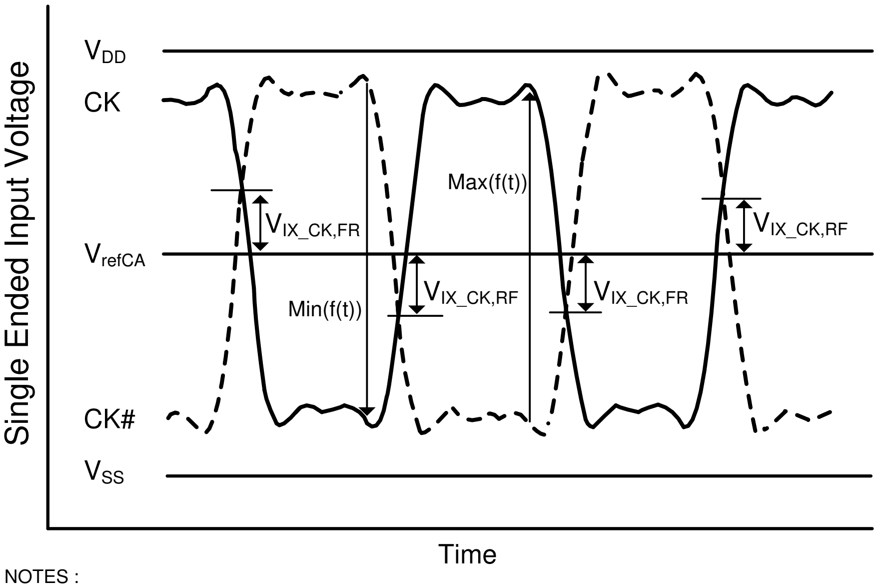
Symbol	Parameter	4266/3733		3200		Unit
		Min.	Max.	Min.	Max.	
VIHdiff_CK	Differential Input High	145	-	155	-	mV
VILdiff_CK	Differential Input Low	-	-145	-	-155	mV

Table 96. Differential Input Slew Rate Definition for CK, CK#

Symbol	Parameter	4266/3733/3200		Unit
		Min.	Max.	
SRIdiff_CK	Differential Input Slew Rate for Clock	2	14	V/ns

Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK, CK#) must meet the requirements in table below. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid level that is $V_{REF(CA)}$.



NOTES :
1. The base level of Vix_CK_FR/RF is VREFCA that is device internal setting value by VREF Training.

Figure 55. Vix Definition (Clock)

Table 97. Cross point voltage for differential input signals (Clock)

Symbol	Parameter	4266/3733/3200		Unit	Note
		Min.	Max.		
Vix_CK_ratio	Clock Differential input cross point voltage ratio	-	25	%	1-5

Notes:
1. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
2. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
3. Vix_CK_FR is defined as delta between cross point (CK fall, CK# rise) to Min(f(t))/2.
4. Vix_CK_RF is defined as delta between cross point (CK rise, CK# fall) to Max(f(t))/2.
5. In LPDDR4X un-terminated case, CK mid-level is calculated as: High level＝VDDQ, Low level=VSS, Mid-level = VDDQ/2.

Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS/2 specification at input receiver and their measurement period is 1UI (tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS/2 is max and min peak voltage from 0V.

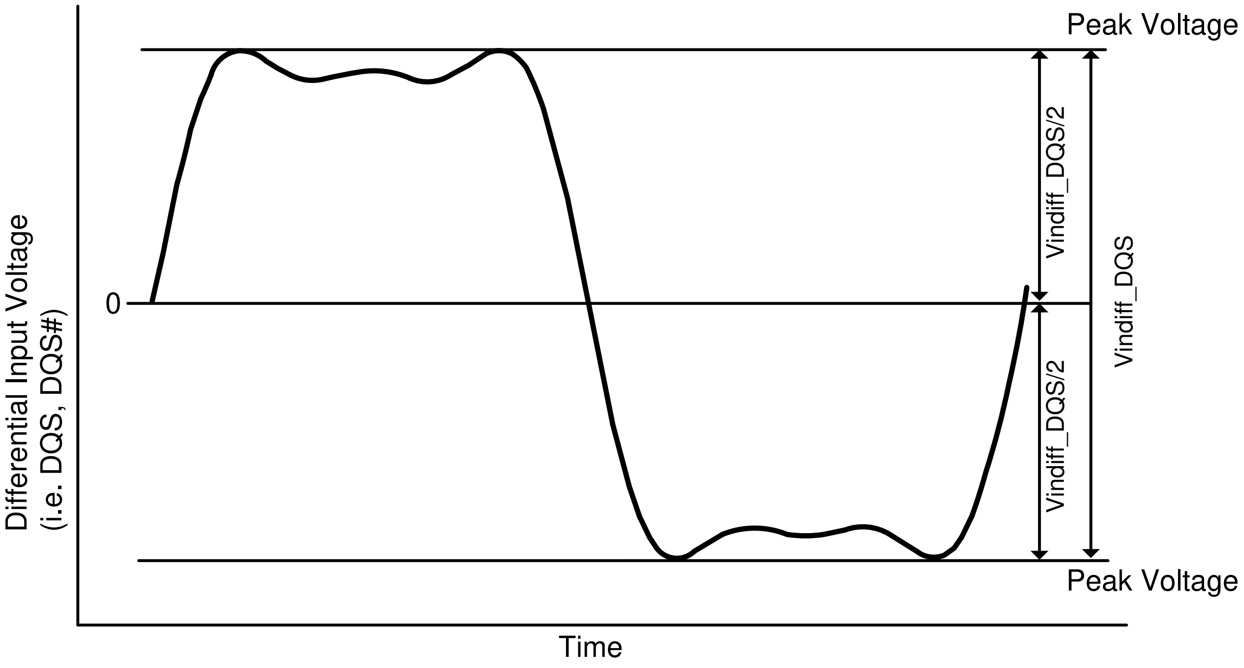


Figure 56. DQS Differential Input Voltage

Table 98. DQS Differential Input Voltage

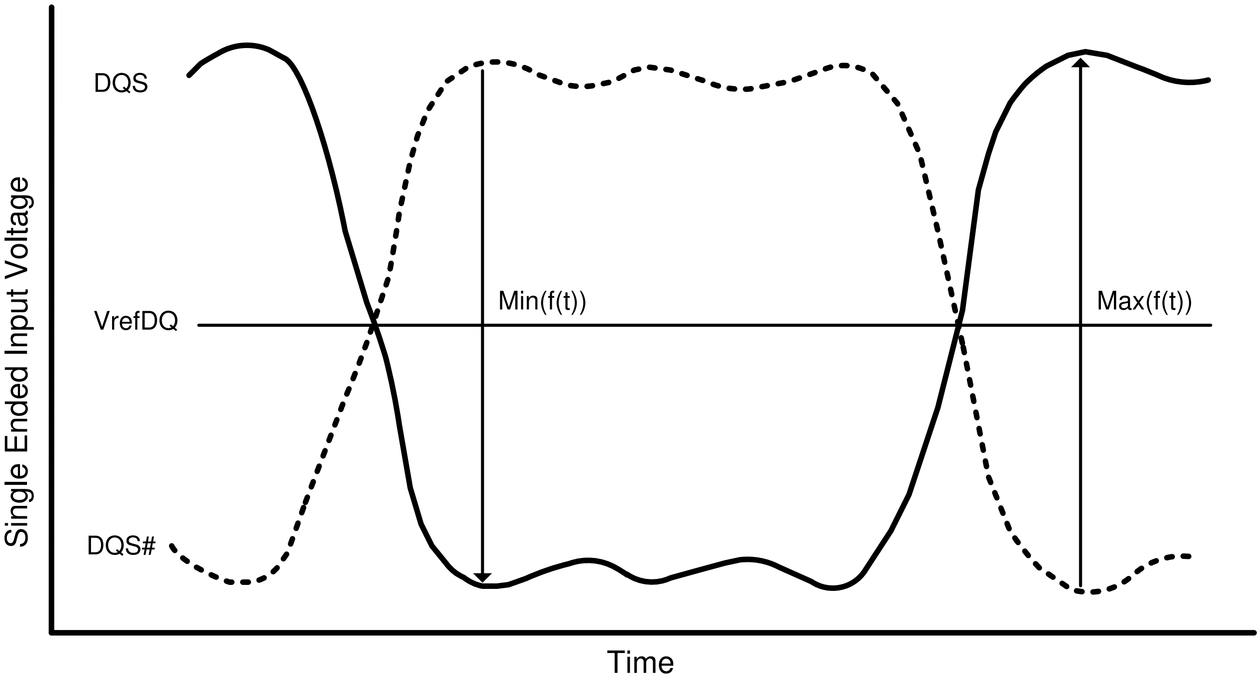
Symbol	Parameter	4266/3733		3200		Unit	Note
		Min.	Max.	Min.	Max.		
Vindiff_DQS	DQS differential input	340	-	360	-	mV	1

Notes:

1. The peak voltage of Differential DQS signals is calculated in a following equation.
   Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VDQS – VDQS#

Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.
VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VDQS – VDQS#

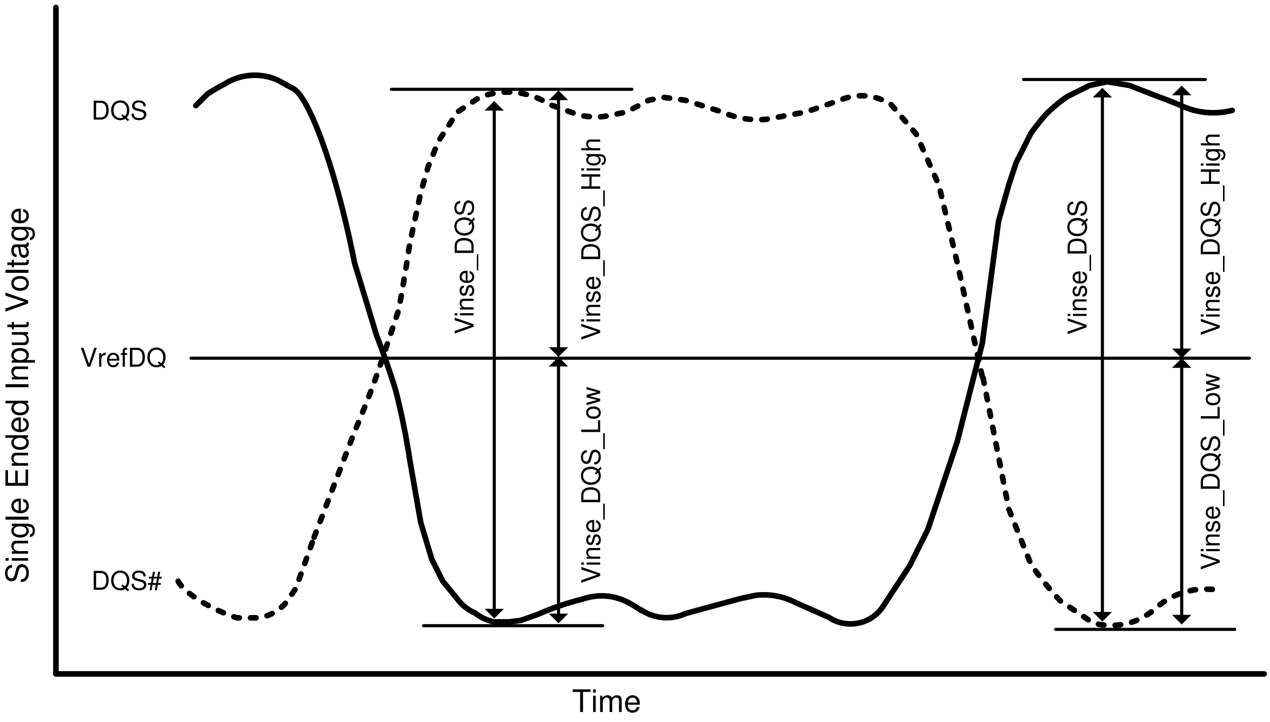


NOTES : 1. VrefDQ is device internal setting value by Vref Training.

Figure 57. Definition of differential DQS Peak Voltage

Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both Vinse_DQS, Vinse_DQS_High/Low specification at input receiver.



NOTES : 1. VrefDQ is device internal setting value by Vref Training.

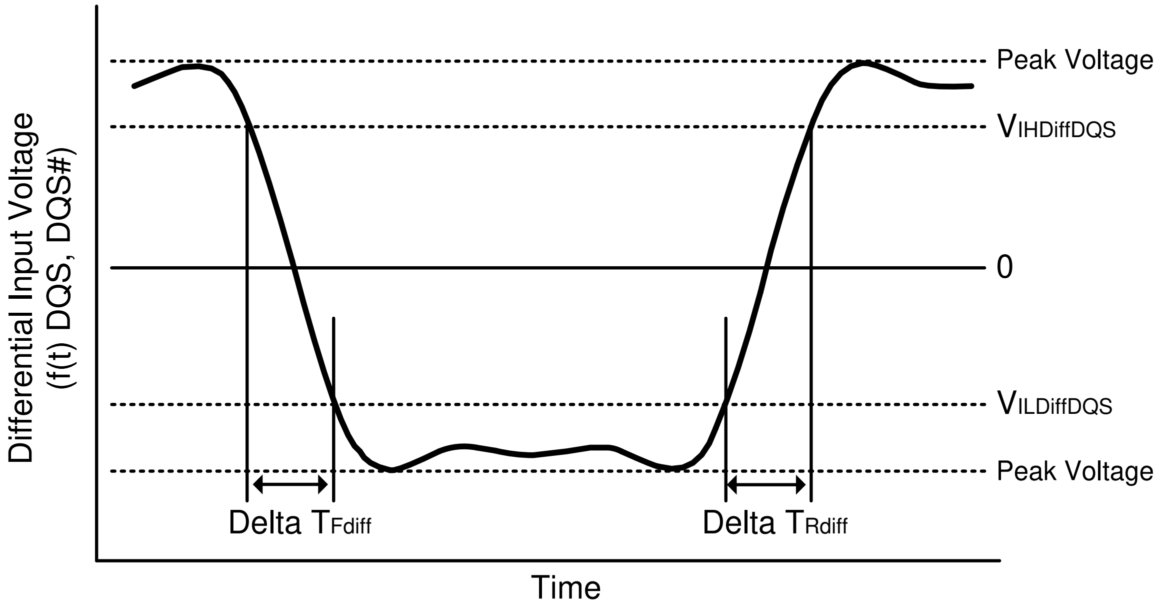
Figure 58. DQS Single-Ended Input Voltage

Table 99. DQS Single-Ended Input Voltage

Symbol	Parameter	4266/3733		3200		Unit
		Min.	Max.	Min.	Max.	
Vinse_DQS	DQS Single-Ended input voltage	170	-	180	-	mV
Vinse_DQS_High	DQS Single-Ended input voltage High from VREFDQ	85	-	90	-	mV
Vinse_DQS_Low	DQS Single-Ended input voltage Low from VREFDQ	85	-	90	-	mV

Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS, DQS#) are defined and measured as shown below in figure and the tables.



NOTE 1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
NOTE 2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Figure 59. Differential Input Slew Rate Definition for DQS, DQS#

Table 100. Differential Input Slew Rate Definition for DQS, DQS#

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS – DQS#)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS – DQS#)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTFdiff

Table 101. Differential Input Level for DQS, DQS#

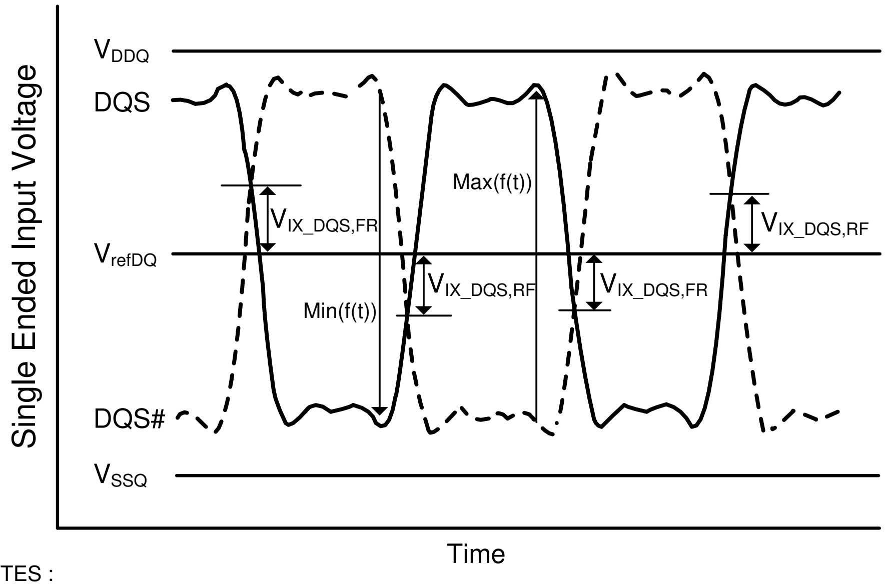
Symbol	Parameter	4266/3733		3200		Unit
		Min.	Max.	Min.	Max.	
VIHdiff_DQS	Differential Input High	120	-	140	-	mV
VILdiff_DQS	Differential Input Low	-	-120	-	-140	mV

Table 102. Differential Input Slew Rate Definition for DQS, DQS#

Symbol	Parameter	4266/3733/3200		Unit
		Min.	Max.	
SRIdiff	Differential Input Slew Rate	2	14	V/ns

Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS, DQS#) must meet the requirements in table below. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid level that is V_{REFDQ}.



NOTES :
1. The base level of Vix_DQS_FR/RF is VrefDQ that is device internal setting value by Vref Training.

Figure 60. Vix Definition (DQS)

Table 103. Cross point voltage for differential input signals (DQS)

Symbol	Parameter	4266/3733/3200		Unit	Note
		Min.	Max.		
Vix_DQS_ratio	DQS Differential input cross point voltage ratio	-	20	%	1,2

Notes:
1. Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_FR/|Min(f(t))|
2. Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_RF/Max(f(t))

Input level for ODT Input

Table 104. Input Level for ODT(CA)

Symbol	Parameter	Value		Unit
		Min.	Max.	
VIHODT	ODT Input high level	0.75 x V_{DD2}	V_{DD2} + 0.2	V
VILODT	ODT Input low level	-0.2	0.25 x V_{DD2}	V

Overshoot and Undershoot Specifications

Table 105. AC Overshoot/Undershoot

Parameter	4266/3733/3200	Unit
Maximum peak Amplitude allowed for overshoot area	0.3	V
Maximum peak Amplitude allowed for undershoot area	03	V
Maximum overshoot area above VDD/VDDQ	0.1	V-ns
Maximum undershoot area below VSS/VSSQ	0.1	V-ns

Notes:
1. VDD stands for VDD2 for CA[5:0], CK, CK#, CS, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS and DQS#.
2. VSS stands for VSS for CA[5:0], CK, CK#, CS, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS and DQS#.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

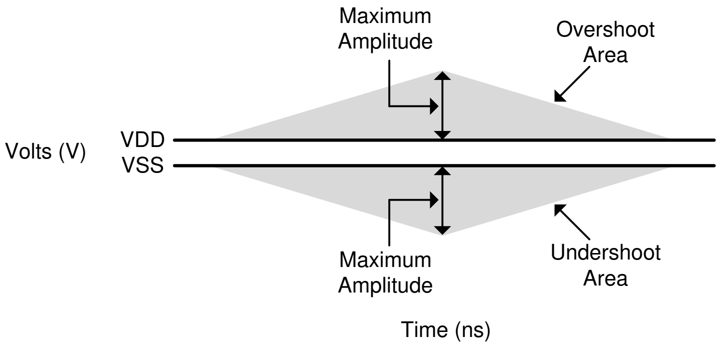


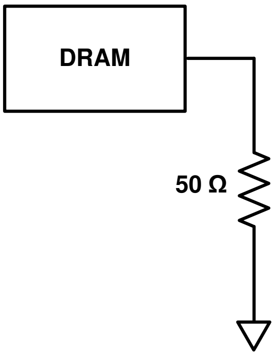
Figure 61. Overshoot and Undershoot Definition

Table 106. Overshoot/Undershoot for CKE and RESET

Parameter	Value	Unit
Maximum peak Amplitude allowed for overshoot area	0.35	V
Maximum peak Amplitude allowed for undershoot area	035	V
Maximum overshoot area above VDD	0.8	V-ns
Maximum undershoot area below VSS	0.8	V-ns

Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Note:
1. All output timing parameter values are reported with respect to this reference load.
   This reference load is also used to report slew rate.

Figure 62. Driver Output Reference Load for Timing and Slew Rate

LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator.

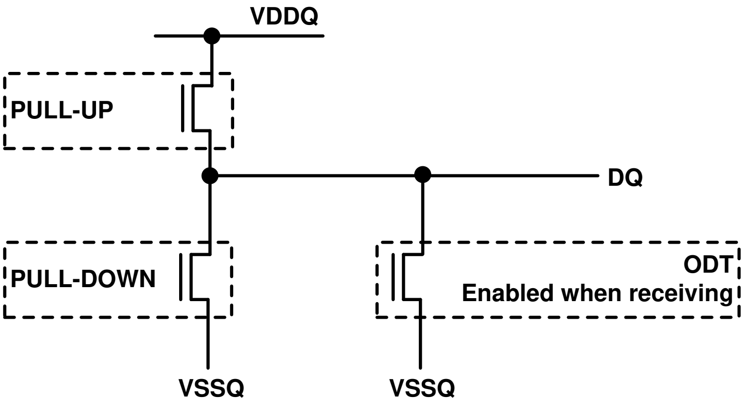


Figure 63. LVSTL I/O Cell

To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as following example:

1. First calibrate the pull-down device against a 240 Ω resister to VDDQ via the ZQ pin.
   - Set Strength Control to minimum setting.
   - Increase drive strength until comparator detects data bit is less than VDDQ/2.
   - NMOS pull-down device is calibrated to 240 Ω

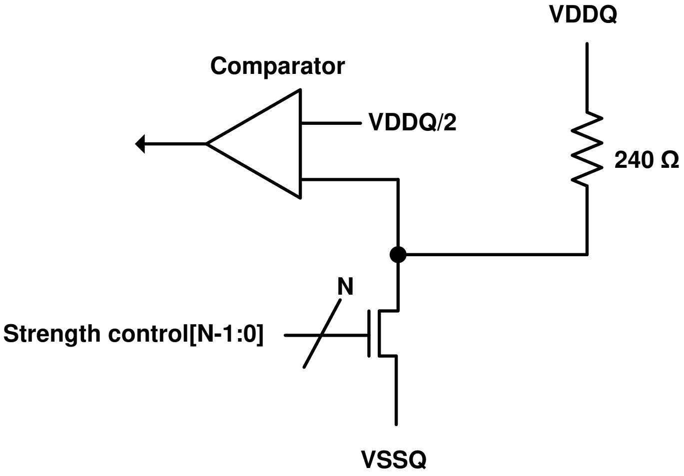


Figure 64. Pull-down calibration

2. Then calibrate the pull-up device against the calibrated pull-down device.
   - Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
   - Set Strength Control to minimum setting.
   - Increase drive strength until comparator detects data bit is greater than VOH target.
   - NMOS pull-up device is now calibrated to VOH target.

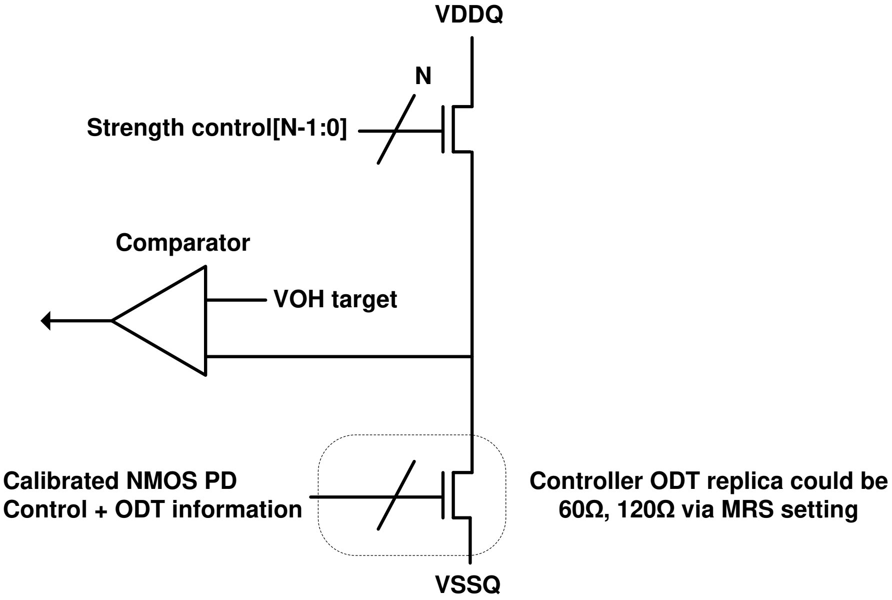


Figure 65. Pull-up calibration

CA Rx Voltage and Timing

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the CA Receiver (Rx) Mask figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

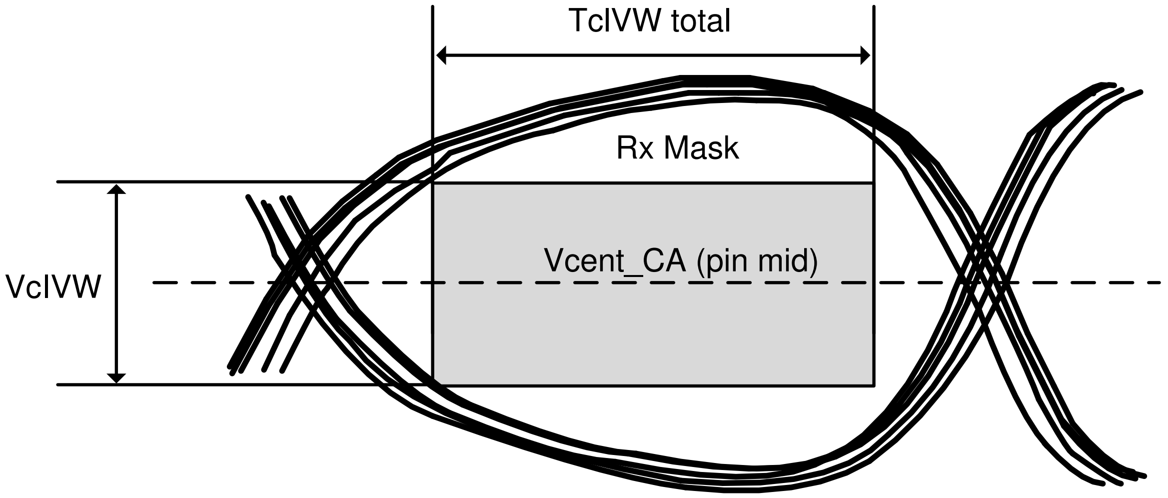


Figure 66. CA Receiver (Rx) mask

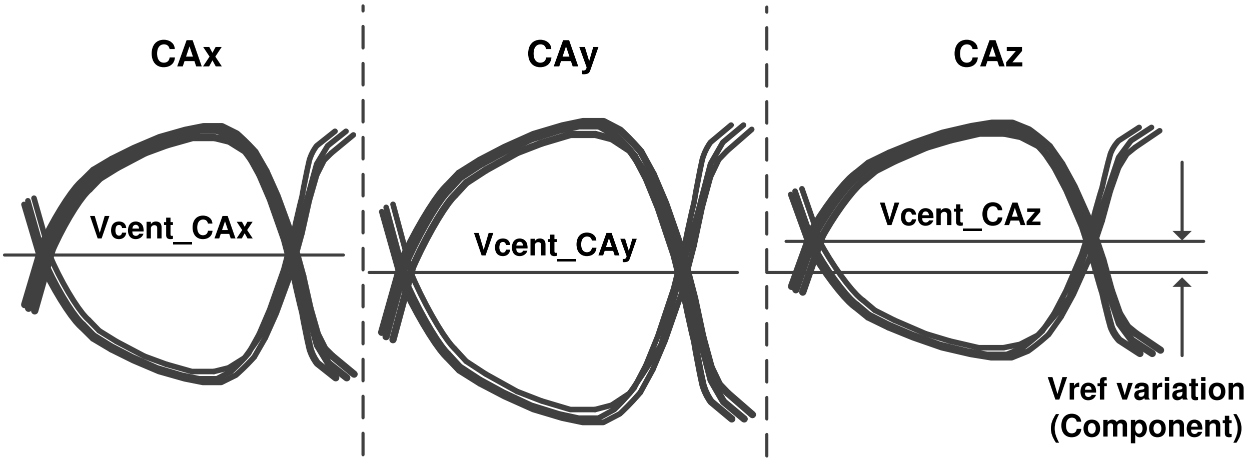


Figure 67. Across pin VREFCA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.

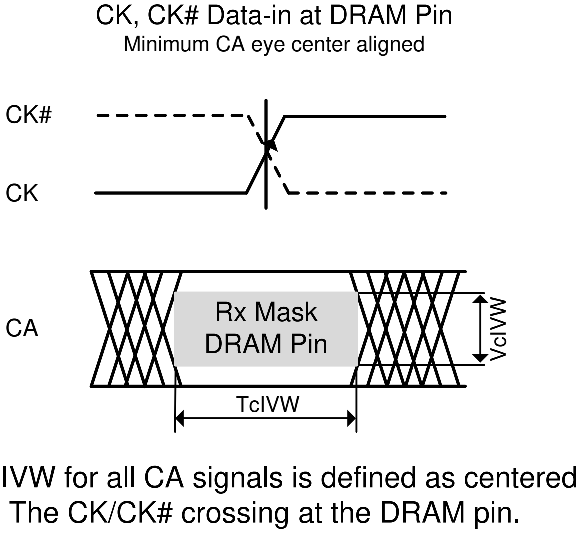
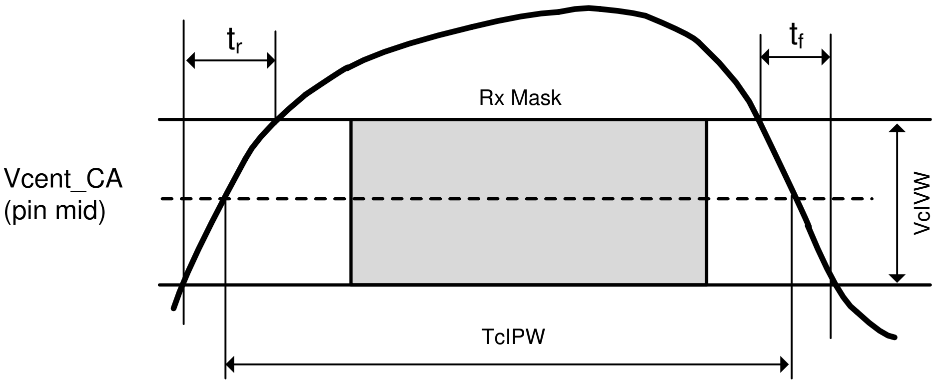


Figure 68. CA Timings at the DRAM Pins

All of the timing terms in above figure are measured from the CK/CK# to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).



NOTE:
SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 69. CA TcIPW and SRIN_cIVW definition (for each input pulse)

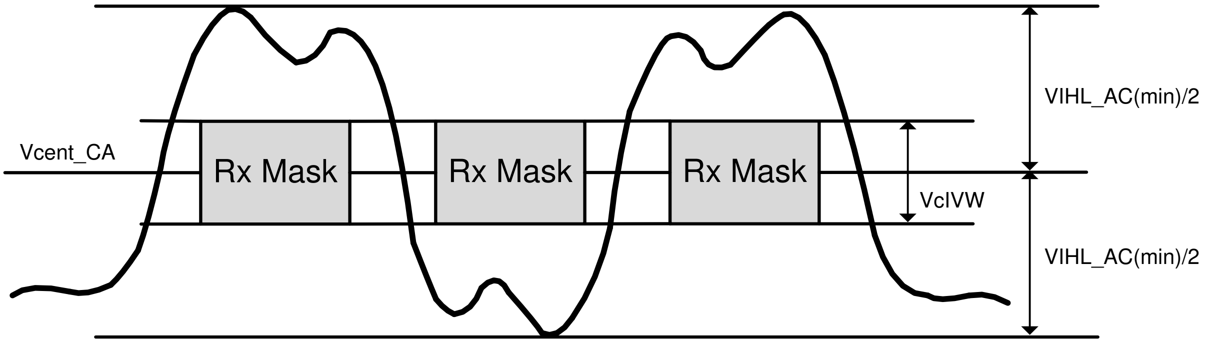


Figure 70. CA VIHL_AC definition (for each input pulse)

Table 107. DRAM CMD/ADR, CS

Symbol	Parameter	4266		3733		3200		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
VcIVW	Rx Mask voltage - p-p	-	145	-	150	-	155	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	UI	1-4
VIHL_AC	CA AC input pulse amplitude pk-pk	180	-	180	-	190	-	mV	5,8
TcIPW	CA input pulse width	0.6	-	0.6	-	0.6	-	UI	6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	V/ns	7

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal Vref range. The Rx mask at the pin must be within the internal Vref CA range irrespective of the input signal common mode.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
8. VIHL_AC does not have to be met when no transitions are occurring.
9. UI=tck(avg)min

DRAM Data Timing

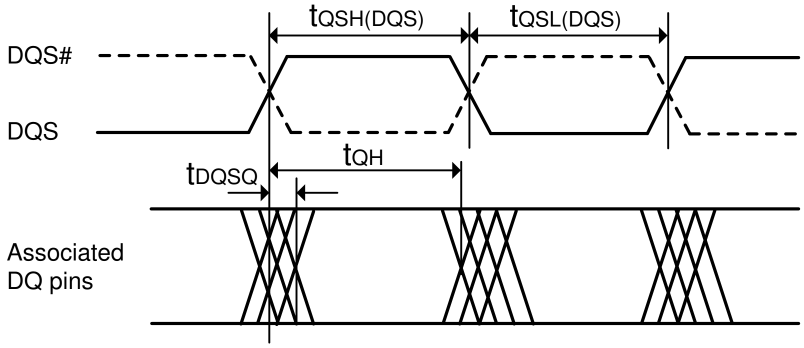


Figure 71. Read data timing definitions tQH and tDQSQ across all DQ signals per DQS group

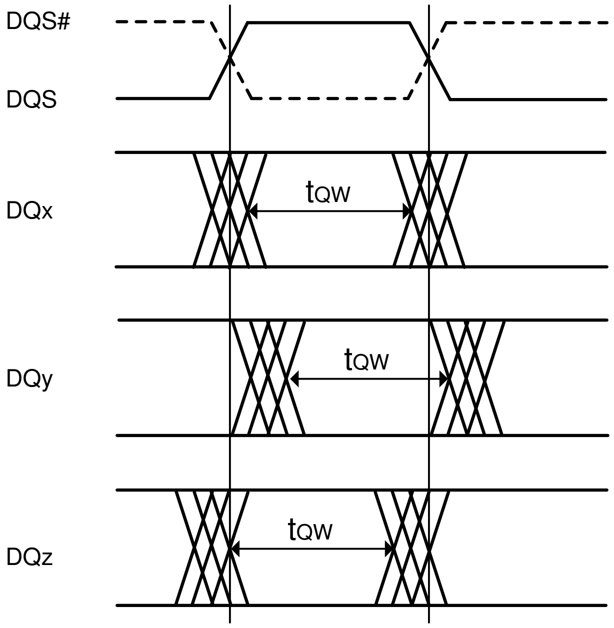


Figure 72. Read Data Timing tQW Valid Window Defined per DQ Signal

DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the figure below. The “total” mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

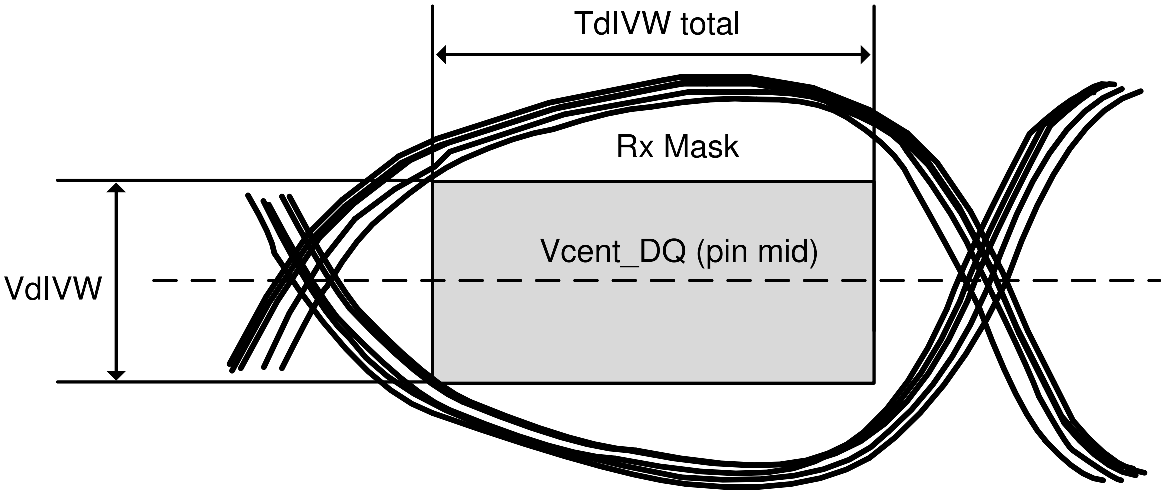


Figure 73. DQ Receiver (Rx) Mask

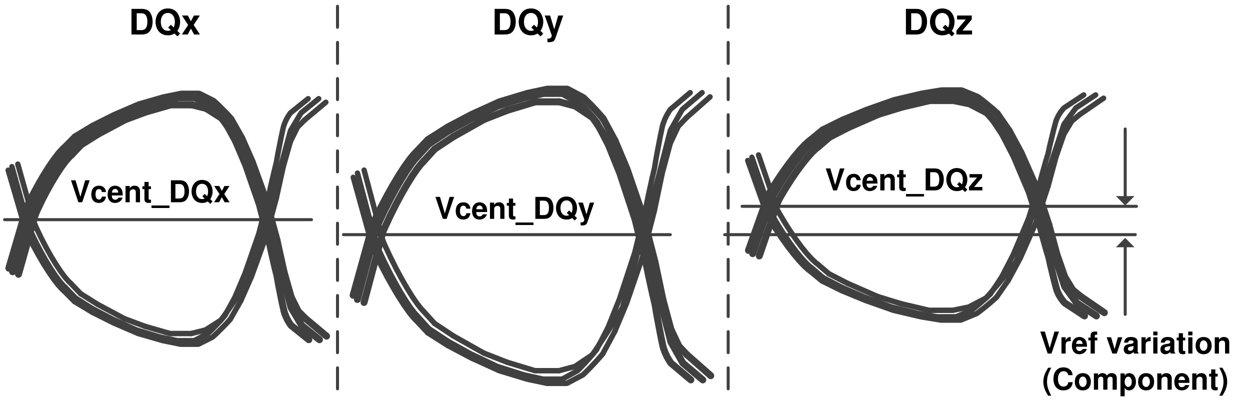
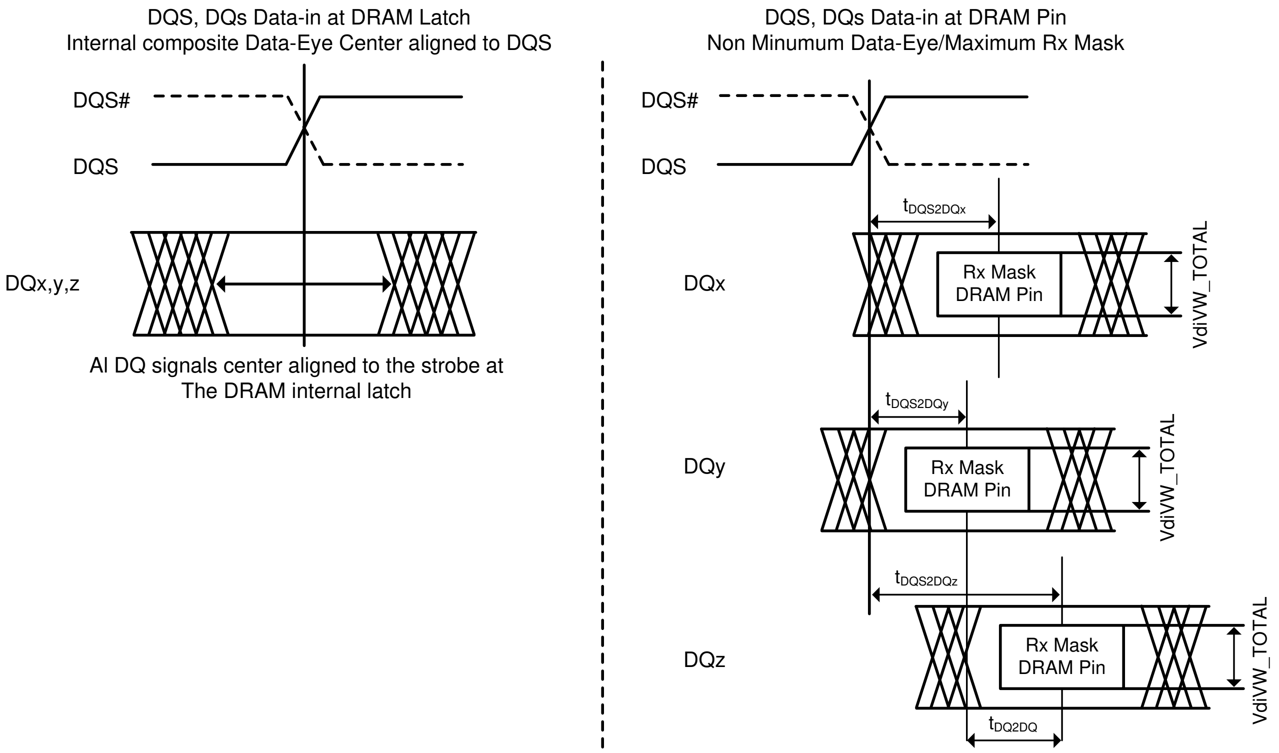


Figure 74. Across Pin Vref DQ Voltage Variation

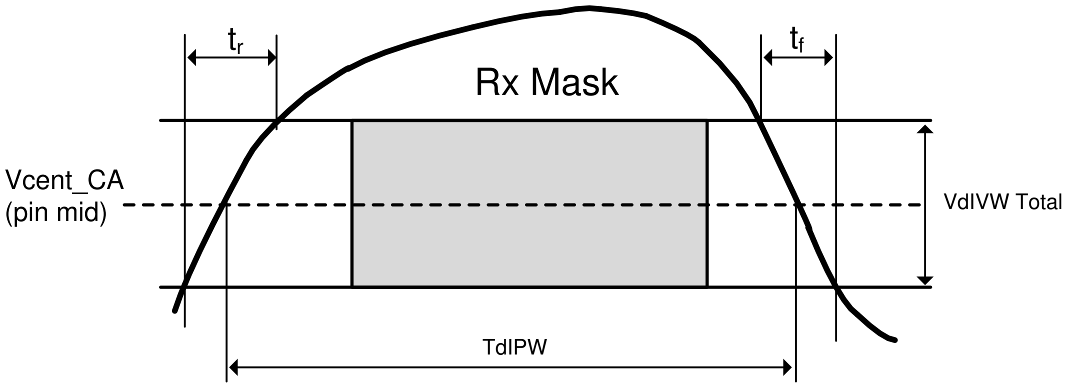
Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.



NOTE:

1. The tDQS2DQ is measured at the center(midpoint) of the TdiVW window.
2. The DQz represents the max tDQS2DQ in this example.
3. DQy represents the min tDQS2DQ in this example.

Figure 75. DQ to DQS tDQS2DQ and tDQ2DQ Timings at the DRAM pins referenced from the internal latch



NOTE:
SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 76. DQ TdIPW and SRIN_dIVW definition (for each input pulse)

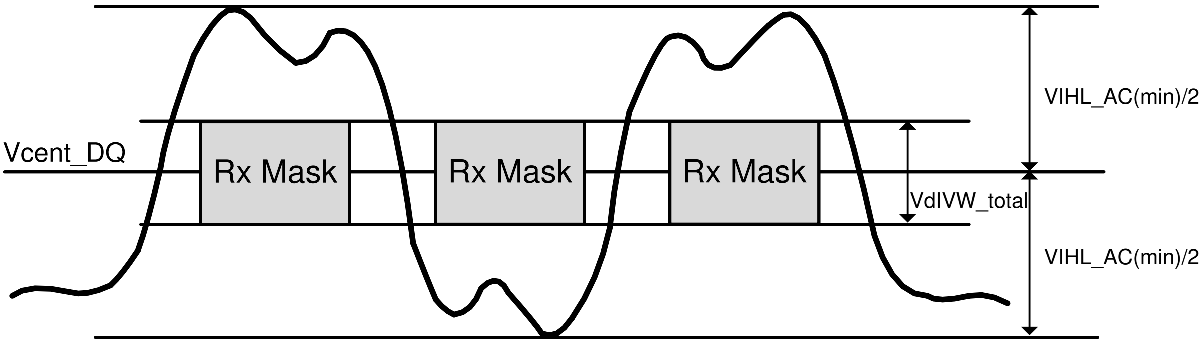


Figure 77. DQ VIHL_AC definition (for each input pulse)

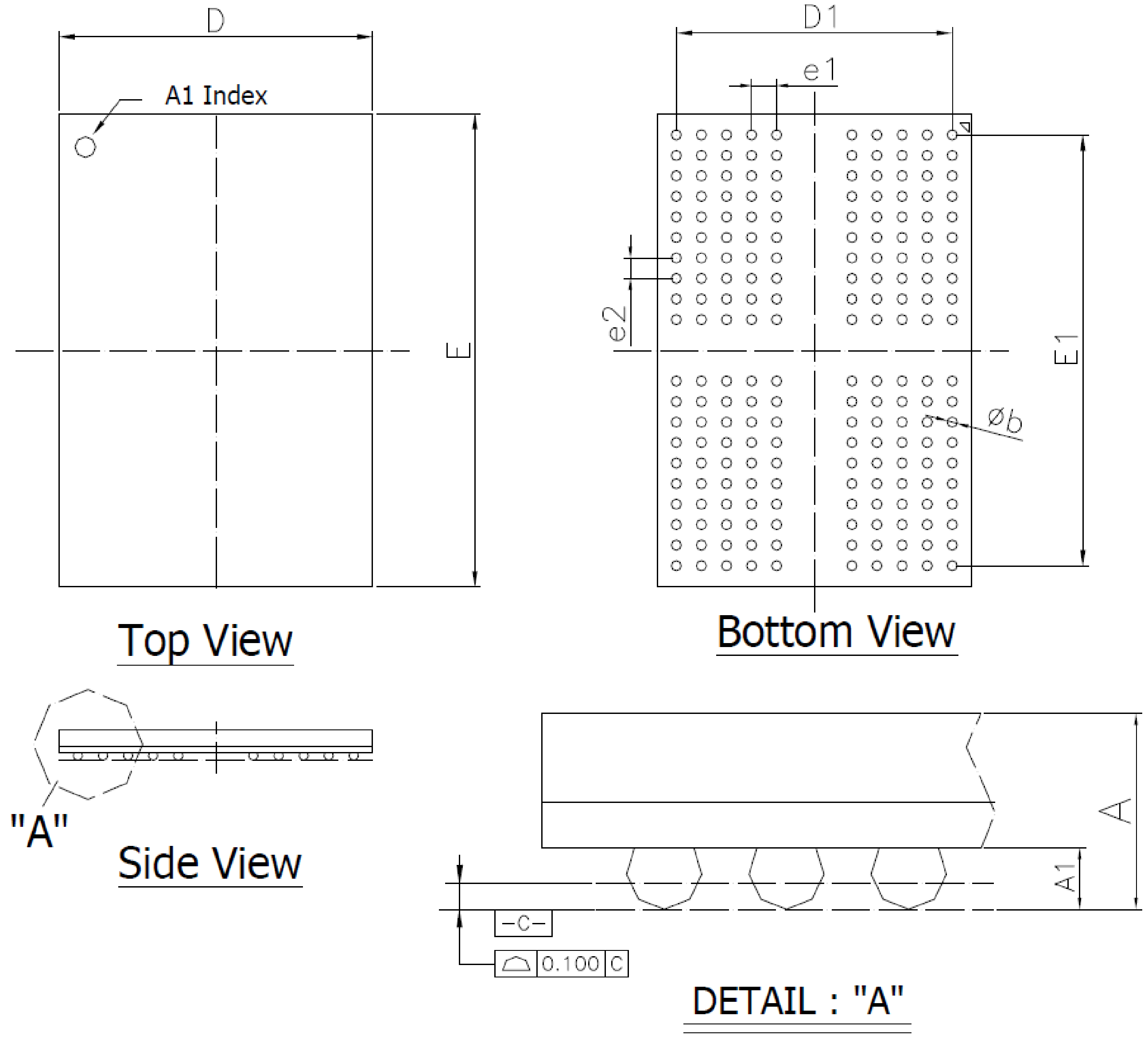
Table 108. DRAM DQs In Receive Mode (Unit UI = tCK(avg)min/2)

Symbol	Parameter	4266		3733		3200		Unit	Note
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
V_{dIVW_total}	Rx Mask voltage - p-p total	-	120	-	140	-	140	mV	1-4
T_{dIVW_total}	Rx timing window total (At VdIVW voltage levels)	-	0.25	-	0.25	-	0.25	UI	1,2,4
T_{dIVW_1bit}	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	UI	1,2,4,12
V_{IHL_AC}	DQ AC input pulse amplitude pk-pk	170	-	180	-	180	-	mV	5,13
$T_{dIPW\ DQ}$	Input pulse width (At Vcent_DQ)	0.45	-	0.45	-	0.45	-	UI	6
t_{DQS2DQ}	DQ to DQS offset	200	800	200	800	200	800	ps	7
t_{DQ2DQ}	DQ to DQ offset	-	30	-	30	-	30	ps	8
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	ps/°C	9
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation	-	33	-	33	-	33	ps/ 50mV	10
S_{RIN_dIVW}	Input Slew Rate over VdIVWJotal	1	7	1	7	1	7	V/ns	11
$t_{DQS2DQ\_rank2rank}$	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	ps	14,15

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.0354	0.0394	0.0433	0.90	1.00	1.10
A1	0.0009	0.0114	0.0134	0.24	0.29	0.34
D	0.3898	0.3937	0.3976	9.90	10.00	10.10
E	0.5669	0.5709	0.5748	14.40	14.50	14.60
D1	--	0.3465	--	--	8.80	--
E1	--	0.5374	--	--	13.65	--
e1	--	0.0315	--	--	0.80	--
e2	--	0.0256	--	--	0.65	--
b	0.0150	0.0169	0.0189	0.38	0.43	0.48

Figure 78. 200-Ball FBGA Package 10x14.5x1.1mm (max)