

## 1024M x 16 bit DDR4 Synchronous DRAM (SDRAM)

Advance (Rev. 1.0, Sep. /2024)

### Features

- JEDEC Standard Compliant
- Fast clock rate: 1600MHz
- Power supplies:
  - $V_{DD}$  &  $V_{DDQ}$  =  $+1.2V \pm 0.06V$
  - $V_{PP}$  =  $+2.5V -0.125V / +0.25V$
- Operating temperature range: (Commercial)
  - Normal operating temperature:  $T_C = 0\text{~}85^\circ\text{C}$
  - Extended temperature:  $T_C = 85\text{~}95^\circ\text{C}$
- Supports JEDEC clock jitter specification
- Bidirectional differential data strobe, DQS &DQS#
- Differential Clock, CK & CK#
- 8 internal banks: 2 groups of 4 banks each
- Separated IO gating structures by Bank Group
- 8n-bit prefetch architecture
- Precharge & Active power down
- Auto Refresh and Self Refresh
- Low-power auto self refresh (LPASR)
- Self Refresh Abort
- Fine Granularity Refresh
- Dynamic ODT (RTT\_PARK & RTT\_Nom & RTT\_WR)
- Write Leveling
- DQ Training via MPR
- Programmable preamble is supported both of  $1t_{CK}$  and  $2t_{CK}$  mode
- Command/Address (CA) Parity
- Data bus write cyclic redundancy check (CRC)
- Boundary Scan Mode
- Internal  $V_{REFDQ}$  Training
- Read Preamble Training
- Control Gear Down Mode
- Per DRAM Addressability (PDA)
- Output Driver Impedance Control
- Dynamic on-die termination (ODT)
- Input Data Mask (DM) and Data Bus Inversion (DBI)
- ZQ Calibration
- Command/Address latency (CAL)
- Asynchronous Reset
- DLL enable/disable
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Burst type: Sequential / Interleave
- CAS Latency (CL)
- CAS Write Latency (CWL)
- Additive Latency (AL): 0, CL-1, CL-2
- Average refresh period
  - 8192 cycles/64ms (7.8us at  $0^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ )
  - 8192 cycles/32ms (3.9us at  $+85^\circ\text{C} \leq T_C \leq +95^\circ\text{C}$ )
- Data Interface: Pseudo Open Drain (POD)
- RoHS compliant
- Hard post package repair (hPPR)
- Soft post package repair (sPPR)
- Package: Pb Free and Halogen Free
  - 96-ball 7.5 x 13 x 1.2mm FBGA

**Table 1. Ordering Information**

Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6OG16NWBB-62H	1600MHz	3200Mbps/pin	$V_{DD}/V_{DDQ} 1.2V, V_{PP} 2.5V$	FBGA

WB: indicates 7.5 x 13 x 1.2mm FBGA Package

B: indicates Generation Code

H: indicates Pb and Halogen Free

**Table 2. Speed Grade Information**

Speed Grade	Clock Frequency	CAS Latency	$t_{RCD}$ (ns)	$t_{RP}$ (ns)
DDR4-3200	1600MHz	22	13.75	13.75

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## Ball Assignment

	1	2	3	...	7	8	9
A	VDDQ	VSSQ	DQ8		UDQS#	VSSQ	VDDQ
B	VPP	VSS	VDD		UDQS	DQ9	VDD
C	VDDQ	DQ12	DQ10		DQ11	DQ13	VSSQ
D	VDD	VSSQ	DQ14		DQ15	VSSQ	VDDQ
E	VSS	UDM#/ UDBI#	VSSQ		LDM#/ LDBI#	VSSQ	VSS
F	VSSQ	VDDQ	LDQS#		DQ1	VDDQ	ZQ
G	VDDQ	DQ0	LDQS		VDD	VSS	VDDQ
H	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ
J	VDD	VDDQ	DQ6		DQ7	VDDQ	VDD
K	VSS	CKE	ODT		CK	CK#	VSS
L	VDD	WE#/ A14	ACT#		CS#	RAS#/ A16	VDD
M	VREFCA	BG0	A10/AP		A12/ BC#	CAS#/ A15	VSS
N	VSS	BA0	A4		A3	BA1	TEN
P	Reset#	A6	A0		A1	A5	Alert#
R	VDD	A8	A2		A9	A7	VPP
T	VSS	A11	PAR		NC	A13	VDD

Figure 1. 96-Ball (FBGA Top View)

## Functional Block Diagram

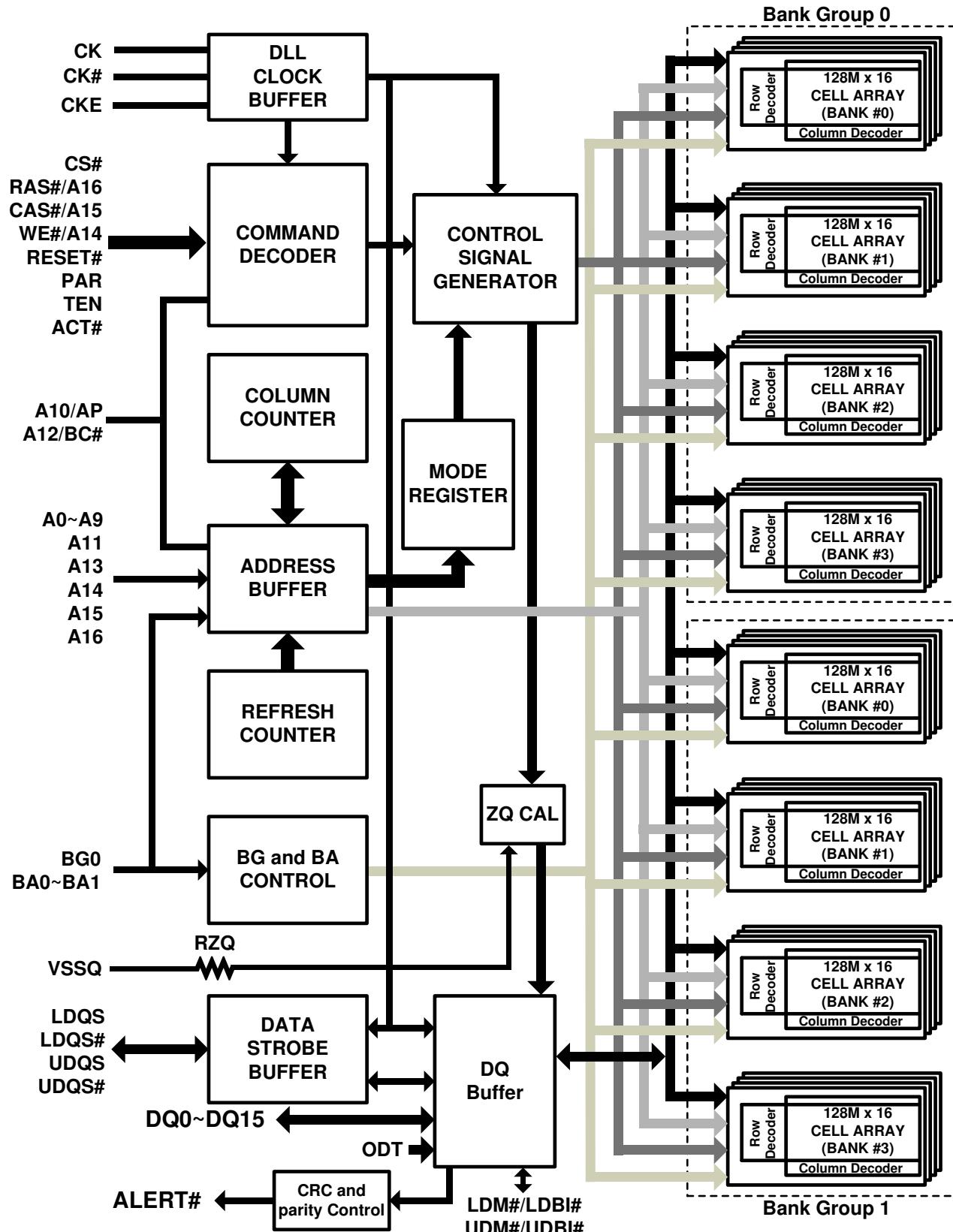


Figure 2. Block Diagram

## Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

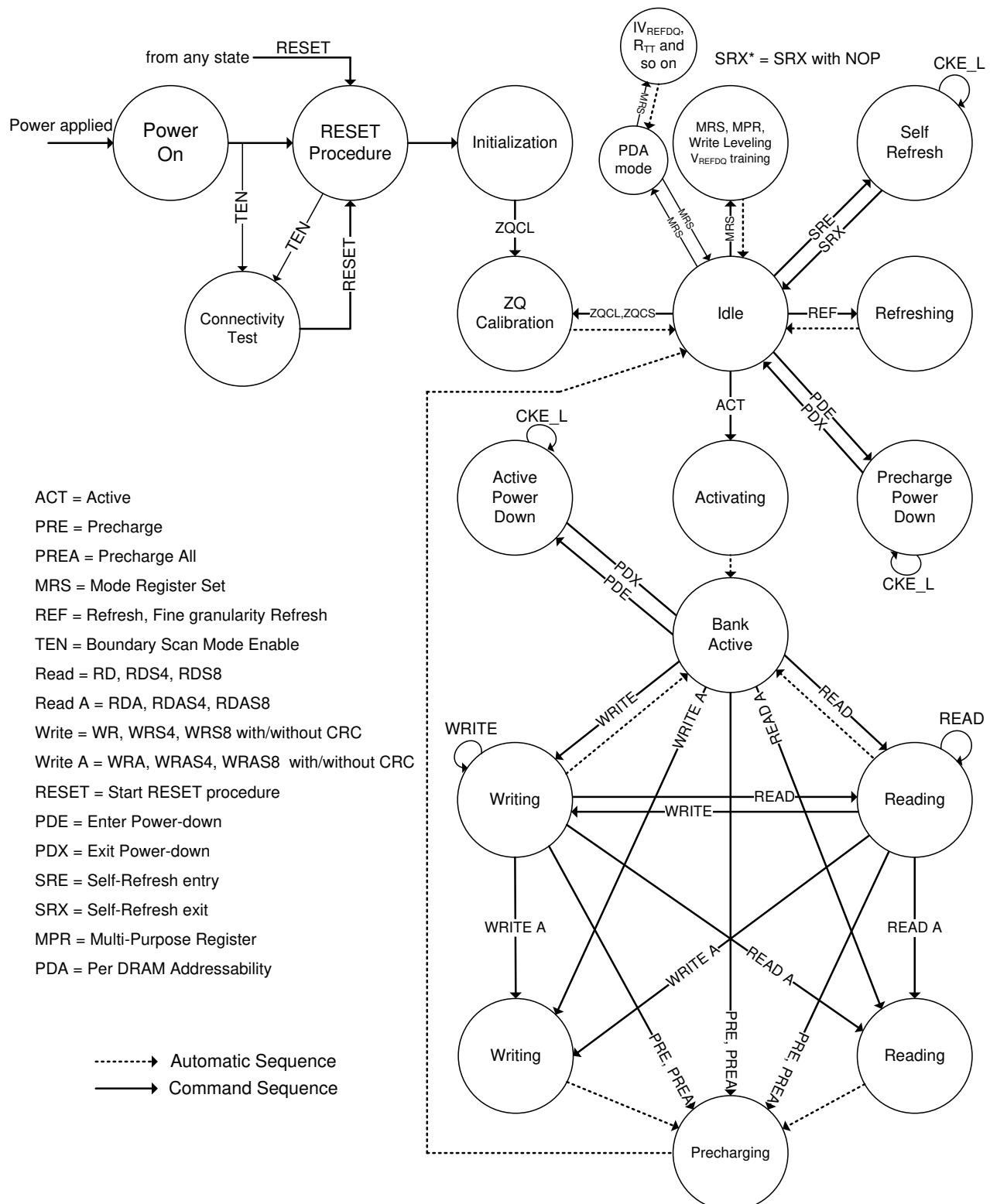


Figure 3. State Diagram

## Ball Descriptions

Table 3. Ball Details

Symbol	Type	Description
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE	Input	<b>Clock Enable:</b> CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After $V_{REFCA}$ and Internal DQ $V_{REF}$ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	<b>Chip Select:</b> All commands are masked when CS# is registered high. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	<b>On Die Termination:</b> ODT (registered high) enables $R_{TT\_NOM}$ termination resistance internal to the DDR4 SDRAM. When enabled, ODT is applied to each DQ, LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM signal. The ODT pin will be ignored if MR1 is programmed to disable $R_{TT\_NOM}$ .
ACT#	Input	<b>Activation Command Input:</b> ACT# defines the Activation command being entered along with CS#. The input into RAS#/A16, CAS#/A15 and WE#/A14 will be considered as Row Address A16, A15 and A14.
RAS#/A16 CAS#/A15 WE#/A14	Input	<b>Command Inputs:</b> RAS#/A16, CAS#/A15 and WE#/A14 (along with CS#) define the command being entered. Those pins have multi function. For example, for activation with ACT# low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT# high, those are Command pins for Read, Write and other command defined in command truth table.
LDM#/LDBI# UDM#/UDBI#	Input / Output	<b>Input Data Mask and Data Bus Inversion:</b> DM# is an input mask signal for write data. Input data is masked when DM# is sampled low coincident with that input data during a Write access. DM# is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. DBI# is an input /output identifying whether to store/output the true or inverted data. If DBI# is low the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI# is high.
BG0	Input	<b>Bank Group Inputs:</b> BG0 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0-BA1	Input	<b>Bank Address:</b> BA0-BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A16	Input	<b>Address Inputs:</b> Provide the row address (A0~A16) for Activate Commands and the column address (A0~A9) for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC#, RAS#/A16, CAS#/A15 and WE#/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A15 and A16 are used on some higher densities.
A10/AP	Input	<b>Auto-precharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (high: Autoprecharge; low: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by bank addresses.

A12/BC#	Input	<b>Burst Chop:</b> A12/BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (high, no burst chop; low: burst chopped). See command truth table for details.
Reset#	Input	<b>Active Low Asynchronous Reset:</b> Reset is active when Reset# is low, and inactive when Reset# is high. Reset# must be high during normal operation. Reset# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of $V_{DD}$ .
DQ0-DQ15	Input / Output	<b>Data Input/ Output:</b> Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal $V_{REF}$ level during test via Mode Register Setting MR4 A4=high. During this mode, $R_{TT}$ should be set Hi-Z.
LDQS, LDQS#, UDQS, UDQS#,	Input / Output	<b>Data Strobe:</b> output with read data, input with write data. Edge-aligned with read data, centered in write data. LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobe LDQS and UDQS are paired with differential signals LDQS#, and UDQS#, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	<b>Command and Address Parity Input:</b> DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT#, RAS#/A16, CAS#/A15, WE#/A14, BG0, BA0-BA1, and A16-A0. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when CS# is low.
Alert#	Input / Output	<b>Alert:</b> It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert# goes low for the period time interval and goes back high. If there is error in Command Address Parity Check, then Alert# goes low for relatively long period until ongoing DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, Alert# Pin must be bounded to $V_{DD}$ on board.
TEN	Input	<b>Connectivity Test Mode Enable:</b> Connectivity Test Mode is active when TEN is high, and inactive when TEN is low. TEN must be low during normal operation. TEN is a CMOS rail-to-rail signal with AC high and low at 80% and 20% of $V_{DD}$ (960mV for DC high and 240mV for DC low). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to $V_{SS}$ . The host controller should use good enough strength when activating connectivity test mode to avoid current fighting at TEN signal and inability of connectivity test mode.
NC	-	<b>No Connect:</b> These pins should be left unconnected.
$V_{DD}$	Supply	<b>Power Supply:</b> $+1.2V \pm 0.06V$ .
$V_{SS}$	Supply	<b>Ground</b>
$V_{DDQ}$	Supply	<b>DQ Power Supply:</b> $+1.2V \pm 0.06V$ .
$V_{SSQ}$	Supply	<b>DQ Ground</b>
$V_{PP}$	Supply	<b>DRAM Activating Power Supply:</b> $2.5V$ ( $2.375V$ min , $2.75V$ max)
$V_{REFCA}$	Supply	<b>Reference voltage for CA</b>
ZQ	Supply	<b>Reference pin for ZQ calibration.</b>

NOTE: Input only pins (BG0, BA0-BA1, A0-A16, ACT#, RAS#/A16, CAS#/A15, WE#/A14, CS#, CKE, ODT, and RESET#) do not supply termination.

## Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally organized with eight-banks (2 bank groups each with 4 banks). The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Activate Command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate Command are used to select the bank and row to be activated (BG0 select the bank group; BA0-BA1 select the bank; A0-A16 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

## Reset and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings need to be defined:

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate  
Per DRAM Addressability (MR3 A[4]) : 0 = Disable  
CS# to Command/Address Latency (MR4 A[8:6]) : 000 = Disable  
CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable  
Hard Post Package Repair mode (MR4 A[13]) : 0 = Disable  
Soft Post Package Repair mode (MR4 A[5]) : 0 = Disable

## Power-up Initialization Sequence

The following sequence is required for Power up and Initialization:

1. Apply power (Reset# and TEN are recommended to be maintained below  $0.2 \times V_{DD}$ ; all other inputs may be undefined). Reset# needs to be maintained below  $0.2 \times V_{DD}$  for minimum 200us with stable power and TEN needs to be maintained below  $0.2 \times V_{DD}$  for minimum 700us with stable power. CKE is pulled "Low" anytime before Reset# being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to  $V_{DD,min}$  must be no greater than 200ms; and during the ramp,  $V_{DD} \geq V_{DDQ}$  and  $(V_{DD}-V_{DDQ}) < 0.3$  V.  $V_{PP}$  must ramp at the same time or earlier than  $V_{DD}$  and  $V_{PP}$  must be equal to or higher than  $V_{DD}$  at all times.

During power-up, either of the following conditions may exist and must be met:

Condition A:

- $V_{DD}$  and  $V_{DDQ}$  are driven from a single power converter output, AND
- The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side. In addition,  $V_{TT}$  is limited to 0.76 V max once power ramp is finished, AND
- $V_{REFCA}$  tracks  $V_{DD}/2$ .

Condition B:

- Apply  $V_{DD}$  without any slope reversal before or at the same time as  $V_{DDQ}$
- Apply  $V_{DDQ}$  without any slope reversal before or at the same time as  $V_{TT}$  &  $V_{REFCA}$ .
- Apply  $V_{PP}$  without any slope reversal before or at the same time as  $V_{DD}$ .
- The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side.

2. After Reset# is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.

3. Clocks (CK, CK#) need to be started and stabilized for at least 10ns or  $5t_{CK}$  (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock ( $t_{IS}$ ) must be met. Also a Deselect command must be registered (with  $t_{IS}$  set up time to clock) at clock edge Td. Once the CKE registered "high" after Reset, CKE needs to be continuously registered "high" until the initialization sequence is finished, including expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as Reset# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after Reset# deassertion until CKE is registered high. The ODT input signal may be in undefined state until  $t_{IS}$  before CKE is registered high. When CKE is registered high, the ODT input signal may be statically held at either low or high. If  $R_{TT\_NOM}$  is to be enabled in MR1 the ODT input signal must be statically held low. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ .
5. After CKE is being registered high, wait minimum of Reset CKE Exit time,  $t_{XPR}$ , before issuing the first MRS command to load mode register. ( $t_{XPR} = \text{Max}(t_{XS}, 5nCK)$ )
6. Issue MRS Command to load MR3 with all application settings (To issue MRS command to MR3, provide "low" to BG0, "high" to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "low" to BA0, "high" to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "low" to BA1, "high" to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration.
14. Wait for both  $t_{DLLK}$  and  $t_{ZQinit}$  completed.
15. The DDR4 SDRAM is now ready for Read/Write training (include  $V_{REF}$  training and Write leveling).

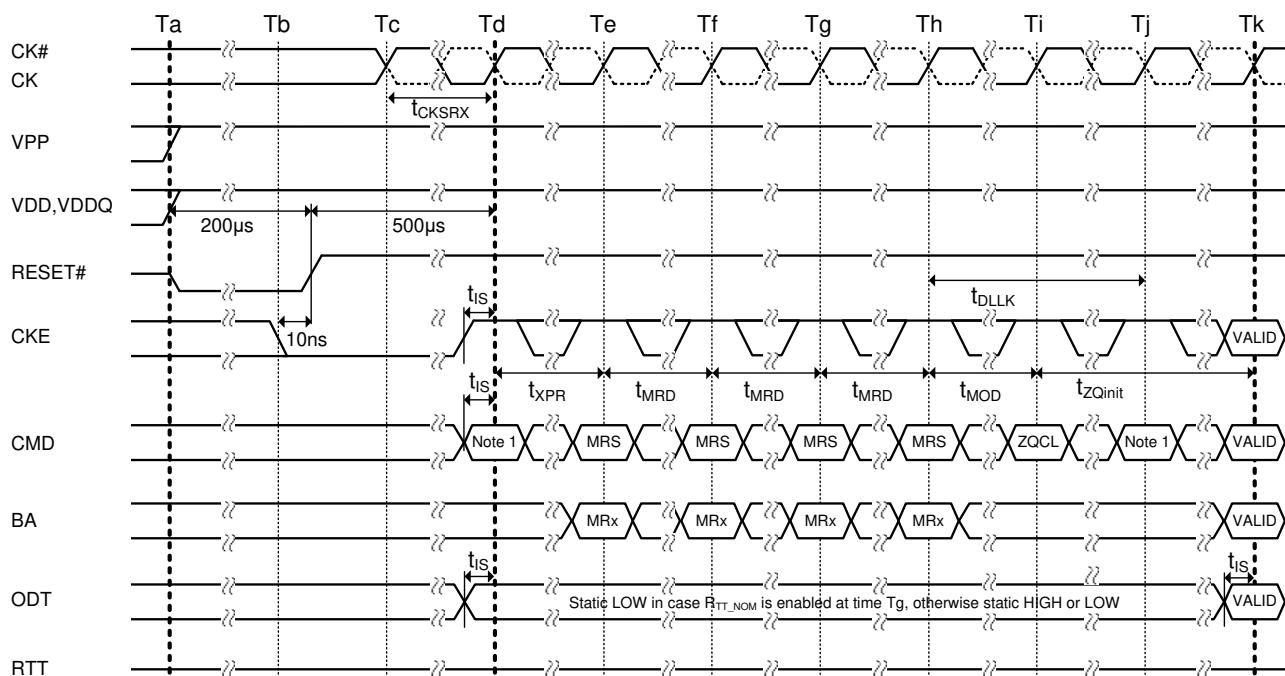


Figure 4. RESET# and Initialization Sequence at Power-on Ramping

## **V<sub>DD</sub> Slew rate at Power-up Initialization Sequence**

**Table 4.  $V_{DD}$  Slew Rate**

Symbol	Min.	Max.	Units	Notes
$V_{DD\_sl}$	0.004	600	V/ms	1,2
$V_{DD\_on}$	-	200	ms	1,3

**Notes:**

1. Measurement made between 300mv and 80%  $V_{DD}$  minimum.
2. 20 MHz bandlimited measurement.
3. Maximum time to ramp  $V_{DD}$  from 300 mV to  $V_{DD}$  minimum.

## Reset Initialization with Stable Power

The following sequence is required for Reset at no power interruption initialization:

1. Asserted Reset# below  $0.2 \times V_{DD}$  anytime when reset is needed (all other inputs may be undefined). Reset# needs to be maintained for minimum  $t_{PW\_Reset}$ . CKE is pulled "low" before Reset# being de-asserted (min. time 10 ns).
2. Follow steps 2 to 10 in "Power-up Initialization Sequence".
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include  $V_{REF}$  training and Write leveling)

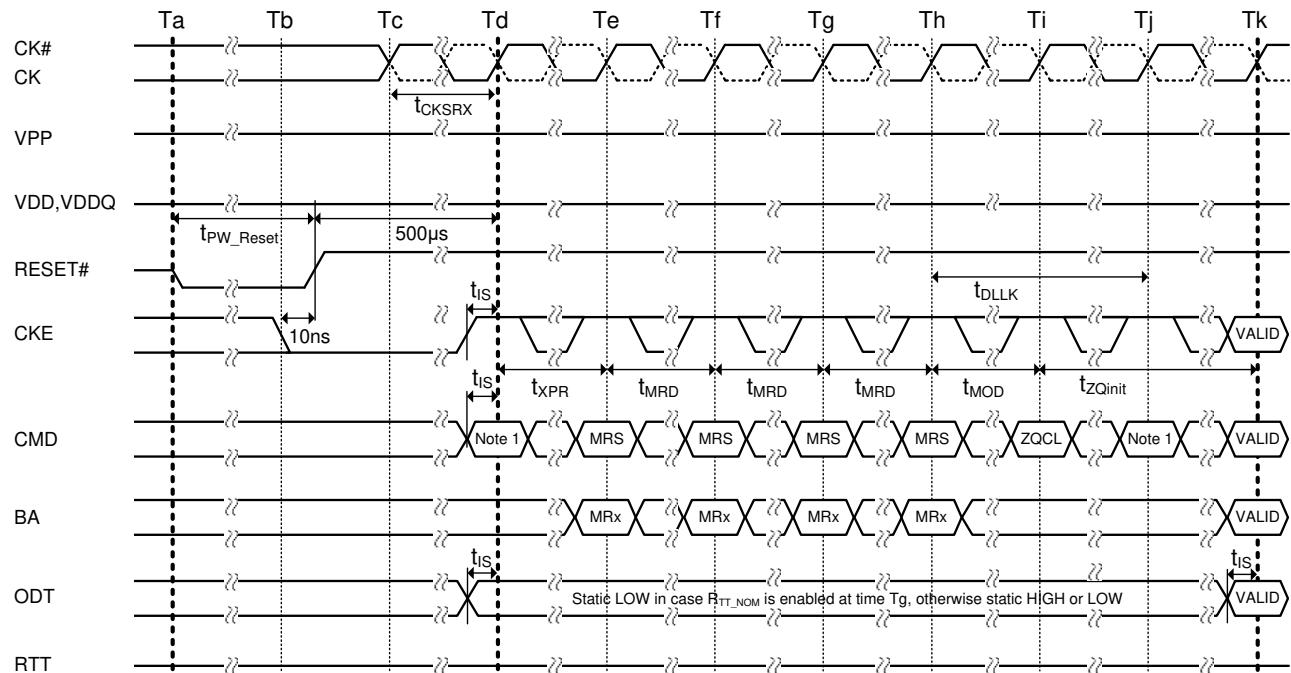


Figure 5. Beset Procedure at Power Stable

## Operation Mode Truth Table

Notes 1, 2, 3 and 4 apply to the entire Command Truth Table.

Note 5 Applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid].

**Table 5. Command Truth Table**

Function	Symbol	CKE <sub>n-1</sub>	CKE <sub>n</sub>	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	BG0	BA0-1	BC#/A12	A13, A11	A10/AP	A0-A9
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA				OP Code
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V
Self Refresh Entry <sup>7,9</sup>	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V
Self Refresh Exit <sup>7,10</sup>	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X
				L	H	H	H	H	V	V	V	V	V	V
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H	RFU	RFU	RFU	RFU	RFU	RFU
Bank Activate	ACT	H	H	L	L	RA	RA	RA	BG	BA	RA	RA	RA	RA
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	L	V	L	CA
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	H	V	L	CA
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	H	CA
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	L	V	H	CA
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	H	V	H	CA
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	L	V	L	CA
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	H	V	L	CA
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	H	CA
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	L	V	H	CA
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	H	V	H	CA
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X
Power Down Entry <sup>6</sup>	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X
Power Down Exit <sup>6</sup>	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	H	V
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	L	V

Note 1. All DDR4 SDRAM commands are defined by states of CS#, ACT#, RAS#/A16, CAS#/A15, WE#/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When ACT# = H; pins RAS#/A16, CAS#/A15, and WE#/A14 are used as command pins RAS#, CAS#, and WE# respectively. When ACT# = L; pins RAS#/A16, CAS#/A15, and WE#/A14 are used as address pins A16, A15, and A14 respectively.

Note 2. Reset# is low enable command which will be used only for asynchronous reset so must be maintained high during any function.

Note 3. Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

Note 4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

Note 5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

Note 6. The Power Down Mode does not perform any refresh operation.

Note 7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note 8. Controller guarantees self refresh exit to be synchronous.

Note 9. V<sub>PP</sub> and V<sub>REF</sub>(V<sub>REFCA</sub>) must be maintained during Self Refresh operation.

Note 10. The No Operation (NOP) command may be used only when entering gear-down mode.

Note 11. Refer to the CKE Truth Table for more detail with CKE transition.

**Table 6. CKE Truth Table**

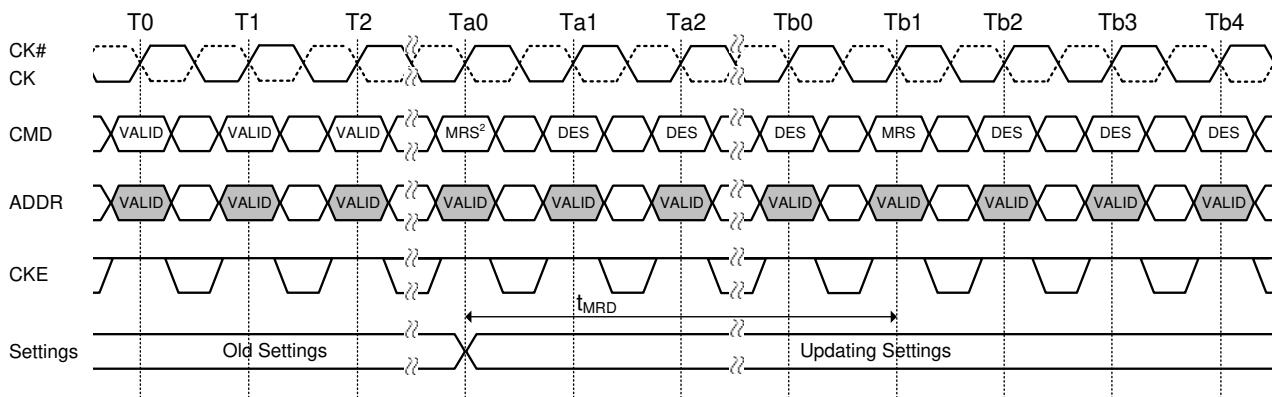
Current State <sup>(2)</sup>	CKEn-1 <sup>(1)</sup>	CKEn <sup>(1)</sup>	Command n <sup>(3)</sup> RAS#, CAS#, WE#, CS#	Action n <sup>(3)</sup>	Notes
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	Deselect	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	Deselect	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	Deselect	Active Power-Down Entry	11,13,14
Reading	H	L	Deselect	Power-Down Entry	11,13,14,17
Writing	H	L	Deselect	Power-Down Entry	11,13,14,17
Precharging	H	L	Deselect	Power-Down Entry	11,13,14,17
Refreshing	H	L	Deselect	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect	Precharge Power-Down Entry	11,13,14,18
	H	L	Refresh	Self-Refresh	9,13,18
See Command Truth Table for additional command details					10

**Notes:**

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and Action n is a result of command n, ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. During any CKE transition (registration of CKE H → L or CKE L → H) the CKE level must be maintained until 1nCK prior to t<sub>CKEmin</sub> being satisfied (at which time CKE may transition again).
7. Deselect and NOP are defined in the Command Truth Table.
8. On Self Refresh Exit Deselect commands must be issued on every clock edge occurring during the t<sub>XS</sub> period. Read or ODT commands may be issued only after t<sub>XSDLL</sub> is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are Deselect only.
12. Valid commands for Self Refresh Exit are Deselect only, except for Gear Down mode. NOP is allowed for the mode.
13. Self Refresh cannot be entered during Read or Write operations. For a detailed list of restrictions see section "Self-Refresh Operation" and see section "Power-Down Modes".
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around V<sub>REF</sub>) in Self Refresh and Power Down. It also applies to Address pins.
16. V<sub>PP</sub> and V<sub>REF</sub> (V<sub>REFCA</sub>) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered.
18. 'Idle state' is defined as all banks are closed (t<sub>RP</sub>, t<sub>DAL</sub>, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t<sub>MRD</sub>, t<sub>MOD</sub>, t<sub>RFC</sub>, t<sub>Qinit</sub>, t<sub>ZQoper</sub>, t<sub>ZQCS</sub>, etc.) as well as all Self Refresh exit and Power Down Exit parameters are satisfied (t<sub>XS</sub>, t<sub>XP</sub>, etc.).

## Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers ( $MR_n$ ) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time,  $t_{MRD}$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in the  $t_{MRD}$  timing figure.



NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. List of MRS commands exception that do not apply to  $t_{MRD}$

TIME BREAK  DON'T CARE

- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- $V_{REFDQ}$  training Value,  $V_{REFDQ}$  Training mode and  $V_{REFDQ}$  training Range.

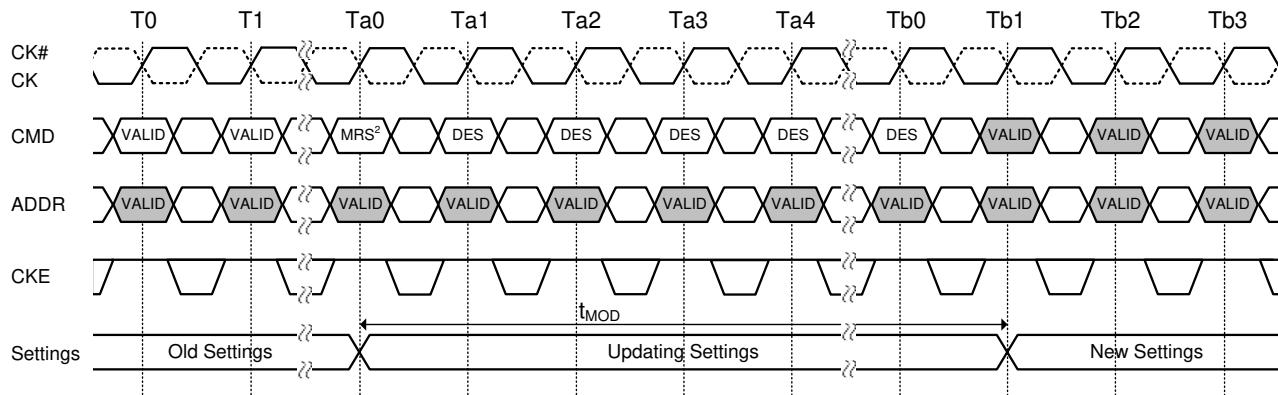
Figure 6.  $t_{MRD}$  timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands that do not apply  $t_{MRD}$  timing to next MRS command. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay,  $t_{MOD}$ , is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES, as shown in the  $t_{MOD}$  timing figure.

Some of the mode register setting cases, function updating takes longer than  $t_{MOD}$ . The MRS commands that do not apply  $t_{MOD}$  timing to next valid command excluding DES is listed in Note 2 of  $t_{MOD}$  timing figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



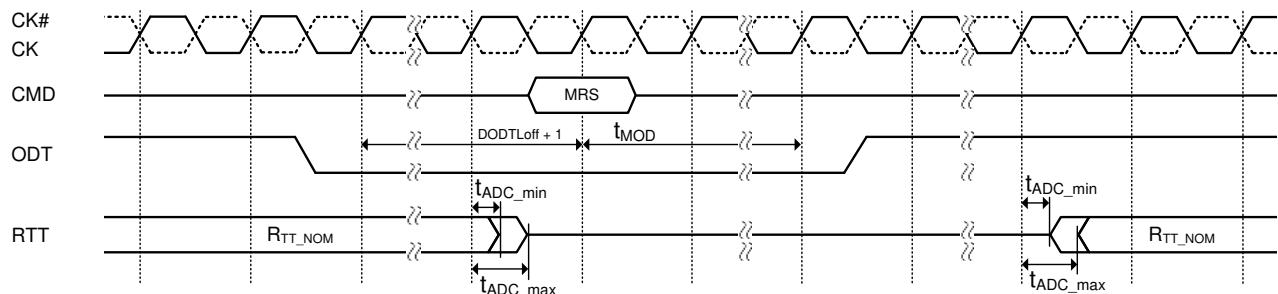
NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. TIME BREAK □ DON'T CARE

NOTE 2. List of MRS commands exception that do not apply to  $t_{MOD}$

- DLL Enable, DLL Reset
- $V_{REFDQ}$  training Value, internal  $V_{REF}$  Monitor,  $V_{REFDQ}$  Training mode and  $V_{REFDQ}$  training Range
- Gear down mode
- Per DRAM addressability mode
- CA Parity mode

Figure 7.  $t_{MOD}$  timing



NOTE 1. This timing diagram shows C/A Parity Latency mode is "Disable" case.

NOTE 2. When an MRS command mentioned in this note affects R<sub>TT\_NOM</sub> turn on timings, R<sub>TT\_NOM</sub> turn off timings and R<sub>TT\_NOM</sub> value, this means the MR register value changes. The ODT signal should set to be low for at least DODT<sub>loff</sub> + 1 clock before their affecting MRS command is issued and remain low until  $t_{MOD}$  expires. The following MR registers affects R<sub>TT\_NOM</sub> turn on timings, R<sub>TT\_NOM</sub> turn off timings and R<sub>TT\_NOM</sub> value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear down mode
- R<sub>TT\_NOM</sub>

Figure 8. ODT Status at MRS affecting ODT turn-on/off timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state, i.e., all banks are in the precharged state with  $t_{RP}$  satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If R<sub>TT\_NOM</sub> function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring R<sub>TT\_NOM</sub> is in an off state prior to MRS command affecting R<sub>TT\_NOM</sub> turn-on and off timing. The ODT signal may be registered high after  $t_{MOD}$  has expired. ODT signal is a don't care during MRS command if DRAM R<sub>TT\_NOM</sub> function is disabled in the mode register prior and after an MRS command.

## Mode Register MR0

Table 7. MR0 Definition

BG0	BA1	BA0	RAS#/A16	CAS#/A15	WE#/A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0				
0	0	0	0	0	0	0 <sup>1</sup>	0 <sup>1</sup>	WR & RTP <sup>2,3</sup>		DLL Rst	TM		CL		BT	CL	BL						
↓																							
A8	DLL Reset		A7	Test Mode		A3	Read Burst Type			A1	A0	BL											
0	No		0	Normal		0	Sequential			0	0	8 (Fixed)											
1	Yes					1	Interleave			0	1	BC4 or 8 (on the fly)											
1										1	0	BC4 (Fixed)											
1										1	1	Reserved											
↓																							
A11	A10	A9	WR	RTP		A6	A5	A4	A2	CAS Latency													
0	0	0	10	5 <sup>4</sup>		0	0	0	0	9 <sup>4</sup>													
0	0	1	12	6		0	0	0	1	10													
0	1	0	14	7 <sup>4</sup>		0	0	1	0	11 <sup>4</sup>													
0	1	1	16	8		0	0	1	1	12													
1	0	0	18	9 <sup>4</sup>		0	1	0	0	13 <sup>4</sup>													
1	0	1	20	10		0	1	0	1	14													
1	1	1	22	11 <sup>4</sup>		0	1	1	0	15 <sup>4</sup>													
1	1	0	24	12		0	1	1	1	16													
↓																							
Write Recovery and Read to Precharge for auto precharge																							

Note 1. Reserved for future use and must be programmed to 0 during MR.

Note 2. WR (write recovery for autoprecharge)min in clock cycles is calculated following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with  $t_{RP}$  to determine  $t_{DAL}$ .

Note 3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

Note 4. Not allowed when 1/4 rate gear-down mode is enabled.

## CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal read command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL):  $RL = AL + CL$ .

## Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

## DLL Reset

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL reset function has been issued. After the DLL is enabled, a subsequent DLL reset should be applied. Any time the DLL reset function is used,  $t_{DLLK}$  must be met before functions requiring the DLL can be used. (For example, Read commands or ODT synchronous operations).

## Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

**Table 8. Burst Type and Burst Order**

Burst Length	Read/Write	Starting Column Address			Burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	Note
		A2	A1	A0			
4 Chop	Read	0	0	0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	1, 2, 3
		0	0	1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	
		0	1	0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	
		0	1	1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	
		1	0	0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	
		1	0	1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	
		1	1	0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	
		1	1	1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	
	Write	0	V	V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 2, 4, 5
		1	V	V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	
8	Read	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2
		0	0	1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	Write	V	V	V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	2, 4

**Notes:**

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for  $t_{WR}$  and  $t_{WTR}$  will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for  $t_{WR}$  and  $t_{WTR}$  will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

## Write Recovery (WR)/Read-to-Precharge (RTP)

The programmed write recovery (WR) value is used for the auto precharge feature along with  $t_{RP}$  to determine  $t_{DAL}$ . WR for auto precharge (MIN) in clock cycles is calculated by dividing  $t_{WR}$  (in ns) by  $t_{CK}$  (in ns) and rounding to the next integer:

The WR value must be programmed to be equal to or larger than  $t_{WR}$  (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array;  $t_{WR}$  values will change when enabled. If there is a CRC error, the device blocks the Write operation and discards the data.

Internal Read-to-Precharge (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing  $t_{RTP}$  (in ns) by  $t_{CK}$  (in ns) and rounding to the next integer:

The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with  $t_{RP}$  to determine the ACT timing to the same bank.

## Mode Register MR1

**Table 9. MR1 Definition**

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. Outputs disabled - DQs, DQSs, DQS#s.

Note 3. States reversed to “0 as Disable” with respect to DDR4.

Note 3. States reversed to "0 as Disable" with respect to Note 4. Additive Latency is not supported for x16 device.

Note 5. Not allowed when 1/4 rate gear-down mode is enabled.

## DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the Self Refresh operation and is automatically re-enabled upon exit of the Self Refresh operation. Any time the DLL is enabled and subsequently reset,  $t_{DLLK}$  clock cycles must occur before a Read or Synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the  $t_{DQSCK}$ ,  $t_{AON}$ , or  $t_{AOE}$  parameters.

During  $t_{DLLK}$ , CKE must continuously be registered High. The device does not require DLL for any Write operation, except when  $R_{TT\ WR}$  is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin Low and/or by programming the  $R_{TT\_NOM}$  bits  $MR1[10:8] = 000$  via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set  $R_{TT\_WD}\cdot MR2[11:9] = 00$ .

## Output Driver Impedance Control

The output driver impedance of the device is selected by MB1[2:1]

## ODT $R_{TT\_NOM}$ Values

The device is capable of providing three different termination values:  $R_{TT\_PARK}$ ,  $R_{TT\_NOM}$ , and  $R_{TT\_WR}$ . The nominal termination value,  $R_{TT\_NOM}$ , is programmed in MR1. A separate value,  $R_{TT\_WR}$ , may be programmed in MR2 to enable a unique  $R_{TT}$  value when ODT is enabled during Write operations. The  $R_{TT\_WR}$  value can be applied during Write commands even when  $R_{TT\_NOM}$  is disabled. A third  $R_{TT}$  value,  $R_{TT\_PARK}$ , is programmed in MR5.  $R_{TT\_PARK}$  provides a termination value when the ODT signal is Low.

## Additive Latency

The Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in the device. In this operation, the device allows a Read or Write command (either with or without auto precharge) to be issued immediately after the Activate command. The command is held for the time of AL before it is issued inside the device. Read latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. Write latency (WL) is controlled by the sum of the AL and CAS Write latency (CWL) register settings. Additive Latency is not supported for x16 device.

## Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

## Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

## Mode Register MR2

Table 10. MR2 Definition

BG0	BA1	BA0	RAS#/A16	CAS#/A15	WE#/A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0																
0	1	0	0	0	0	0 <sup>1</sup>	Write CRC	R <sub>TT_WR</sub>			0 <sup>1</sup>	LPASR	CWL			0 <sup>1</sup>	0 <sup>1</sup>	0 <sup>1</sup>																	
↓																																			
A12	Write CRC		A11	A10	A9	R <sub>TT_WR</sub>																													
0	Disable		0	0	0	R <sub>TT(WR)</sub> disabled (Write does not affect R <sub>TT</sub> value)																													
1	Enable		0	0	1	RZQ/2																													
0	1	0	0	0	1	RZQ/1																													
0	1	1	0	0	1	Hi-Z																													
1	0	0	0	0	0	RZQ/3																													
↓																																			
A5	A4	A3	CWL	Operating Data Rate in MT/s for 1 t <sub>Clock</sub> Write Preamble				Operating Data Rate in MT/s for 2 t <sub>Clock</sub> Write Preamble <sup>2</sup>																											
				1 <sup>st</sup> Set		2 <sup>nd</sup> Set		1 <sup>st</sup> Set		2 <sup>nd</sup> Set																									
				0	0	0	9	1600 <sup>3</sup>		-		-				-																			
				0	0	1	10	1866		-		-				-																			
				0	1	0	11	2133		1600 <sup>3</sup>		-				-																			
				0	1	1	12	2400		1866		-				-																			
				1	0	0	14	2666		2133		2400				2400																			
				1	0	1	16	2933 / 3200		2400		2666				2933 / 3200																			
1	1	0	18	-		2666		2933 / 3200		-																									
1	1	1	20	-		2933 / 3200		-		2933 / 3200																									
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## Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT ( $R_{TT\_WR}$ ) settings in MR2[11:9]. In write leveling mode, only  $R_{TT\_NOM}$  is available.

## Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

## Mode Register MR3

**Table 11. MR3 Definition**

The diagram illustrates the bit assignments for various memory control parameters, organized into several tables:

- MPR Read Format:** A12 (MSB) and A11 (LSB) define the MPR Read Format. The combinations are:
  - 00: Serial
  - 01: Parallel
  - 10: Staggered
  - 11: Reserved
- CRC+DM Write Command Latency:** A10 (MSB) and A9 (LSB) define the CRC+DM Write Command Latency. The combinations are:
  - 00: 4 t<sub>CK</sub> (1600)
  - 01: 5 t<sub>CK</sub> (1866/2133/2400/2666)
  - 10: 6 t<sub>CK</sub> (2933/3200)
  - 11: RFU
- Geardown Mode:** A3 (MSB) defines the Geardown Mode. The combinations are:
  - 0: 1/2 Rate
  - 1: 1/4 Rate
- MPR Operation:** A2 (MSB) defines the MPR Operation. The combinations are:
  - 0: Normal
  - 1: Data flow from/to MPR
- Temperature sensor:** A5 (MSB) defines the Temperature sensor. The combinations are:
  - 0: Disable
  - 1: Enable

Arrows indicate the flow of control from the top row to the sub-tables, and from the sub-tables to the bottom row.

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. Write Command latency when CRC and DM are both enabled:

- At less than or equal to 1600 then  $4t_{CK}$ ; neither  $5t_{CK}$  nor  $6t_{CK}$
- At greater than 1600 and less than or equal to 2666 then  $5t_{CK}$ ; neither  $4t_{CK}$  nor  $6t_{CK}$
- At greater than 2666 and less than or equal to 3200 then  $6t_{CK}$ ; neither  $4t_{CK}$  nor  $5t_{CK}$

Note 3. Refer to MPR Data Format table.

## Write Command Latency When CRC/DM is Enabled

The Write command latency (WCL) must be set when both Write CRC and DM are enabled for Write CRC persistent mode. This provides the extra time required when completing a Write burst when Write CRC and DM are enabled.

## Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening  $t_{RFC}$  and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

## Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

## Per-DRAM Addressability

The MRS command mask allows programmability of a given device that may be in the same rank (devices sharing the same command and address signals). As an example, this feature can be used to program different ODT or  $V_{REF}$  values on DRAM devices within a given rank.

## Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS#, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode no MRS command or sync pulse is required.

## Mode Register MR4

**Table 12. MR4 Definition**

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. Not allowed when 1/4 rate gear-down mode is enabled.

Note 3. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

## Write Preamble

Programmable Write preamble,  $t_{WPRE}$ , can be set to  $1t_{CK}$  or  $2t_{CK}$  via the MR4 register. The  $1t_{CK}$  setting is similar to DDR3. However, when operating in  $2t_{CK}$  Write preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable  $t_{CK}$  range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

## Read Preamble

Programmable Read preamble  $t_{RPRE}$  can be set to  $1t_{CK}$  or  $2t_{CK}$  via the MR4 register. Both the  $1t_{CK}$  and  $2t_{CK}$  DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 Read preamble settings may require the memory controller to train (or read level) its data strobe receivers using the Read preamble training.

## Read Preamble Training

Programmable Read preamble training can be set to  $1t_{CK}$  or  $2t_{CK}$ . This mode can be used by the memory controller to train or Read level its data strobe receivers.

## Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than  $t_{REFI}$  of the normal temperature range by skipping external Refresh commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

## Command Address Latency

Command Address Latency (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles ( $t_{CAL}$ ) between a CS# registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of  $[t_{CK}(ns)/t_{CAL}(ns)]$ .

## Internal VREF Monitor

The device generates its own internal  $V_{REFDQ}$ . This mode may be enabled during  $V_{REFDQ}$  training, and when enabled,  $V_{REF, \text{time-short}}$  and  $V_{REF, \text{time-long}}$  need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

## Mode Register MR5

**Table 13. MR5 Definition**

Note 1. Reserved for future use and must be programmed to 0 during MRS.

Note 2. When  $R_{TT\_NOM}$  Disable is set in MR1, A5 of MR5 will be ignored.

Note 3. Not allowed when 1/4 rate gear-down mode is enabled.

## Data Bus Inversion

The Data Bus Inversion (DBI) function has been added to the device and is supported for x16 configurations. The DBI function shares a common pin with the DM functions. The DBI function applies to both Read and Write operations; Write DBI cannot be enabled at the same time the DM function is enabled. DBI is not allowed during MPR Read operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

## Data Mask

The Data Mask (DM) function, also described as a partial write, has been added to the device and is supported for x16 configurations. The DM function shares a common pin with the DBI functions. The DM function applies only to Write operations and cannot be enabled at the same time the write DBI function is enabled.

## CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

## ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide  $R_{TT\_NOM}$  termination. However, the device may provide  $R_{TT\_PARK}$  termination depending on the MR settings. This is primarily for additional power savings.

## CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

## CRC Error Clear

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

## CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on  $t_{CK}$ , is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT#, RAS#/A16, CAS#/A15, WE#/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS# are not included in the parity calculation.

## Mode Register MR6

Table 14. MR6 Definition

BG0	BA1	BA0	RAS#/A16	CAS#/A15	WE#/A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	0	0 <sup>1</sup>	Data rate			0 <sup>1</sup>	0 <sup>1</sup>	V <sub>REFDQ</sub> Training	V <sub>REFDQ</sub> Range	V <sub>REFDQ</sub> Training Value					

A12	A11	A10	Data rate		
0	0	0	Data rate $\leq$ 1333Mbps		
0	0	1	1333Mbps $<$ Data rate $\leq$ 1866Mbps (1600, 1866Mbps)		
0	1	0	1866Mbps $<$ Data rate $\leq$ 2400Mbps (2133, 2400Mbps)		
0	1	1	2400Mbps $<$ Data rate $\leq$ 2666Mbps (2666Mbps)		
1	0	0	2666Mbps $<$ Data rate $\leq$ 3200Mbps (2933, 3200Mbps)		
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Reserved		

A6	V <sub>REFDQ</sub> Range
0	Range 1
1	Range 2

A7	V <sub>REFD</sub> Training
0	Disable
1	Enable

A5:A0	Range1	Range2	A5:A0	Range1	Range2	A5:A0	Range1	Range2	A5:A0	Range1	Range2
000000	60.00%	45.00%	001101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
000001	60.65%	45.65%	001110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
000010	61.30%	46.30%	001111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
000011	61.95%	46.95%	010000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
000100	62.60%	47.60%	010001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
000101	63.25%	48.25%	010010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
000110	63.90%	48.90%	010011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
000111	64.55%	49.55%	010100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
001000	65.20%	50.20%	010101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
001001	65.85%	50.85%	010110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
001010	66.50%	51.50%	010111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
001011	67.15%	52.15%	011000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
001100	67.80%	52.80%	011001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111 : Reserved		

Note 1. Reserved for future use and must be programmed to 0 during MRS.

## Data Rate Enable

The device controller must program the correct data rate according to the operating frequency.

## V<sub>REFDQ</sub> Training Enable

V<sub>REFDQ</sub> Training is where the device internally generates its own V<sub>REFDQ</sub> to be used by the DQ input receivers. The device controller is responsible for setting and calibrating the internal V<sub>REFDQ</sub> level using an MRS protocol (adjust up, adjust down, etc.). The procedure is a series of Writes and Reads in conjunction with V<sub>REFDQ</sub> adjustments to optimize and verify the data eye. Enabling V<sub>REFDQ</sub> Training must be used whenever values are being written to the MR6[6:0] register.

## V<sub>REFDQ</sub> Training Range

The device defines two V<sub>REFDQ</sub> calibration ranges: Range 1 and Range 2. Range 1 supports V<sub>REFDQ</sub> between 60% and 92% of V<sub>DDQ</sub> while Range 2 supports V<sub>REFDQ</sub> between 45% and 77% of V<sub>DDQ</sub>. Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

## V<sub>REFDQ</sub> Training Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V<sub>REFDQ</sub>.

## **Mode Register MR7: Ignore**

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

## DLL-off Mode and DLL on/off Switching Procedure

### DLL on/off switching procedure

The DLL-off mode is entered by setting MR1 bit A0 to "0"; this will disable the DLL for subsequent operations until A0 bit is set back to "1".

### DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors,  $R_{TT\_NOM}$ , must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "0" to disable the DLL.
3. Wait  $t_{MOD}$ .
4. Enter Self Refresh Mode; wait until ( $t_{CKSRE}$ ) is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least ( $t_{CKSRX}$ ) at device inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered high until all  $t_{MOD}$  timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all  $t_{MOD}$  timings from any MRS command are satisfied. If  $R_{TT\_NOM}$  features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't Care.
8. Wait  $t_{XS\_Fast}$  or  $t_{XS\_Abort}$  or  $t_{XS}$ , then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary; a ZQCL command may also be issued after  $t_{XS\_Fast}$ ).
  - $t_{XS\_Fast}$  : ZQCL, ZQCS, MRS commands. For MRS command, only CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided the device is not in per DRAM addressability mode. Access to other device mode registers must satisfy  $t_{XS}$  timing.
  - $t_{XS\_Abort}$  : If the MR4 bit A9 is enabled then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of  $t_{XS\_Abort}$ . Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
  - $t_{XS}$  : ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
9. Wait for  $t_{MOD}$ , then device is ready for next command.

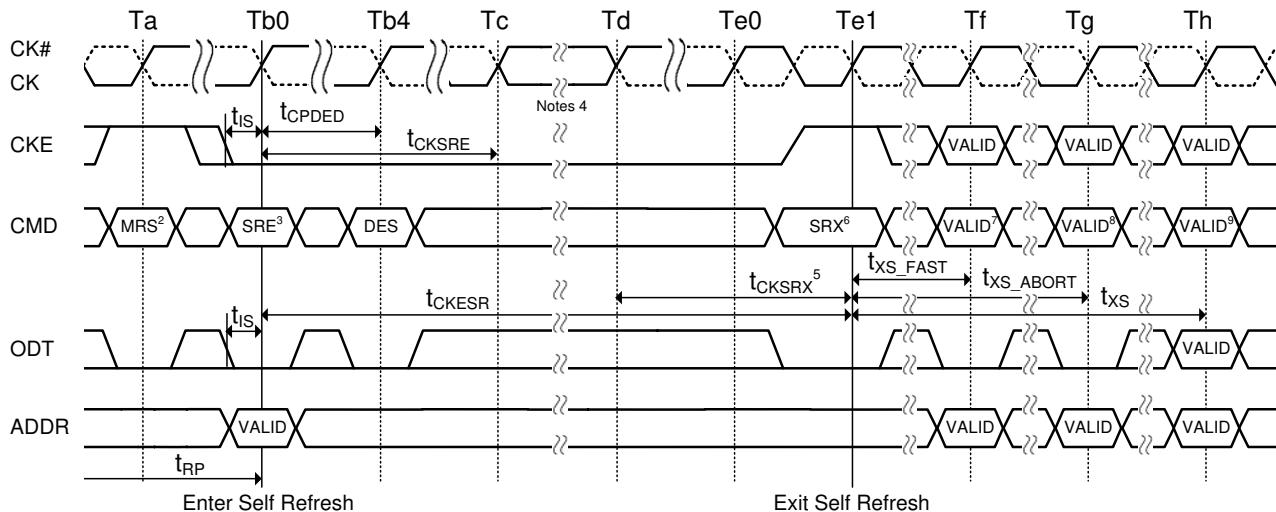


Figure 9. DLL Switch Sequence from DLL ON to DLL OFF

## DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

- Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors ( $R_{TT\_NOM}$ ) must be in high impedance state before Self-Refresh mode is entered.)
- Enter Self Refresh Mode, wait until  $t_{CKSRE}$  satisfied.
- Change frequency, following the guidelines in the Input Clock Frequency Change section.
- Wait until a stable clock is available for at least ( $t_{CKSRX}$ ) at device inputs.
- Starting with the Self Refresh Exit command, CKE must continuously be registered high until  $t_{DLLK}$  timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered low until  $t_{DLLK}$  timings from subsequent DLL Reset command is satisfied. If  $R_{TT\_NOM}$  were disabled in the mode registers when Self Refresh mode was entered, ODT signal is don't care.
- Wait  $t_{XS}$  or  $t_{XS\_ABORT}$  depending on Bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.
- Wait  $t_{MRD}$ , then set MR0 bit A8 to “1” to start DLL Reset.
- Wait  $t_{MRD}$ , then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After  $t_{MOD}$  satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after  $t_{DLLK}$ .)
- Wait for  $t_{MOD}$ , then device is ready for next command. (Remember to wait  $t_{DLLK}$  after DLL Reset before applying command requiring a locked DLL). In addition, wait also for  $t_{ZQoper}$  in case a ZQCL command was issued.

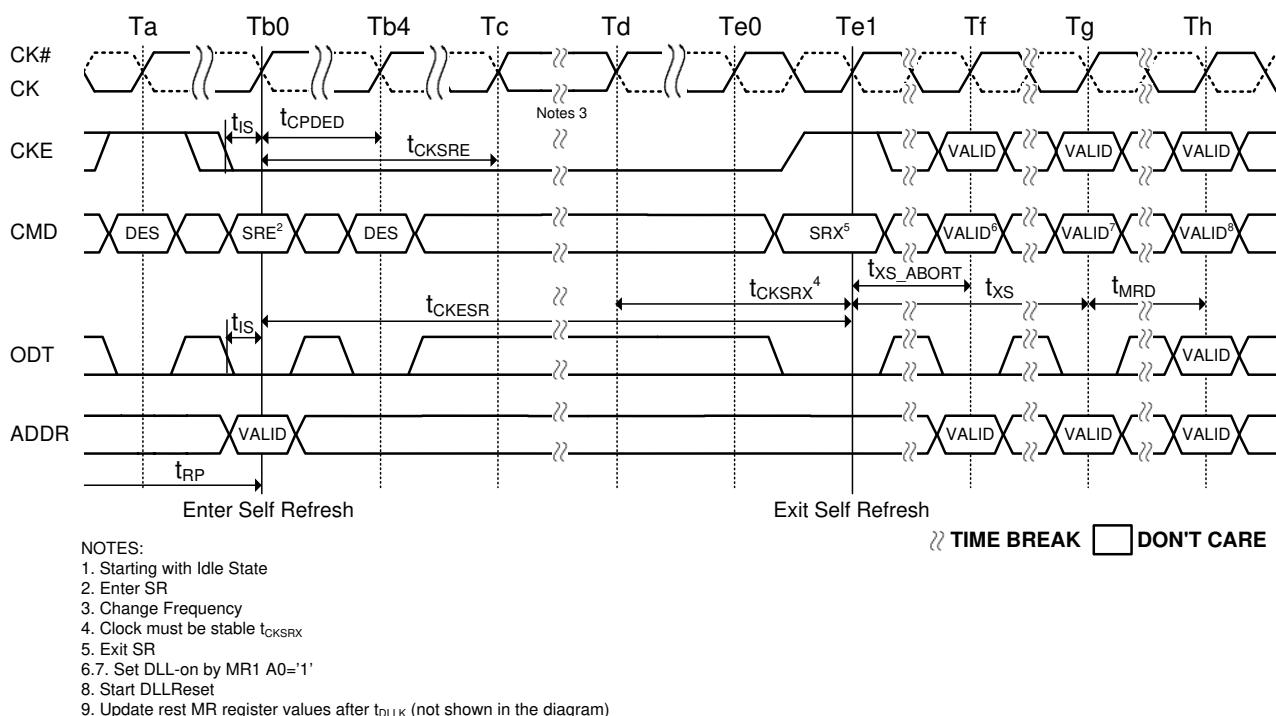


Figure 10. DLL Switch Sequence from DLL OFF to DLL ON

## DLL-off Mode

DLL-off mode is entered by setting MR1 bit A0 to "0"; this will disable the DLL for subsequent operations until A0 bit is set back to "1". The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off Mode is specified by the parameter  $t_{CKDLL\_OFF}$ . There is no minimum frequency limit besides the need to satisfy the refresh interval,  $t_{REFI}$ .

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9.

DLL-off mode will affect the Read data Clock to Data Strobe relationship ( $t_{DQSCK}$ ), but not the Data Strobe to Data relationship ( $t_{DQSQ}$ ,  $t_{QH}$ ). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where  $t_{DQSCK}$  starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode  $t_{DQSCK}$  starts (AL+CL - 1) cycles after the read command. Another difference is that  $t_{DQSCK}$  may not be small compared to  $t_{CK}$  (it might even be larger than  $t_{CK}$ ) and the difference between  $t_{DQSCKmin}$  and  $t_{DQSCKmax}$  is significantly larger than in DLL-on mode.  $t_{DQSCK(DLL\_off)}$  values are undefined.

The timing relations on DLL-off mode Read operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.

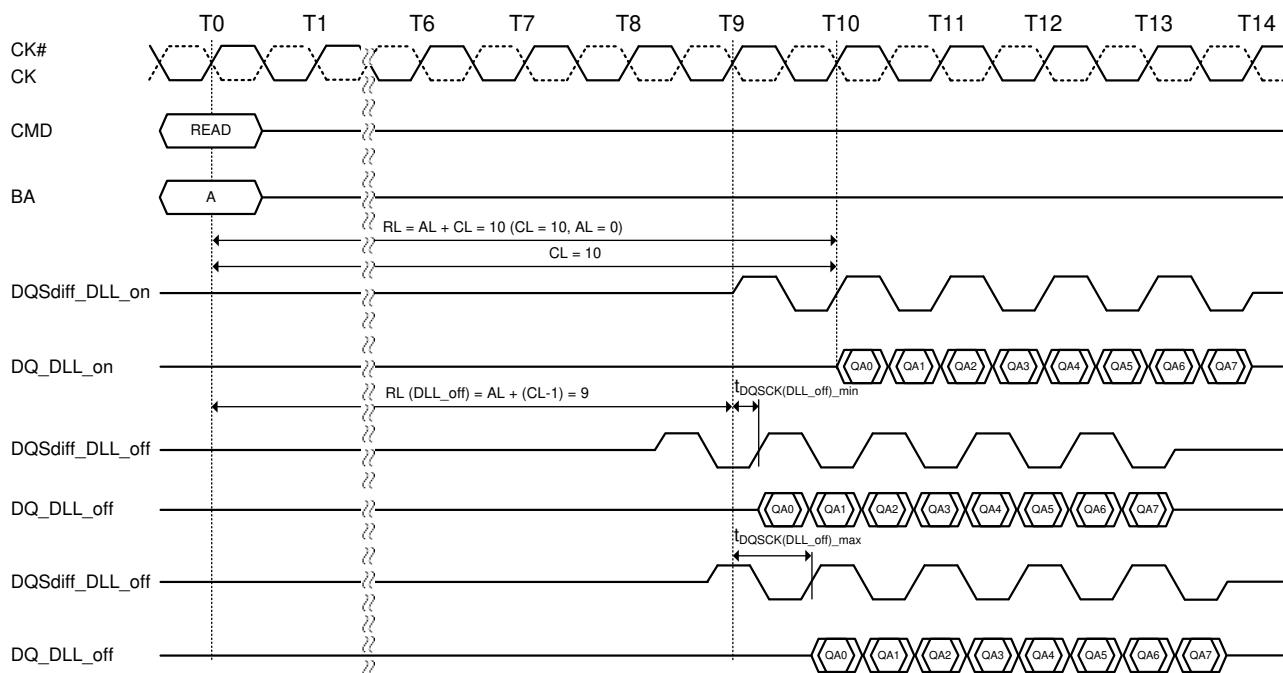


Figure 11. Read operation at DLL-off mode

## Input Clock Frequency Change

After the device is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that after the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in Self- Refresh mode. Outside Self-Refresh mode, it is illegal to change the clock frequency.

After the device has been successfully placed into Self-Refresh mode and  $t_{CKSRE}$  has been satisfied, the state of the clock becomes a "Don't Care". Following a "Don't Care", changing the clock frequency is permissible, provided the new clock frequency is stable prior to  $t_{CKSRX}$ . When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Self-Refresh Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and  $t_{CCD\_L}/t_{DLLK}$  value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, i.e. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2666 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 5. The correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2666, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 5 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the idle state, unless the DRAM is reset. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the idle state.

If MR6 is issued prior to Self Refresh Entry for new  $t_{DLLK}$  value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.

The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence. (See DLL on/off switching procedure)

## Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain  $t_{DQSS}$ ,  $t_{DSS}$ , and  $t_{DSH}$  specification. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the  $t_{DQSS}$ ,  $t_{DSS}$  and  $t_{DSH}$  specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS, DQS# to CK, CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS, DQS# to align the rising edge of DQS, DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, CK#, sampled with the rising edge of DQS, DQS#, through the DQ bus. The controller repeatedly delays DQS, DQS# until a transition from 0 to 1 is detected. The DQS, DQS# delay established through this exercise would ensure  $t_{DQSS}$  specification.

Besides  $t_{DQSS}$ ,  $t_{DSS}$  and  $t_{DSH}$  specification also needs to be fulfilled. One way to achieve this is to combine the actual  $t_{DQSS}$  in the application with an appropriate duty cycle and jitter on the DQS, DQS# signals. Depending on the actual  $t_{DQSS}$  in the application, the actual values for  $t_{DQSL}$  and  $t_{DQSH}$  may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy  $t_{DSS}$  and  $t_{DSH}$  specification. A conceptual timing of this scheme is shown below.

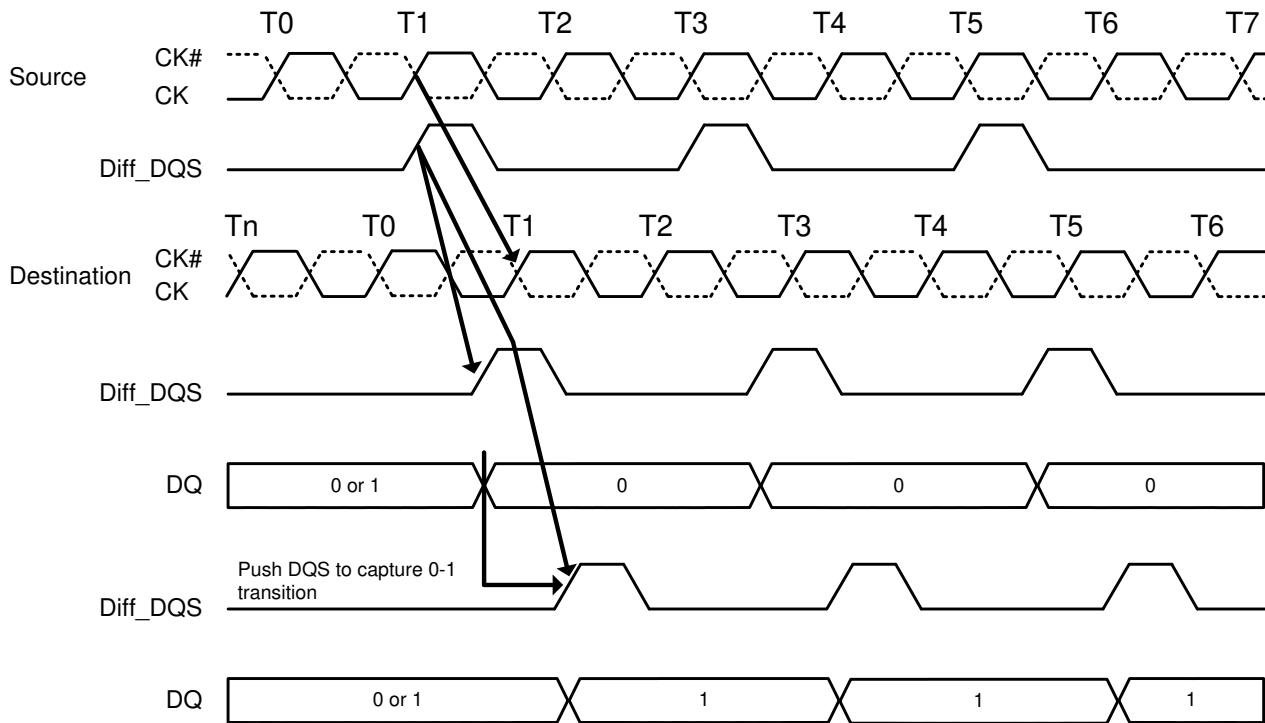


Figure 12. Write Leveling Concept

DQS, DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff\_DQS(diff\_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff\_DQS(diff\_LDQS) to clock relationship.

## **DRAM setting for write leveling & DRAM termination function in that mode**

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (see the MR setting involved in the leveling procedure table). Note that in write leveling mode, only DQS terminations are activated and deactivated via ODT pin, unlike normal operation (see the DRAM termination function in the leveling mode table).

**Table 15. MR setting involved in the leveling procedure**

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

**Table 16. DRAM termination function in the leveling mode**

ODT pin @DRAM if $R_{TT\_NOM}/R_{TT\_PARK}$ Value is set via MRS	DQS/DQS# termination	DQs termination
$R_{TT\_NOM}$ with ODT High	on	off
$R_{TT\_PARK}$ with ODT Low	on	off

Notes:

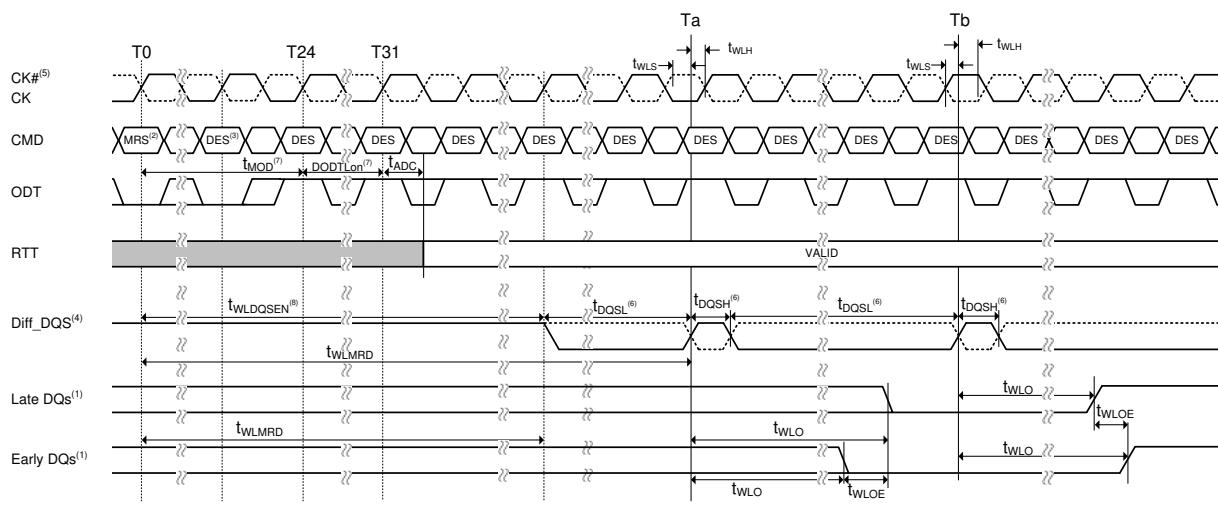
1. In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all  $R_{TT\_NOM}$  and  $R_{TT\_PARK}$  settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) all  $R_{TT\_NOM}$  and  $R_{TT\_PARK}$  settings are allowed.
2. Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A[11:9] must be '000' prior to entering Write Leveling Mode.

## Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only Deselect commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change the other MR1 bits. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after  $t_{MOD}$ , at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of  $t_{WLQSEN}$ , at which time the DRAM has applied on-die termination on these signals. After  $t_{DQSL}$  and  $t_{WLMD}$ , the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller.  $t_{WLMD(max)}$  timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after  $t_{WLO}$  timing. There is a DQ output uncertainty of  $t_{WLOE}$  defined to allow mismatch on DQ bits. The  $t_{WLOE}$  period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS - DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall Write Leveling procedure.



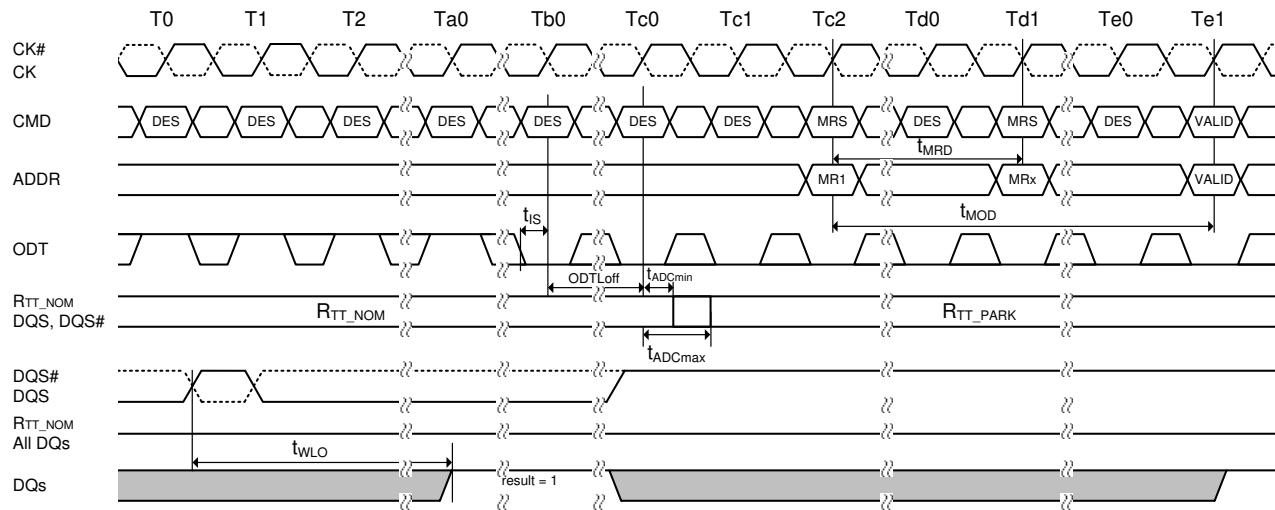
NOTE 1. DDR4 SDRAM drives leveling feedback on all DQs.  
 NOTE 2. MRS: Load MR1 to enter write leveling mode.  
 NOTE 3. DES: Deselect.  
 NOTE 4. diff\_DQS is the differential data strobe (DQS-DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.  
 NOTE 5. CK/CK#: CK is shown with solid dark line, where as CK# is drawn with dotted line.  
 NOTE 6. DQS, DQS# needs to fulfill minimum pulse width requirements  $t_{DQSH(min)}$  and  $t_{DQSL(min)}$  as defined for regular Writes; the max pulse width is system dependent.  
 NOTE 7.  $t_{MOD(min)} = \max(24nCK, 15ns)$ , WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL - 2 = 7.  
 NOTE 8.  $t_{WLQSEN}$  must be satisfied following equation when using ODT.  
 $t_{WLQSEN} > t_{MOD(min)} + ODTlon + t_{ADC}$ : at DLL = Enable  
 $t_{WLQSEN} > t_{MOD(min)} + t_{AONAS}$ : at DLL = Disable

Figure 13. Write Leveling Sequence (DQS capturing CK low at Ta and CK high at Tb)

## Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see  $\sim T0$ ), stop driving the strobe signals (see  $\sim Tc0$ ). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until  $t_{MOD}$  after the respective MRS command ( $Te1$ ).
2. Drive ODT pin low ( $t_{IS}$  must be satisfied) and continue registering low (see  $Tb0$ ).
3. After the  $R_{TT}$  is switched off, disable Write Level Mode via MRS command (see  $Tc2$ ).
4. After  $t_{MOD}$  is satisfied ( $Te1$ ), any valid command may be registered. (MRS commands may be issued after  $t_{MRD}$  ( $Td1$ ).



**Figure 14. Write Leveling Exit**

## CAL Mode (CS# to Command Address Latency)

DDR4 supports Command Address Latency (CAL) function as a power savings feature. CAL is the delay in clock cycles between CS# and CMD/ADDR defined by MR4[A8:A6].

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

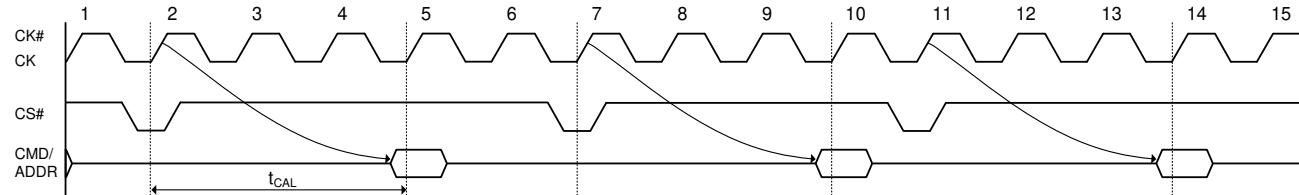


Figure 15. Definition of CAL

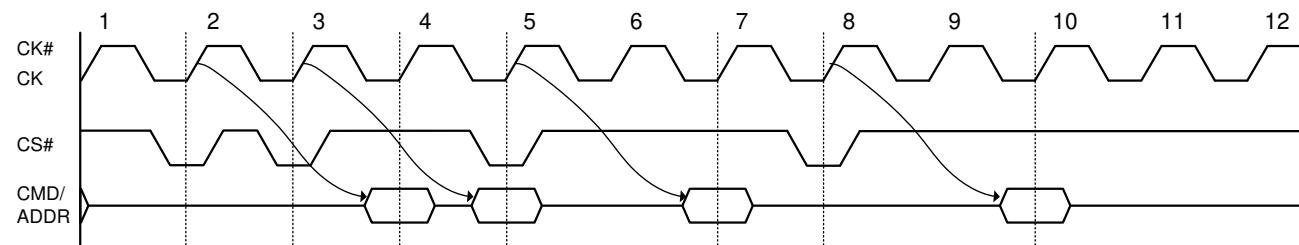
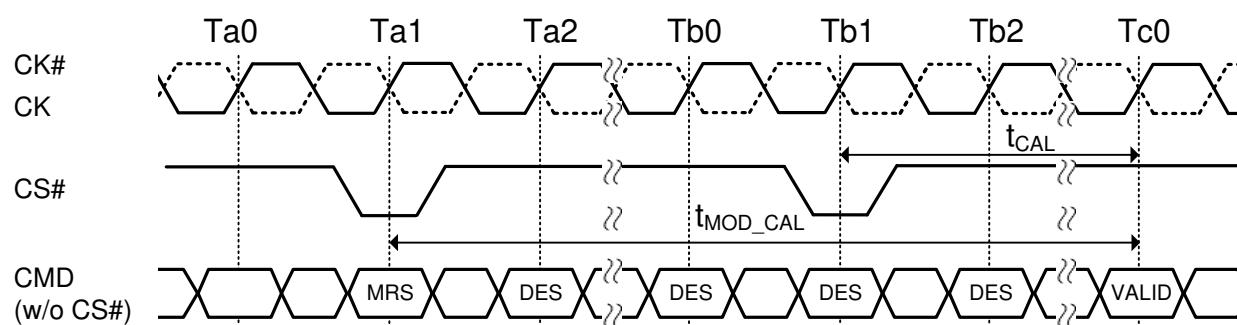


Figure 16. CAL operational timing for consecutive command issues

## MRS Timings with Command/Address Latency enabled

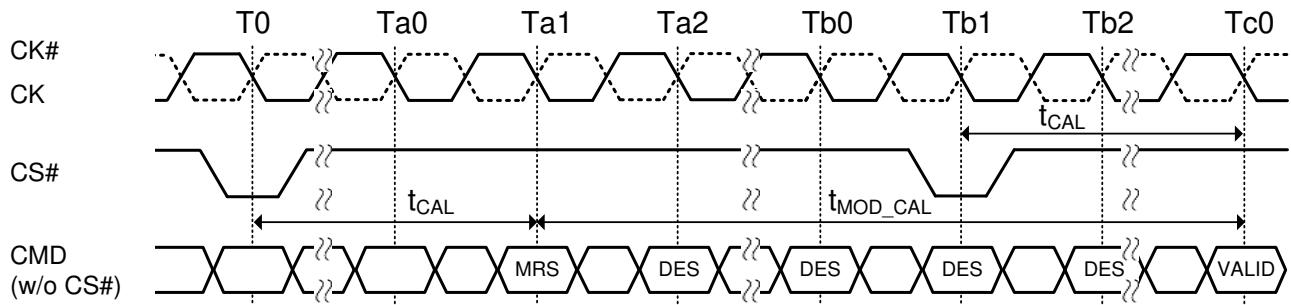
When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is  $t_{MOD\_CAL}$ , where  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$ .



NOTE1: MRS command at Ta1 enables CAL mode.

NOTE2:  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$ .

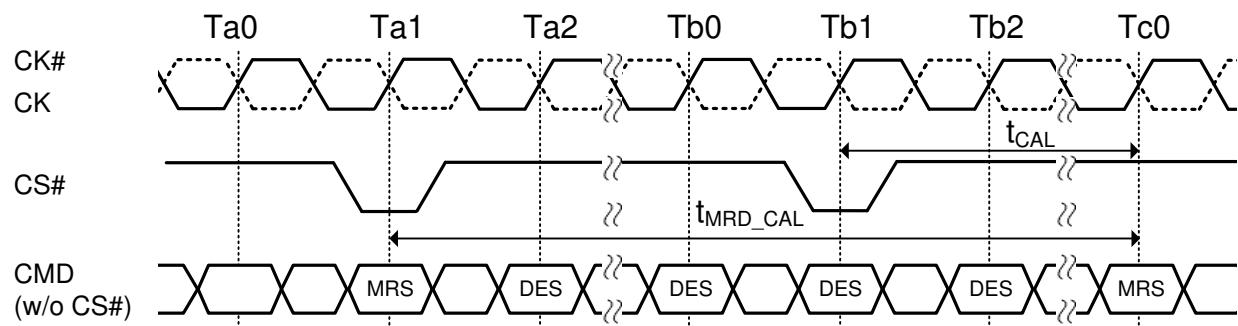
Figure 17. CAL enable timing -  $t_{MOD\_CAL}$



NOTE1: MRS at Ta1 may or may not modify CAL,  $t_{MOD\_CAL}$  is computed based on new  $t_{CAL}$  setting.

NOTE2:  $t_{MOD\_CAL} = t_{MOD} + t_{CAL}$

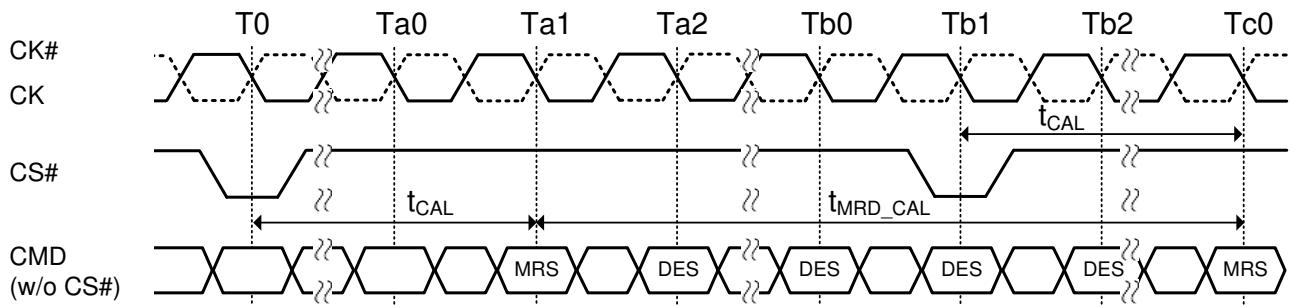
Figure 18.  $t_{MOD\_CAL}$ , MRS to valid command timing with CAL enabled



NOTE1: MRS command at Ta1 enables CAL mode.

NOTE2:  $t_{MRD\_CAL} = t_{MOD} + t_{CAL}$

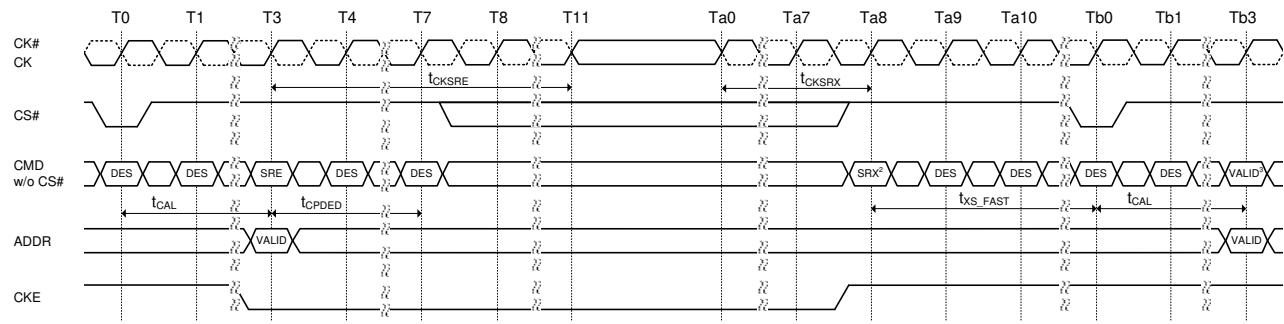
Figure 19. CAL enabling MRS to next MRS command,  $t_{MRD\_CAL}$



NOTE1: MRS at Ta1 may or may not modify CAL,  $t_{MRD\_CAL}$  is computed based on new  $t_{CAL}$  setting.

NOTE2:  $t_{MRD\_CAL} = t_{MOD} + t_{CAL}$

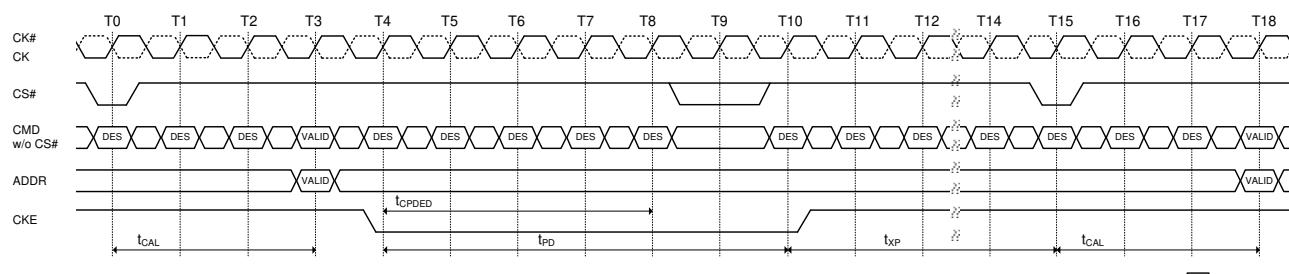
Figure 20.  $t_{MRD\_CAL}$ , mode register cycle time with CAL enabled



NOTES:  
1.  $t_{CAL} = 3nCK$ ,  $t_{CPDDED} = 4nCK$ ,  $t_{CKSRE} = 8nCK$ ,  $t_{CKSPX} = 8nCK$ ,  $t_{XS\_FAST} = t_{RFC4(min)} + 10ns$   
2. CS# = H, ACT# = Don't Care, RAS#/A16 = Don't Care, CAS#/A15 = Don't Care, WE#/A14 = Don't Care  
3. Only MRS (limited to those described in the Self-Refresh Operation section). ZOCS or ZOCL command allowed.

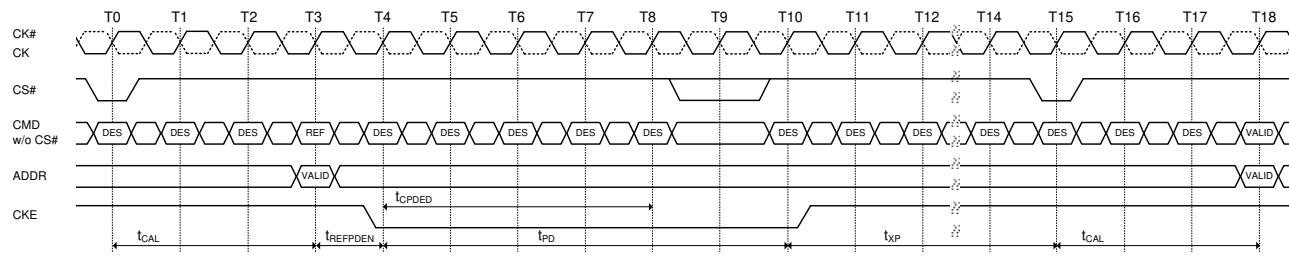
TIME BREAK □ DON'T CARE

Figure 21. Self Refresh Entry/Exit Timing with CAL



NOTE 1.  $t_{CAL} = 3nCK$ ,  $t_{CPDDED} = 4nCK$ ,  $t_{PD} = 6nCK$ ,  $t_{XP} = 5nCK$

Figure 22. Active Power Down Entry and Exit Timing with CAL



NOTE 1.  $t_{CAL} = 3nCK$ ,  $t_{REFPDEN} = 1nCK$ ,  $t_{CPDDED} = 4nCK$ ,  $t_{PD} = 6nCK$ ,  $t_{XP} = 5nCK$

Figure 23. Refresh Command to Power Down Entry with CAL

## Fine Granularity Refresh Mode

DDR4 supports Command Address Latency (CAL) function as a power savings feature. CAL is the delay in clock cycles between CS# and CMD/ADDR defined by MR4[A8:A6].

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

### Mode Register and Command Truth Table

The Refresh cycle time ( $t_{RFC}$ ) and the average Refresh interval ( $t_{REFI}$ ) can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the device (on-the-fly mode). The on-the-fly (OTF) mode must be enabled by MRS before any on-the-fly Refresh command can be issued.

**Table 17. MR3 definition for Fine Granularity Refresh Mode**

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal Mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected ('A8=1'), the device evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation.

**Table 18. Refresh command truth table**

Function	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	BG0	BA0-1	A10/AP	A[9:0], A[13:11]	MR3 [8:6]
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	0VV
Refresh (on-the-fly 1x)	L	H	L	L	H	L	V	V	V	1VV
Refresh (on-the-fly 2x)	L	H	L	L	H	H	V	V	V	101
Refresh (on-the-fly 4x)	L	H	L	L	H	H	V	V	V	110

**t<sub>REFI</sub> and t<sub>RFC</sub> parameters**

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e.,  $t_{REFI1} = t_{REFI(base)}$  (for  $T_{CASE} \leq 85^{\circ}\text{C}$ ), and the duration of each refresh command is the normal refresh cycle time ( $t_{RFC1}$ ). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the device at the double frequency ( $t_{REFI2} = t_{REFI(base)}/2$ ) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled ( $t_{REFI4} = t_{REFI(base)}/4$ ). Per each mode and command type,  $t_{RFC}$  parameter has different values as defined in the following table.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency ( $t_{REFI2} = t_{REFI(base)}/2$ ) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate ( $t_{REFI4} = t_{REFI(base)}/4$ ) may be referred to as a REF4x command.

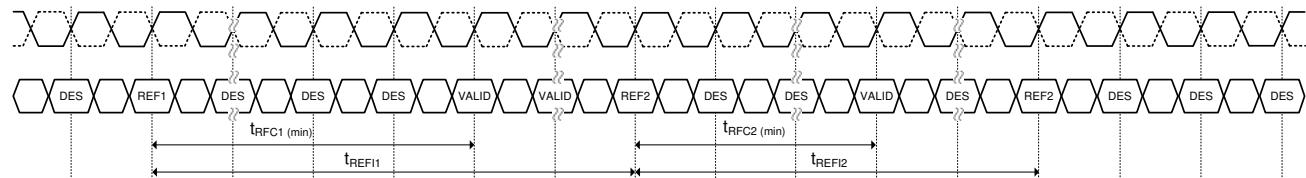
In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

**Table 19. Refresh command truth table**

Refresh Mode	Parameter		16Gb	Unit
	$t_{REFI(base)}$		7.8	$\mu\text{s}$
1x mode	$t_{REFI1}$	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI(base)}$	$\mu\text{s}$
		$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI(base)}/2$	$\mu\text{s}$
	$t_{RFC1}(\text{min})$		350	ns
2x mode	$t_{REFI2}$	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI(base)}/2$	$\mu\text{s}$
		$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI(base)}/4$	$\mu\text{s}$
	$t_{RFC2}(\text{min})$		260	ns
4X mode	$t_{REFI4}$	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	$t_{REFI(base)}/4$	$\mu\text{s}$
		$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	$t_{REFI(base)}/8$	$\mu\text{s}$
	$t_{RFC4}(\text{min})$		160	ns

## Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new  $t_{REFI}$  and  $t_{RFC}$  parameters would be applied from the moment of the rate change. When REF1x command is issued to the DRAM, then  $t_{REF1}$  and  $t_{RFC1}$  are applied from the time that the command was issued. When REF2x command is issued, then  $t_{REF2}$  and  $t_{RFC2}$  should be satisfied.



**Figure 24. On-the-fly Refresh Command Timing**

The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention cannot be guaranteed.

- In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued because the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
- In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
- In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

## **Usage with Temperature Controlled Refresh mode**

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; MR3 [8:6] = 000) is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

## **Self Refresh entry and exit**

The device can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows:

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval ( $t_{REFI}$ ).
3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval ( $t_{REFI}$ ).

## Self Refresh Operation

The Self-Refresh command can be used to retain data in the device, even if the rest of the system is powered down. When in the Self-Refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#/A16, CAS#/A15, and CKE held low with WE#/A14 and ACT# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the device must be idle with all bank precharge state with  $t_{RP}$  satisfied. Idle state is defined as all banks are closed ( $t_{RP}$ ,  $t_{DAL}$ , etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied ( $t_{MRD}$ ,  $t_{MOD}$ ,  $t_{RFC}$ ,  $t_{ZQinit}$ ,  $t_{ZQoper}$ ,  $t_{ZQCS}$ , etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and  $R_{TT\_PARK}$  set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set  $R_{TT\_PARK}$  asynchronously during  $t_{XSDLL}$  when  $R_{TT\_PARK}$  is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the device has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are “don’t care.” For proper Self-Refresh operation, all power supply and reference pins ( $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$ ,  $V_{PP}$ , and  $V_{REFCA}$ ) must be at valid levels. DRAM internal  $V_{REFDQ}$  generator circuitry may remain on or turned off depending on the MR6 bit 7 setting. If DRAM internal  $V_{REFDQ}$  circuitry is turned off in self refresh, when DRAM exits from self refresh state, it ensures that  $V_{REFDQ}$  generator circuitry is powered up and stable within  $t_{XS}$  period. First Write operation or first Write Leveling Activity may not occur earlier than  $t_{XS}$  after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within  $t_{CKE}$  period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is  $t_{CKESR}$ . The user may change the external clock frequency or halt the external clock  $t_{CKSRE}$  after Self- Refresh entry is registered, however, the clock must be restarted and stable  $t_{CKSRX}$  before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back high. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

Commands that do not require locked DLL:

- $t_{XS} = ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8$
- $t_{XSFast} = ZQCL, ZQCS, MRS$  commands. For MRS command, only DRAM CL and WR/RTP register and DLL Reset in MR0,  $R_{TT\_NOM}$  register in MR1, CWL and  $R_{TT\_WR}$  register in MR2 and geardown mode in MR3, Write and Read Preamble register in MR4,  $R_{TT\_PARK}$  register in MR5,  $t_{CCD\_L}/t_{DLK}$  and  $V_{REFDQ}$  Training Value in MR6 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy  $t_{XS}$  timing. Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

Commands that require locked DLL:

- $t_{XSDLL} = RD, RDS4, RDS8, RDA, RDAS4, RDAS8$

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in the ZQ Calibration Commands section. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain high for the entire Self-Refresh exit period  $t_{XSDLL}$  for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the device can be put back into Self-Refresh mode or Power down mode after waiting at least  $t_{XS}$  period and issuing one refresh command (refresh period of  $t_{RFC}$ ). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval  $t_{XS}$ . Low level of ODT pin must be registered on each positive clock edge during  $t_{XSDLL}$  when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.

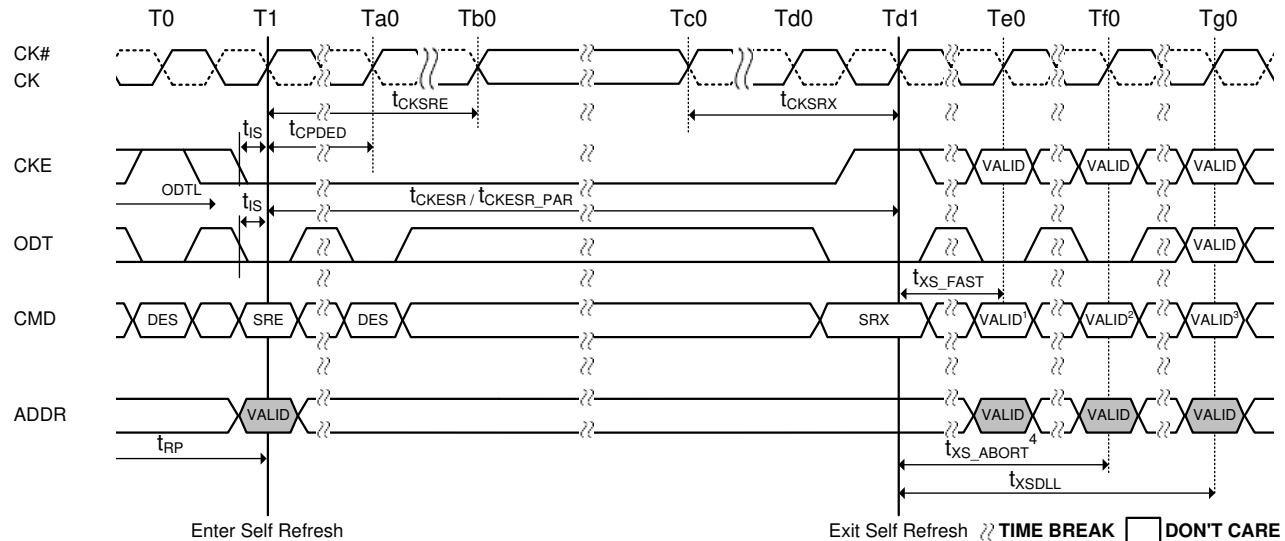
The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

## Self Refresh Abort

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is  $t_{XS}$ . The value of  $t_{XS}$  is  $(t_{RFC} + 10\text{ns})$ . This delay is to allow for any refreshes started by the DRAM to complete.  $t_{RFC}$  continues to grow with higher density devices so  $t_{XS}$  will grow as well.

A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses  $t_{XS}$  timings. If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of  $t_{XS\_ABORT}$ .

Upon exit from Self-Refresh, the device requires a minimum of one extra refresh command before it is put back into Self- Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.



NOTE 1. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

NOTE 2. Valid commands not requiring a locked DLL.

NOTE 3. Valid commands requiring a locked DLL.

NOTE 4. Only DES is allowed during  $t_{XS\_ABORT}$ .

Figure 25. Self-Refresh Entry/Exit Timing

## Low Power Auto Self Refresh (LPASR)

DDR4 devices support Low Power Auto Self-Refresh (LPASR) operation at multiple temperatures ranges (See temperature table below)

## **Auto Self Refresh (ASR)**

DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bits A6=1 and A7=1. The device will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, the device will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

## **Manual Modes**

If ASR mode is not enabled, the LPASR Mode Register must be manually programmed to one of the three self-refresh operating modes. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the self refresh according to their system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exiting from self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk to data retention resulting in loss of data.

**Table 20. Self Refresh Function table**

MR2 [A7]	MR2 [A6]	LPASR Mode	Self Refresh Operation	Allowed Operating Temperature Range for Self Refresh Mode (all reference to DRAM $T_{CASE}$ )
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85°C DRAM $T_{CASE(max)}$ is not exceeded to avoid any risk of data loss	(0°C ~ 85°C)
0	1	Reduced Temperature range	Variable or fixed self-Refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM $T_{CASE(max)}$ is not exceeded to avoid any risk of data loss	(0°C ~ 45°C)
1	0	Extended Temperature range	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(0°C ~ 95°C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption and data retention are optimized for any given operating temperature conditions	All of the above

## Power down Mode

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or Read / Write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams below illustrate entry and exit of power-down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

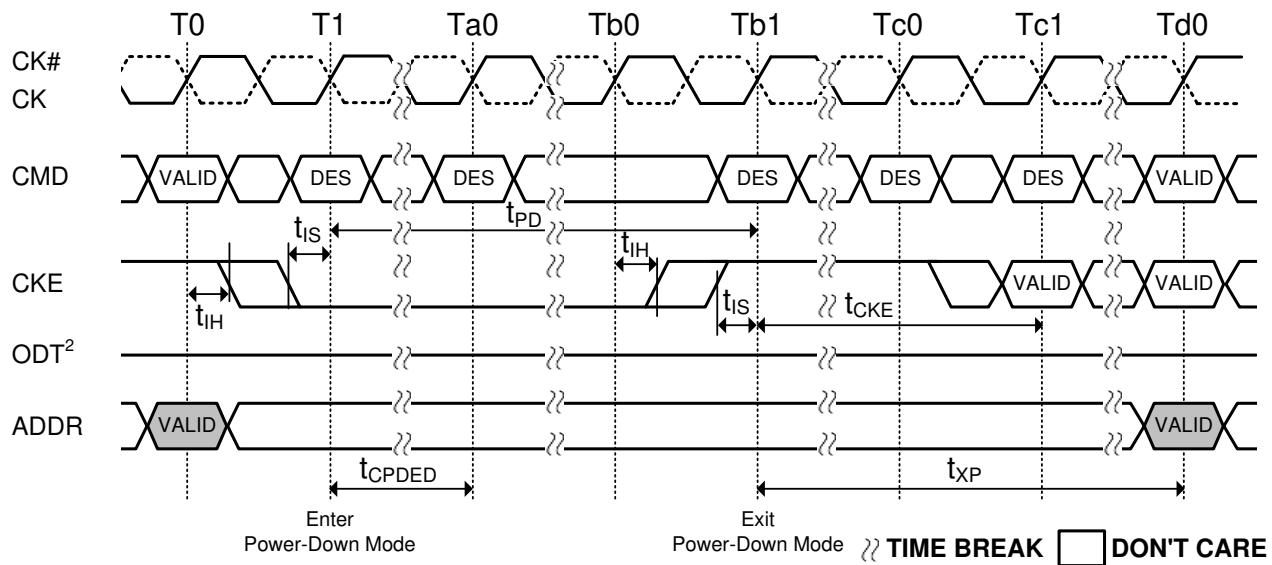
Entering power-down deactivates the input and output buffers, excluding CK, CK#, CKE and RESET#. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide  $R_{TT\_NOM}$  termination. Note that DRAM continues to provide  $R_{TT\_PARK}$  termination if it is enabled in DRAM mode register MR5 A[8:6]. To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as  $t_{CPDED}$ . CKE low will result in deactivation of command and address receivers after  $t_{CPDED}$  has expired.

**Table 21. Power-Down Entry Definitions**

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	$t_{XP}$ to any valid command
Precharged (All banks precharged)	On	Fast	$t_{XP}$ to any valid command

Also, the DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the device, and ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET# goes low during Power-Down, the device will be out of power-down mode and into reset state.) CKE low must be maintained until  $t_{CKE}$  has been satisfied. Power-down duration is limited by 9 times  $t_{REFI}$ .

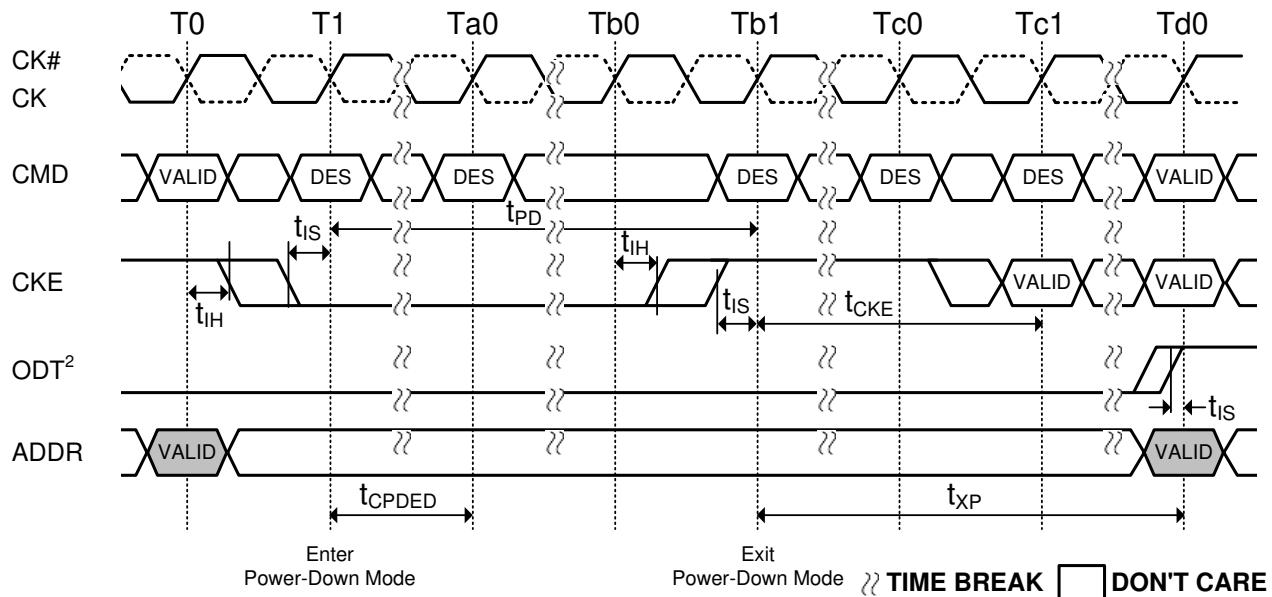
The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until  $t_{CKE}$  has been satisfied. The ODT input signal must be at valid level when device exits from power-down mode independent of MR5 bit A5 if  $R_{TT\_NOM}$  is enabled in DRAM mode register. If  $R_{TT\_NOM}$  is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency,  $t_{XP}$  after CKE goes high. Power-down exit latency is defined in the AC specifications table.



NOTE 1. Valid command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

NOTE 2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

**Figure 26. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5 = 0**



NOTE 1. Valid command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

NOTE 2. ODT pin driven to a valid state. MR5 bit A5=1 is shown.

**Figure 27. Active Power-Down Entry and Exit Timing Diagram MR5 bit A5=1**

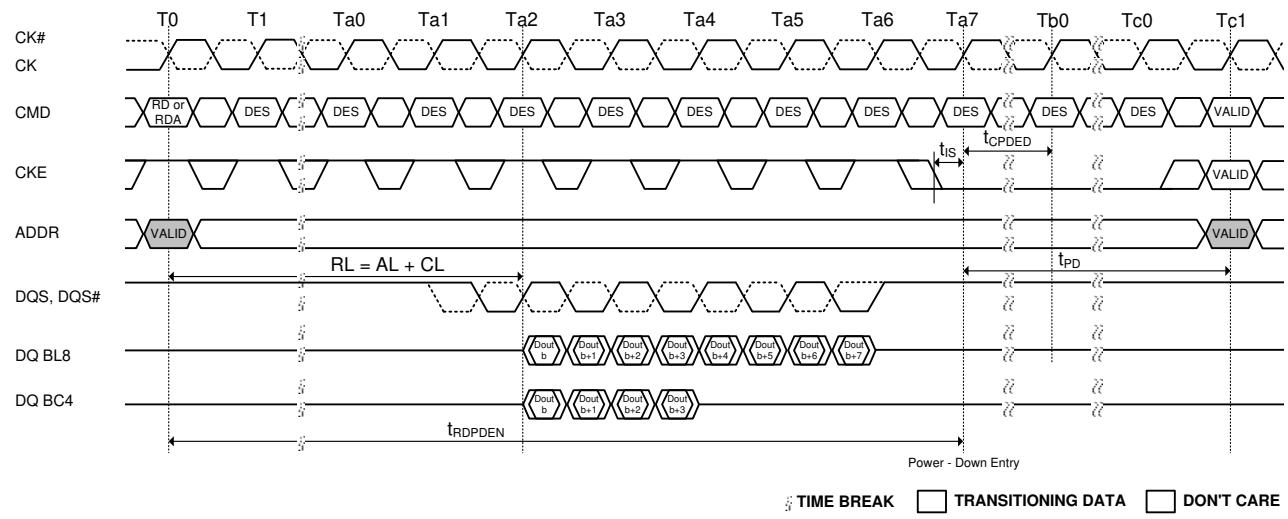


Figure 28. Power-Down Entry after Read and Read with Auto Precharge

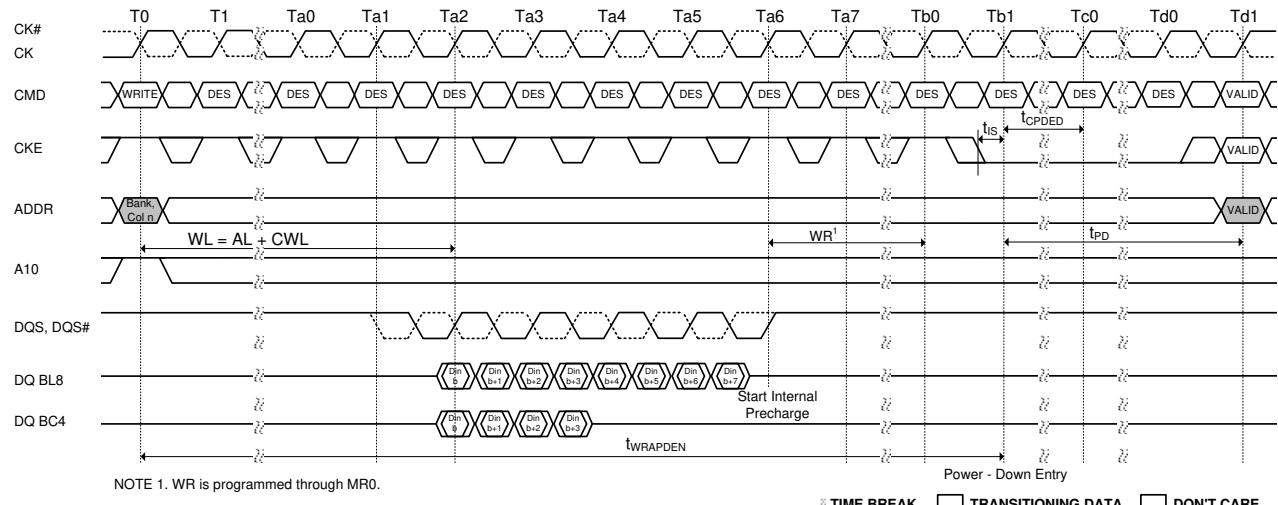


Figure 29. Power-Down Entry After Write with Auto Precharge

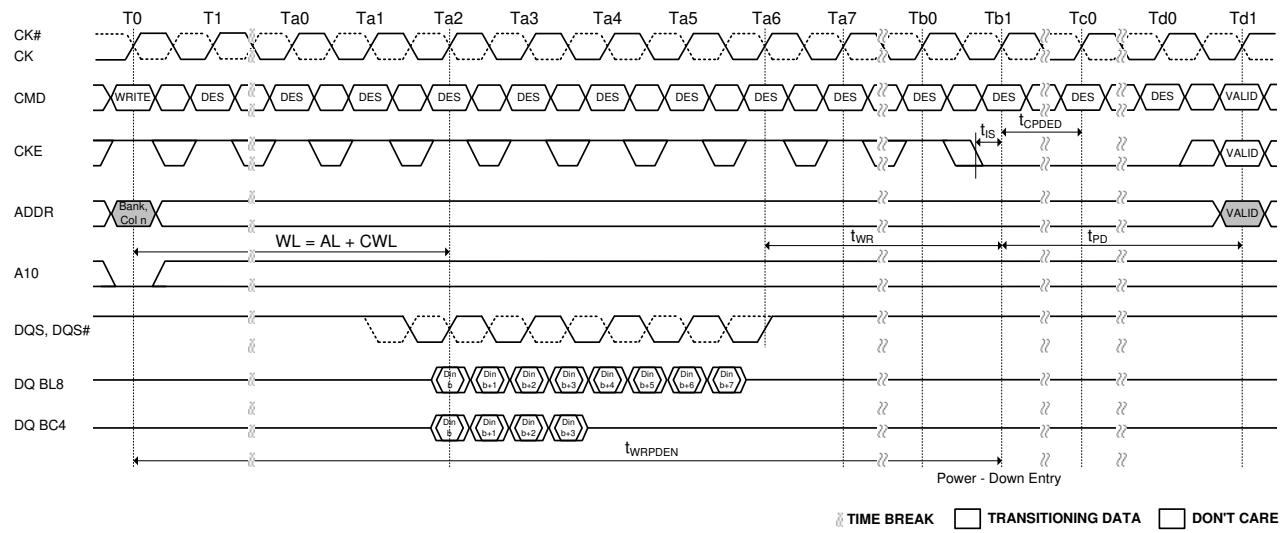


Figure 30. Power-Down Entry After Write

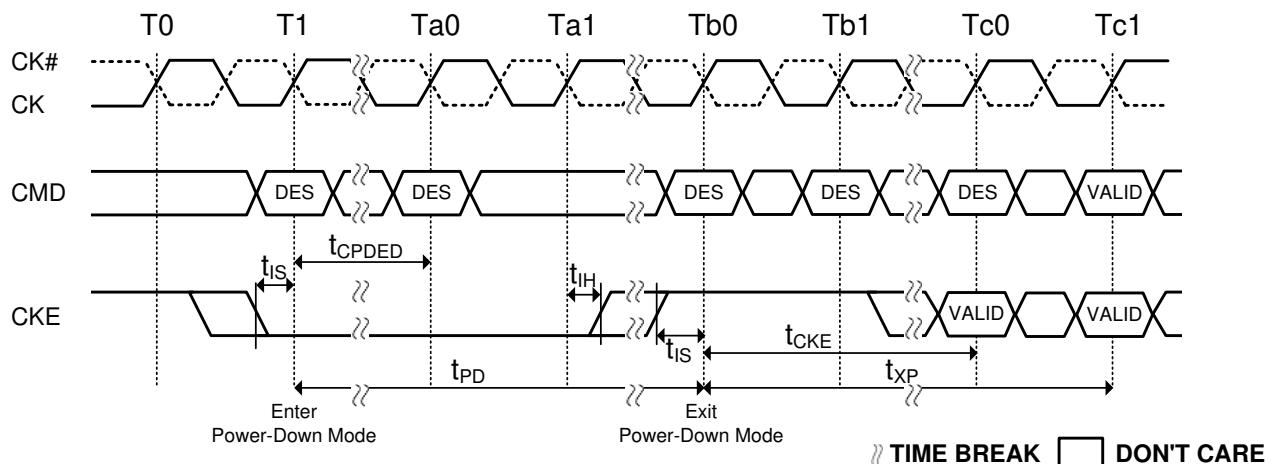


Figure 31. Precharge Power-Down Entry and Exit

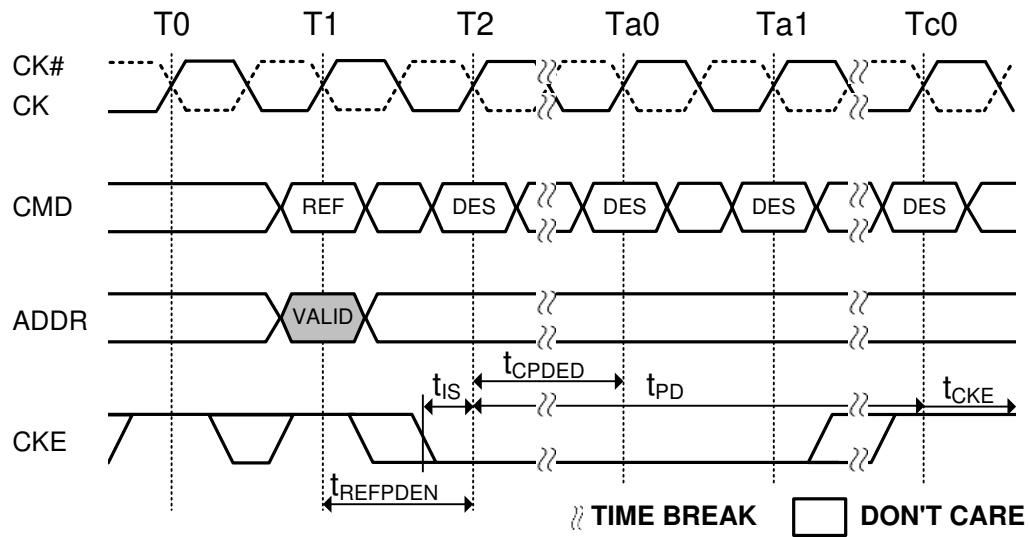


Figure 32. Refresh Command Power-Down Entry

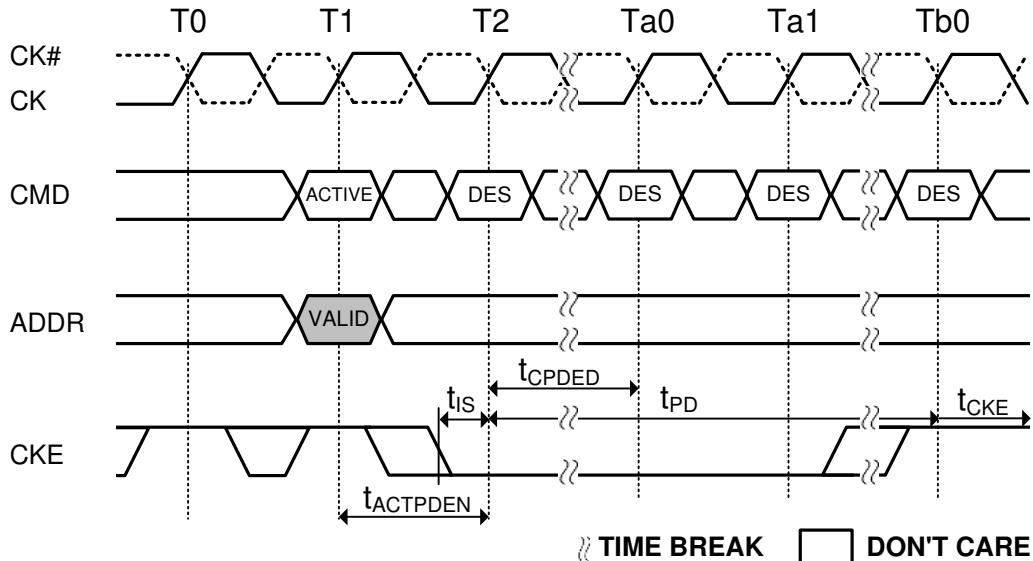


Figure 33. Activate Command Power-Down Entry

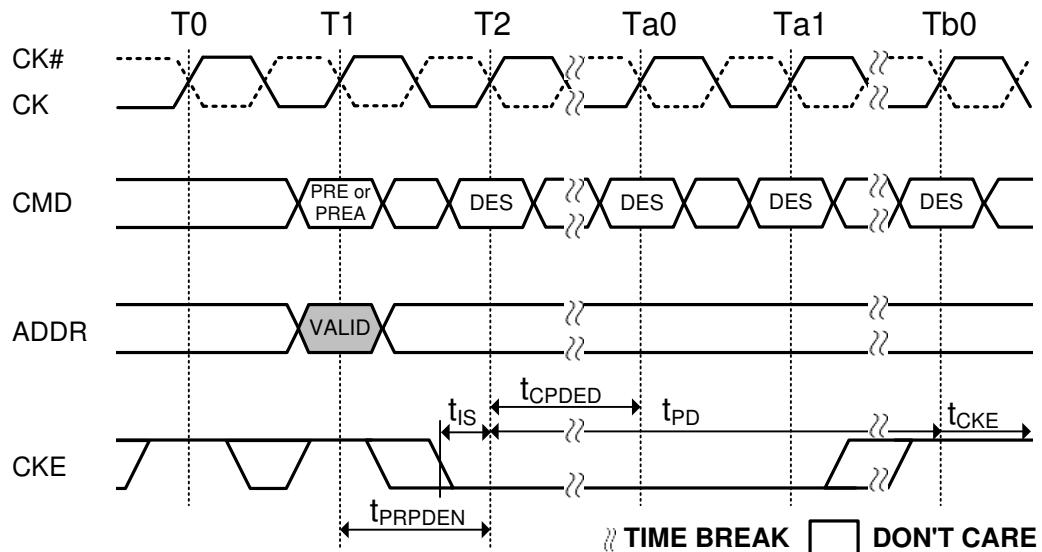


Figure 34. Precharge/Precharge all Command Power-Down Entry

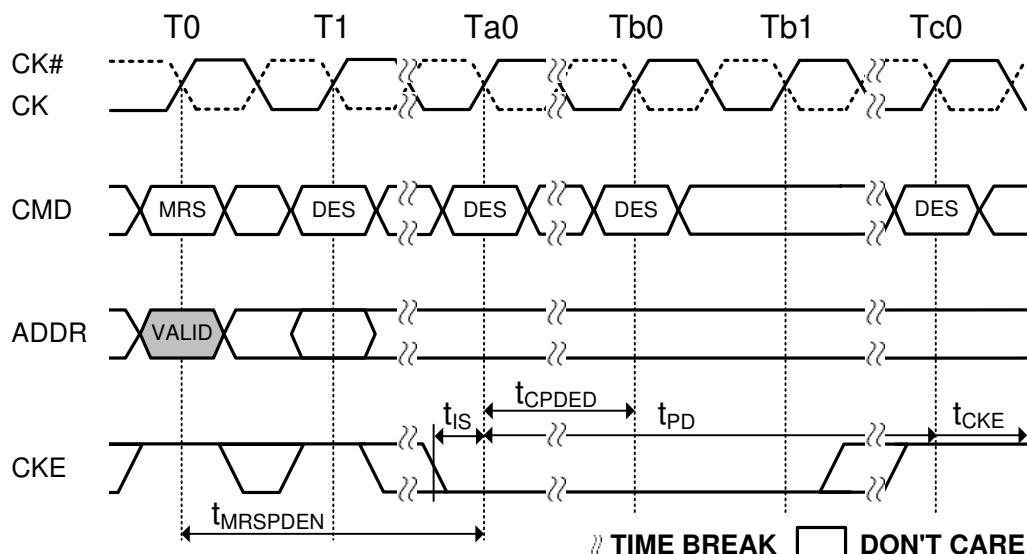


Figure 35. MRS Command Power-Down Entry

## Power-Down Clarifications

When CKE is registered low for power-down entry,  $t_{PD(MIN)}$  must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter  $t_{PD(MIN)}$  is equal to the minimum value of parameter  $t_{CKE(MIN)}$  as shown in the timing parameters table. A detailed example of Case 1 is shown below.

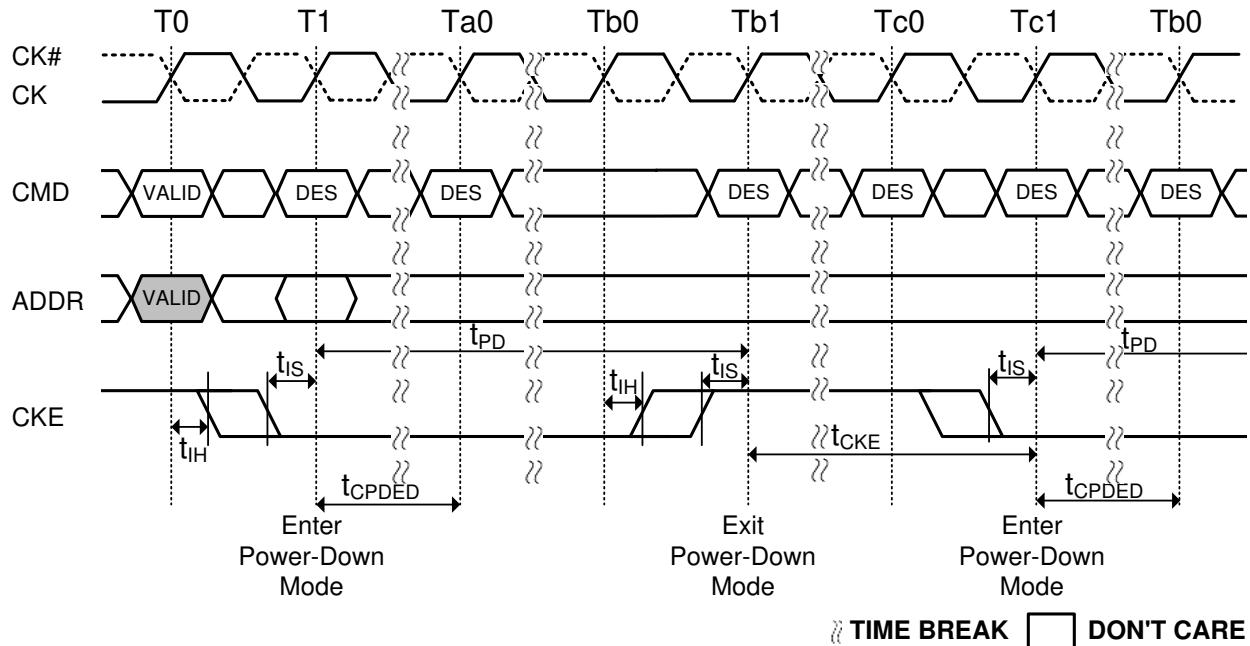
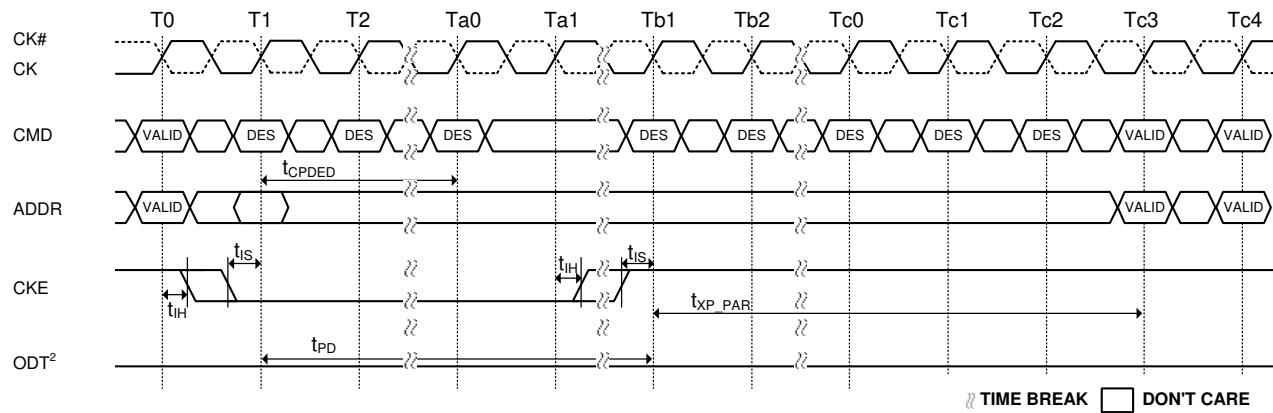


Figure 36. Power-Down Entry/Exit Clarification

## Power Down Entry and Exit timing during Command/Address Parity Mode is Enable

Power Down entry and exit timing during Command/Address Parity mode is enable shown below.



NOTE 1 VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

NOTE 2 ODT pin driven to a valid state, MR5[A5 = 0] (default setting) is shown

NOTE 3 CA Parity = Enable

**Figure 37. Power-Down Entry and Exit Timing with C/A Parity**

**Table 22. AC Timing Table**

Symbol	Parameter	Min.	Max.	Unit
$t_{XP\_PAR}$	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled	max (4nCK,6ns) + PL	-	

## Control Gear-down Mode

The following description represents the sequence for the gear-down mode which is specified with MR3 A[3]. This mode is allowed just during initialization and self refresh exit. The DRAM defaults in 1/2 rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS#, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode MRS command for geardown or sync pulse are not required. DRAM defaults in 1/2 rate mode.

General sequence for operation in geardown during initialization

- DRAM defaults to a 1/2 rate (1N mode) internal clock at power up/reset
- Assertion of Reset
- Assertion of CKE enables the DRAM
- MRS is accessed with a low frequency  $N \times t_{CK}$  geardown MRS command. ( $Nt_{CK}$  static MRS command qualified by 1N CS#)
- DRAM controller sends 1N sync pulse with a low frequency  $N \times t_{CK}$  NOP command.  $t_{SYNC\_GEAR}$  is an even number of clocks. The sync pulse on even clock boundary from MRS command.
- Initialization sequence, including the expiration of  $t_{DLLK}$  and  $t_{ZQinit}$ , starts in 2N mode after  $t_{CMD\_GEAR}$  from 1N Sync Pulse.

General sequence for operation in gear-down after self refresh exit

- DRAM reset to 1N mode during self refresh
- MRS is accessed with a low frequency  $N \times t_{CK}$  gear-down MRS command. ( $Nt_{CK}$  static MRS command qualified by 1N CS# which meets txs or txs\_Abort Only Refresh command is allowed to be issued to DRAM before  $Nt_{CK}$  static MRS command.
- DRAM controller sends 1N sync pulse with a low frequency  $N \times t_{CK}$  NOP command.  $t_{SYNC\_GEAR}$  is an even number of clocks Sync pulse is on even clock boundary from MRS command.
- Valid command not requiring locked DLL is available in 2N mode after  $t_{CMD\_GEAR}$  from 1N Sync Pulse.
- Valid command requiring locked DLL is available in 2N mode after  $t_{DLLK}$  from 1N Sync Pulse.

If operation is 1/2 rate(1N) mode after self refresh, no  $N \times t_{CK}$  MRS command or sync pulse is required during self refresh exit. The min exit delay is txs or txs\_Abort to the first valid command.

The DRAM may be changed from 1/4 rate ( 2N ) to 1/2 rate ( 1N ) by entering Self Refresh Mode, which will reset to 1N automatically. Changing from 1/4 ( 2N ) to 1/2 rate ( 1 N ) by any other means, including setting MR3[A3] from 1 to 0, can result in loss of data and operation of the DRAM uncertain.

For the operation of geardown mode in 1/4 rate, the following MR settings should be applied.

CAS Latency (MR0 A[6:4,2]) : Even number of clocks

Write Recovery and Read to Precharge (MR0 A[11:9]) : Even number of clocks

Additive Latency (MR1 A[4:3]) : 0, CL -2

CAS Write Latency (MR2 A[5:3]) : Even number of clocks

CS to Command/Address Latency Mode (MR4 A[8:6]): Even number of clocks

CA Parity Latency Mode (MR5 A[2:0]) : Even number of clocks

CAL or CA parity mode must be disabled prior to Gear down MRS command. They can be enabled again after  $t_{SYNC\_GEAR}$  and  $t_{CMD\_GEAR}$  periods are satisfied.

The diagram below illustrates the sequence for control operation in 2N mode during initialization.

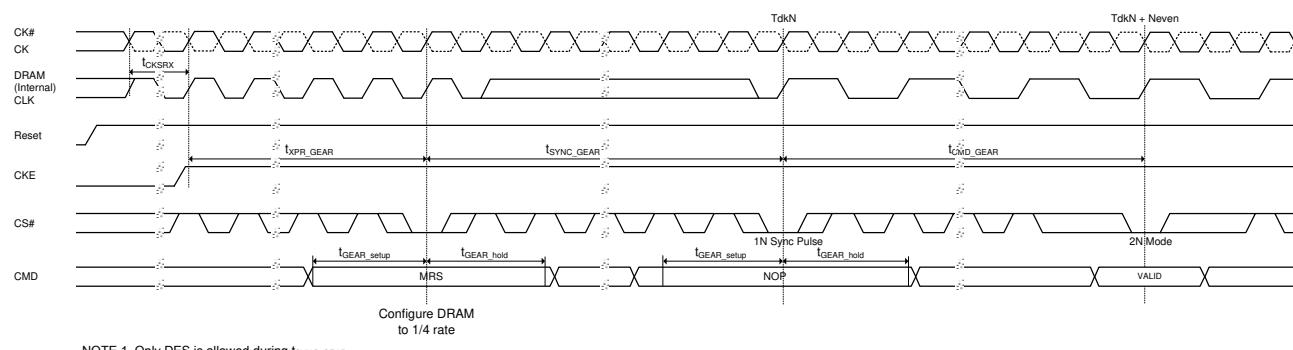
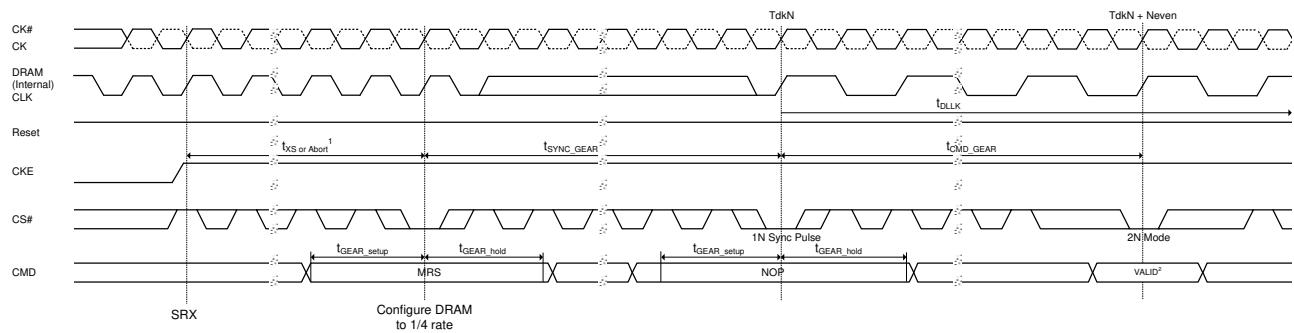


Figure 38. Gear down (2N) mode entry sequence during initialization



NOTE 1. CKE High Assert to Gear Down Enable Time ( $t_{XS}$ ,  $t_{XS\_Abort}$ ) depend on MR setting. A correspondence of  $t_{XS}$ / $t_{XS\_Abort}$  and MR Setting is as follows.

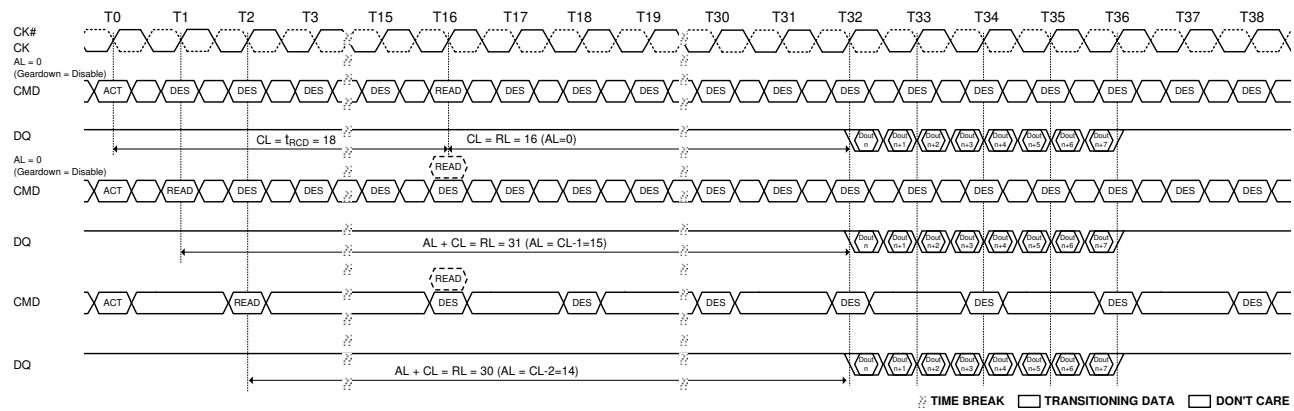
- MR4[A9] = 0 :  $t_{XS}$

- MR4[A9] = 1 :  $t_{XS\_Abort}$

NOTE 2. Command not requiring locked DLL

NOTE 3. Only DES is allowed during  $t_{SYNC\_GEAR}$

**Figure 39. Gear down (2N) mode entry sequence after self refresh exit (SRX)**



NOTE 1. BL = 8, t<sub>RCD</sub> = CL = 16

NOTE 2. D<sub>OUT</sub> n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

**Figure 40. Comparison Timing Diagram Between Geardown Disable and Enable**

## Refresh Command

The Refresh command (REF) is used during normal operation of the device. This command is non persistent, so it must be issued each time a refresh is required. The device requires Refresh cycles at an average periodic interval of  $t_{REFI}$ . When CS#, RAS#/A16 and CAS#/A15 are held Low and WE#/A14 and ACT# are held High at the rising edge of the clock, the device enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time  $t_{RP(min)}$  before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time  $t_{RFC(min)}$ . The  $t_{RFC}$  timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the device regularly every  $t_{REFI}$  interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when the device is in 1X refresh mode; a maximum of 16 Refresh commands can be postponed when the device is in 2X refresh mode; and a maximum of 32 Refresh commands can be postponed when the device is in 4X refresh mode.

When 8 consecutive Refresh commands are postponed, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times t_{REFI}$ . For both the 2X and 4X refresh modes, the maximum interval between surrounding Refresh commands allowed is limited to  $17 \times t_{REFI}2$  and  $33 \times t_{REFI}4$ , respectively.

A limited number Refresh commands can be pulled-in as well. A maximum of 8 additional Refresh commands can be issued in advance or "pulled-in" in 1X refresh mode, a maximum of 16 additional Refresh commands can be issued when in advance in 2X refresh mode, and a maximum of 32 additional Refresh commands can be issued in advance when in 4X refresh mode. Each of these Refresh commands reduces the number of regular Refresh commands required later by one. Note that pulling in more than the maximum allowed Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times t_{REFI}$ ,  $17 \times t_{REFI}2$ , or  $33 \times t_{REFI}4$ . At any given time, a maximum of 16 additional REF commands can be issued within  $2 \times t_{REFI}$ , 32 additional REF2 commands can be issued within  $4 \times t_{REFI}2$ , and 64 additional REF4 commands can be issued within  $8 \times t_{REFI}4$  (larger densities are limited by  $t_{RFC1}$ ,  $t_{RFC2}$ , and  $t_{RFC4}$ , respectively, which must still be met).

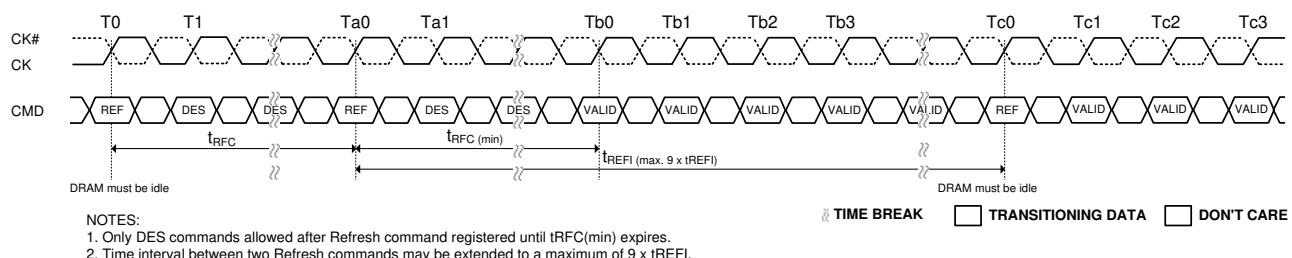


Figure 41. Refresh Command Timing (Example of 1x Refresh mode)

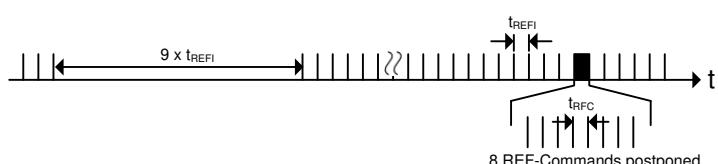


Figure 42. Postponing Refresh Commands (Example of 1X Refresh mode)

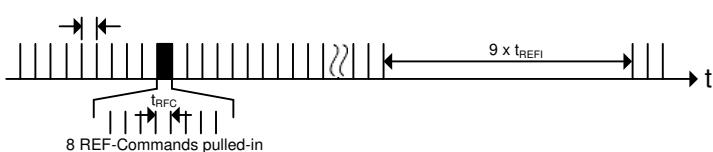


Figure 43. Pulling-in Refresh Commands (Example of 1X Refresh mode)

## Data Mask (DM), Data Bus Inversion (DBI)

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) function in x16 DRAM configuration.

DM#, DBI# functions are supported with dedicated one pin labeled as DM#/DBI#/TDQS. The pin is bi-directional pin for DRAM. The DM#/DBI# pin is Active Low as DDR4 supports  $V_{DDQ}$  reference termination. DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A12:A10 in MR5.

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultaneously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.

Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

**Table 23. DM vs. DBI Function Matrix**

DM (MR5 bit A10)	Write DBI (MR5 bit A11)	Read DBI (MR5 bit A12)
Enabled	Disabled	Enabled or Disabled
Disabled	Enabled	Enabled or Disabled
Disabled	Disabled	Enabled or Disabled
Disabled	Disabled	Disabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if DM# was sampled Low on a given byte lane. If DM# was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if DBI# was sampled Low on a given byte lane. If DBI# was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives DBI# pin Low when the number of '0' data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives DBI# pin High.

**Table 24. DQ Frame Format**

Write	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDM# or LDBI#	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM# or UDBI#	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7
Read	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDBI#	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDBI#	UDBI0	UDBI1	UDBI2	UDBI3	UDBI4	UDBI5	UDBI6	UDBI7

## ZQ Calibration Commands

ZQ Calibration command is used to calibrate DRAM  $R_{ON}$  & ODT values. The device needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of  $t_{ZQinit}$  to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of  $t_{ZQoper}$ .

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter  $t_{ZQCS}$ . One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of  $R_{ON}$  and  $R_{TT}$  impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver Voltage and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature ( $T_{driftrate}$ ) and voltage ( $V_{driftrate}$ ) drift rates that the device is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(Tsens \times Tdriftrate) + (Vsens \times Vdriftrate)}$$

Where  $T_{sens} = \max(dR_{TT}dT, dR_{ON}dT)$  and  $V_{sens} = \max(dR_{TT}dV, dR_{ON}dV)$  define temperature and voltage sensitivities.

For example, if  $T_{sens} = 1.5\text{%/}^{\circ}\text{C}$ ,  $V_{sens} = 0.15\text{%/mV}$ ,  $T_{driftrate} = 1^{\circ}\text{C/sec}$  and  $V_{driftrate} = 15\text{mV/sec}$ , then the interval between ZQCS commands is calculated as:

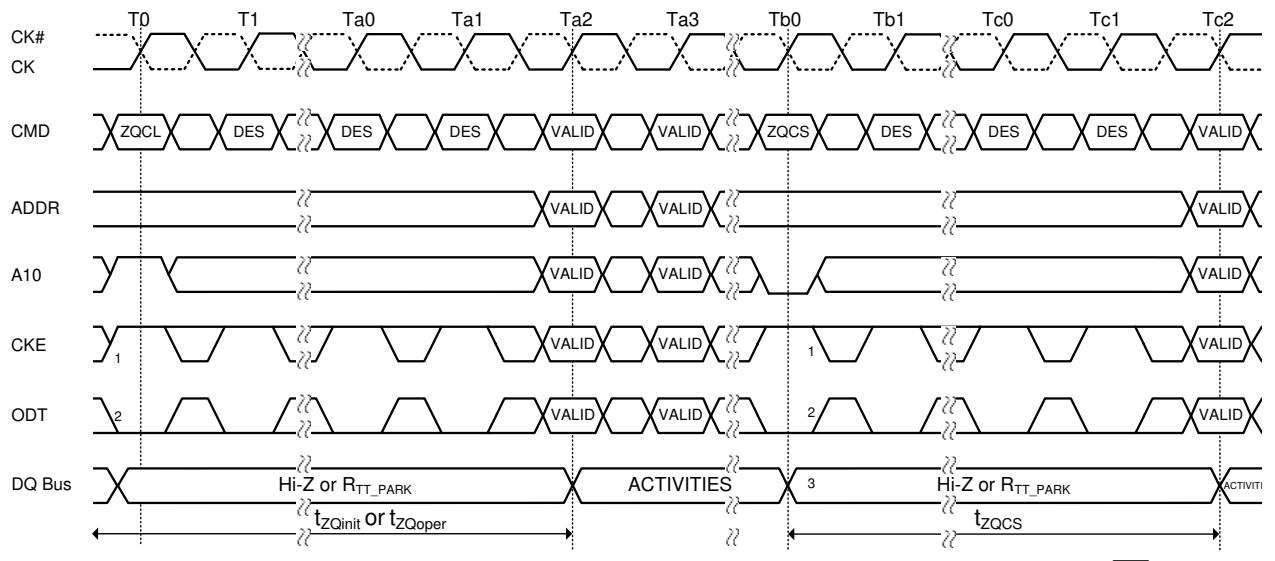
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of  $t_{ZQinit}$ ,  $t_{ZQoper}$ , or  $t_{ZQCS}$ . The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the device should disable ZQ current consumption path to reduce power.

All banks must be precharged and  $t_{RP}$  met before ZQCL or ZQCS commands are issued by the controller. See "Command Truth Table" on Section 4.1 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, the device will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is  $t_{XS}$ ,  $t_{XS\_Abort}$  /  $t_{XS\_FAST}$  depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of  $t_{ZQoper}$ ,  $t_{ZQinit}$ , or  $t_{ZQCS}$  between the devices.



NOTE 1. CKE must be continuously registered high during the calibration procedure.

NOTE 2. During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide  $R_{TT\_PARK}$ .

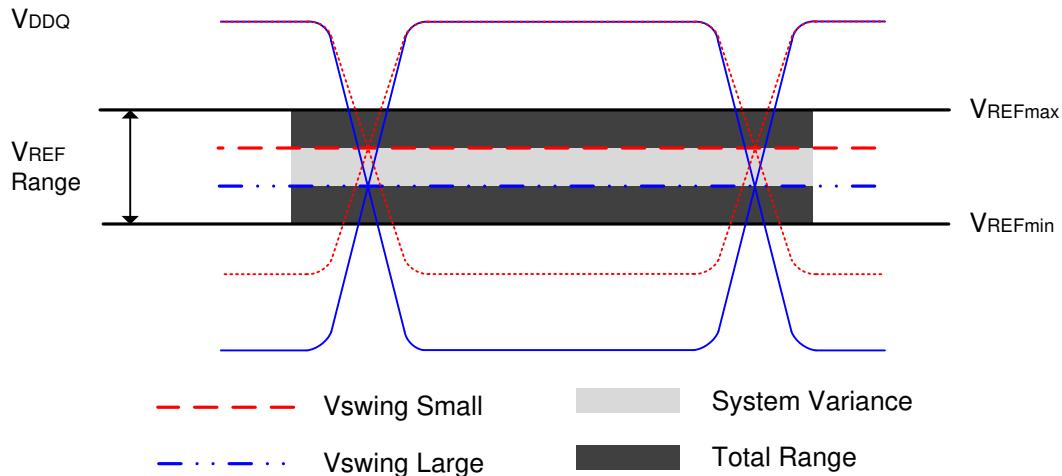
NOTE 3. All devices connected to the DQ bus should be high impedance or  $R_{TT\_PARK}$  during the calibration procedure.

Figure 44. ZQ Calibration Timing

## DQ V<sub>REF</sub> Training

The DRAM internal DQ V<sub>REF</sub> specification parameters are operating voltage range, stepsize, V<sub>REF</sub> step time, V<sub>REF</sub> full step time and V<sub>REF</sub> valid level.

The voltage operating range specifies the minimum required V<sub>REF</sub> setting range for DDR4 DRAM devices. The minimum range is defined by V<sub>REFmax</sub> and V<sub>REFmin</sub> as depicted in the following figure.

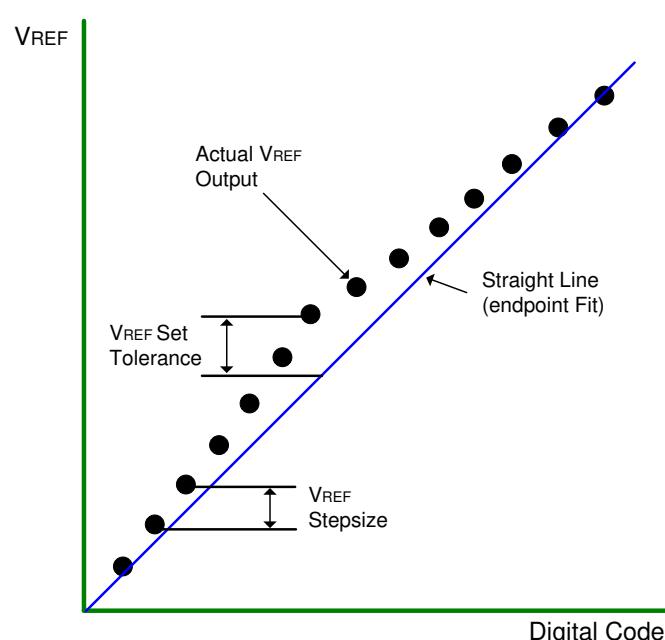


**Figure 45. V<sub>REFDQ</sub> Operating Range (V<sub>REFmin</sub>, V<sub>REFmax</sub>)**

The V<sub>REF</sub> stepsize is defined as the stepsize between adjacent steps. V<sub>REF</sub> stepsize ranges from 0.5% V<sub>DDQ</sub> to 0.8% V<sub>DDQ</sub>. However, for a given design, DRAM has one value for V<sub>REF</sub> step size that falls within the range.

The V<sub>REF</sub> set tolerance is the variation in the V<sub>REF</sub> voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V<sub>REF</sub> set tolerance uncertainty. The range of V<sub>REF</sub> set tolerance uncertainty is a function of number of steps n.

The V<sub>REF</sub> set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max V<sub>REF</sub> values for a specified range. An illustration depicting an example of the stepsize and V<sub>REF</sub> set tolerance is below.



**Figure 46. Example of V<sub>REF</sub> set tolerance (max case only shown) and stepsize**

The  $V_{REF}$  increment/decrement step times are defined by  $V_{REF\_time}$ . The  $V_{REF\_time}$  is defined from  $t_0$  to  $t_1$ , where  $t_1$  is referenced to when the  $V_{REF}$  voltage is at the final DC level within the  $V_{REF}$  valid tolerance ( $V_{REF\_val\_tol}$ ).

The  $V_{REF}$  valid level is defined by  $V_{REF\_val}$  tolerance to qualify the step time  $t_1$ . This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any  $V_{REF}$  increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

$V_{REF\_time}$  is the time including up to  $V_{REFmin}$  to  $V_{REFmax}$  or  $V_{REFmax}$  to  $V_{REFmin}$  change in  $V_{REF}$  voltage.

$t_0$  - is referenced to MRS command clock

$t_1$  - is referenced to the  $V_{REF\_val\_tol}$

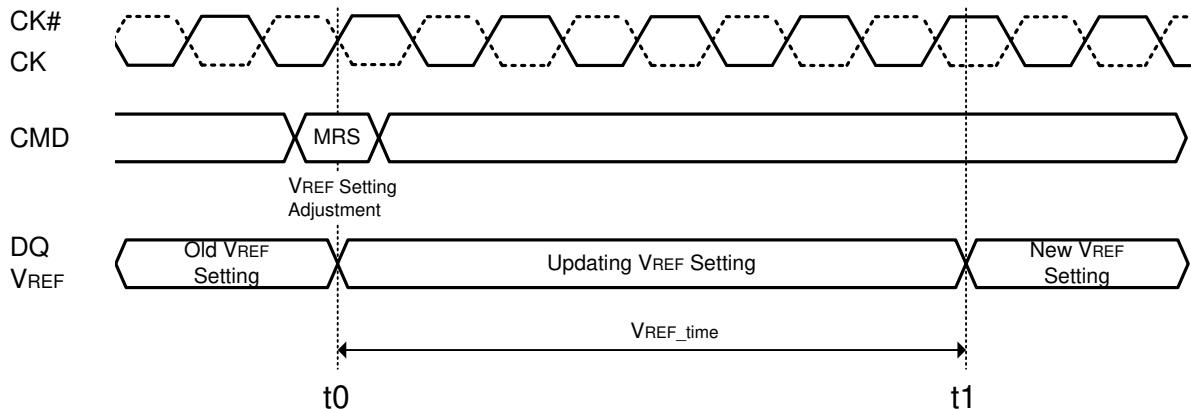
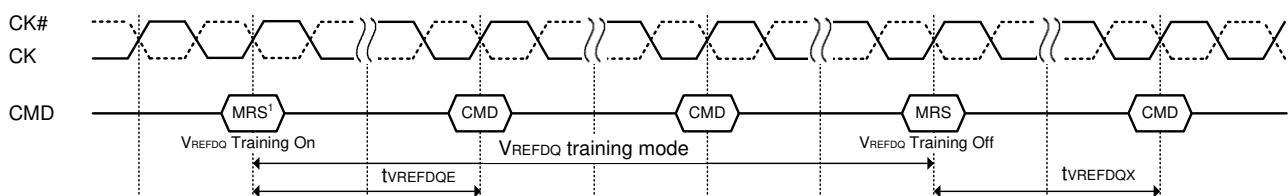


Figure 47.  $V_{REF\_time}$  timing diagram

$V_{REFDQ}$  Calibration Mode is entered via MRS command setting MR6 A[7] to 1 (0 disables  $V_{REFDQ}$  Calibration Mode), and setting MR6 A[6] to either 0 or 1 to select the desired range, and MR6 A[5:0] with a “don’t care” setting (there is no default initial setting; whether  $V_{REFDQ}$  training value (MR6 A[5:0]) at training mode entry with MR6 A[7] = 1 is captured by the DRAM or not is vendor specific). The next subsequent MR command is used to set the desired  $V_{REFDQ}$  values at MR6 A[5:0]. Once  $V_{REFDQ}$  Calibration Mode has been entered,  $V_{REFDQ}$  Calibration Mode legal commands may be issued once  $t_{VREFDQE}$  has been satisfied.  $V_{REFDQ}$  Calibration Mode legal commands are ACT, WR, WRA, RD, RDA, PRE, DES, MRS to set  $V_{REFDQ}$  values, and MRS to exit  $V_{REFDQ}$  Calibration Mode. Once  $V_{REFDQ}$  Calibration Mode has been entered, “dummy” write commands may be issued prior to adjusting  $V_{REFDQ}$  value the first time  $V_{REFDQ}$  calibration is performed after initialization. The “dummy” write commands may have bubbles between write commands provided other DRAM timings are satisfied. A possible example command sequence would be: WR1, DES, DES, DES, WR2, DES, DES, DES, WR3, DES, DES, DES, WR4, DES, DES.....DES, DES, WR50, DES, DES, DES. Setting  $V_{REFDQ}$  values requires MR6 [7] set to 1, MR6 [6] unchanged from initial range selection, and MR6 A[5:0] set to desired  $V_{REFDQ}$  value; if MR6 [7] is set to 0, MR6 [6:0] are not written.  $V_{REF\_time}$  must be satisfied after each MR command to set  $V_{REFDQ}$  value before the internal  $V_{REFDQ}$  value is valid.

If PDA mode is used in conjunction with  $V_{REFDQ}$  calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only  $V_{REFDQ}$  Calibration Mode legal commands noted above that may be used are the MRS commands, i.e. MRS to set  $V_{REFDQ}$  values, and MRS to exit  $V_{REFDQ}$  Calibration Mode.

The last A [6:0] setting written to MR6 prior to exiting  $V_{REFDQ}$  Calibration Mode is the range and value used for the internal  $V_{REFDQ}$  setting.  $V_{REFDQ}$  Calibration Mode may be exited when the DRAM is in idle state. After the MRS command to exit  $V_{REFDQ}$  Calibration Mode has been issued, DES must be issued till  $t_{VREFDQX}$  has been satisfied where any legal command may then be issued.



NOTE 1. The MR command used to enter  $V_{REFDQ}$  Calibration Mode treats MR6 A [5:0] as don’t care while the next subsequent MR command sets  $V_{REFDQ}$  values in MR6 A[5:0].

NOTE 2. Depending on the step size of the latest programmed  $V_{REF}$  value,  $V_{REF\_time}$  must be satisfied before disabling  $V_{REFDQ}$  training mode.

Figure 48.  $V_{REFDQ}$  training mode entry and exit timing diagram

**Table 25. AC parameters of V<sub>REFDQ</sub> training**

Symbol	Parameter	Min.	Max.	Unit
t <sub>VREFDQE</sub>	Enter V <sub>REFDQ</sub> training mode to the first valid command delay	150	-	ns
t <sub>VREFDQX</sub>	Exit V <sub>REFDQ</sub> training mode to the first valid command delay	150	-	ns

### Example scripts for V<sub>REFDQ</sub> Calibration Mode

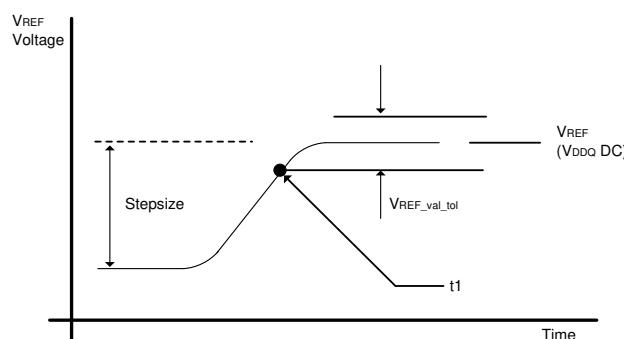
When MR6 [7] = 0 then MR6 [6:0] = XXXXXXXX

Entering V<sub>REFDQ</sub> Calibration if entering range 1:

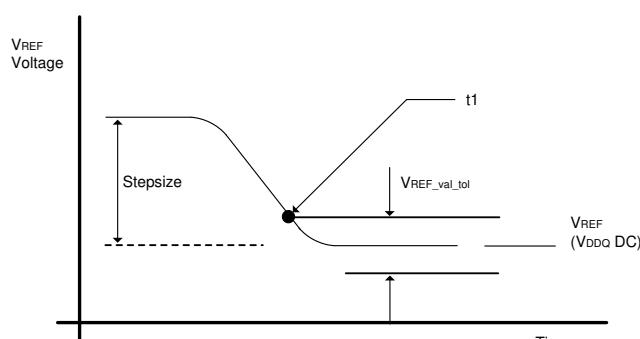
- MR6 [7:6] = 10 & [5:0] = XXXXXX
- All subsequent V<sub>REFDQ</sub> Calibration MR setting commands are MR6 [7:6] = 10 & MR6 [5:0] = VVVVVV
  - {VVVVVV are desired settings for V<sub>REFDQ</sub>}
- Issue ACT/WR/RD looking for pass/fail to determine V<sub>CENT</sub>(midpoint) as needed
- Just prior to exiting V<sub>REFDQ</sub> Calibration mode:
- Last two V<sub>REFDQ</sub> Calibration MR commands are
- MR6 [7:6] = 10, MR6 [5:0] = VVVVVV' where VVVVVV' = desired value for V<sub>REFDQ</sub>
- MR6 [7] = 0, MR6 [6:0] = XXXXXXXX to exit V<sub>REFDQ</sub> Calibration mode

Entering V<sub>REFDQ</sub> Calibration if entering range 2:

- MR6 [7:6] = 11 & [5:0] = XXXXXX
- All subsequent V<sub>REFDQ</sub> Calibration MR setting commands are MR6 [7:6]=11 & MR6 [5:0]=VVVVVV
  - {VVVVVV are desired settings for V<sub>REFDQ</sub>}
- Issue ACT/WR/RD looking for pass/fail to determine V<sub>CENT</sub>(midpoint) as needed
- Just prior to exiting V<sub>REFDQ</sub> Calibration mode:
- Last two V<sub>REFDQ</sub> Calibration MR commands are
- MR6 [7:6] = 11, MR6 [5:0] = VVVVVV' where VVVVVV' = desired value for V<sub>REFDQ</sub>
- MR6 [7] = 0, MR6 [6:0] = XXXXXXXX to exit V<sub>REFDQ</sub> Calibration mode



**Figure 49. V<sub>REF</sub> step single stepsize increment case**



**Figure 50. V<sub>REF</sub> step single stepsize decrement case**

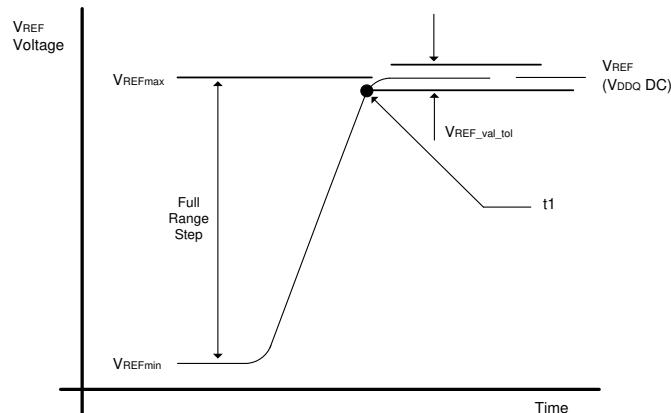


Figure 51. VREF full step from VREFmin to VREFmax case

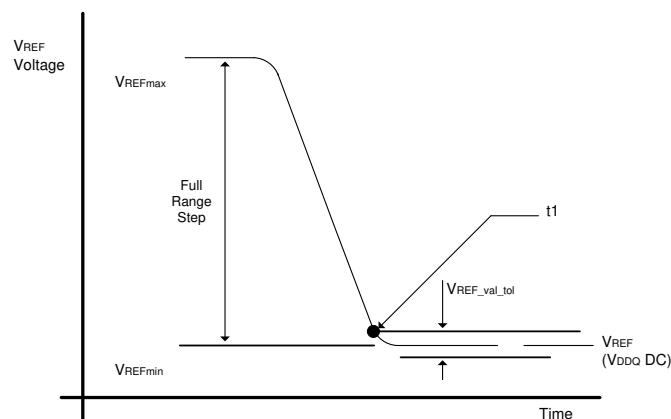


Figure 52. VREF full step from VREFmax to VREFmin case

Table 26. DQ Internal VREF Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VREF_max_R1	VREF max operating point range1	92%	-	-	V <sub>DDQ</sub>	1,10
VREF_min_R1	VREF min operating point range1	-	-	60%	V <sub>DDQ</sub>	1,10
VREF_max_R2	VREF max operating point range2	77%	-	-	V <sub>DDQ</sub>	1,10
VREF_min_R2	VREF min operating point range2	-	-	45%	V <sub>DDQ</sub>	1,10
VREF step	VREF Stepsize	0.50%	0.65%	0.80%	V <sub>DDQ</sub>	2
VREF_set_tol	VREF Set Tolerance	-1.625%	0.00%	1.625%	V <sub>DDQ</sub>	3,4,6
		-0.15%	0.00%	0.15%	V <sub>DDQ</sub>	3,5,7
VREF_time	VREF Step Time	-	-	150	ns	8,11
VREF_val_tol	VREF Valid tolerance	-0.15%	0.00%	0.15%	V <sub>DDQ</sub>	9

Note 1. V<sub>REF</sub> DC voltage referenced to V<sub>DDQ DC</sub>. V<sub>DDQ DC</sub> is 1.2V.

Note 2. V<sub>REF</sub> stepsize increment/decrement range. V<sub>REF</sub> at DC level.

Note 3. V<sub>REF\_new</sub> = V<sub>REF\_old</sub> + n × V<sub>REF\_step</sub>; n = number of step; if increment use "+"; If decrement use "-".

Note 4. The minimum value of V<sub>REF</sub> setting tolerance = V<sub>REF\_new</sub> - 1.625% × V<sub>DDQ</sub>. The maximum value of V<sub>REF</sub> setting tolerance = V<sub>REF\_new</sub> + 1.625% × V<sub>DDQ</sub> for n > 4.

Note 5. The minimum value of V<sub>REF</sub> setting tolerance = V<sub>REF\_new</sub> - 0.15% × V<sub>DDQ</sub>. The maximum value of V<sub>REF</sub> setting tolerance = V<sub>REF\_new</sub> + 0.15% × V<sub>DDQ</sub> for n > 4.

Note 6. Measured by recording the min and max values of the V<sub>REF</sub> output over the range, drawing a straight line between those points and comparing all other V<sub>REF</sub> output settings to that line.

Note 7. Measured by recording the min and max values of the V<sub>REF</sub> output across 4 consecutive steps (n = 4), drawing a straight line between those points and comparing all other V<sub>REF</sub> output settings to that line.

Note 8. Time from MRS command to increment or decrement one step size up to full range of V<sub>REF</sub>.

Note 9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V<sub>REF</sub> valid is to qualify the step times which will be characterized at the component level.

Note 10. DRAM range1 or 2 set by MRS bit MR6, A6.

Note 11. If the V<sub>REF</sub> monitor is enabled, V<sub>REF\_time</sub> must be derated by: +10ns if DQ load is 0pF and an additional +15ns/pF of DQ loading.

## Per DRAM Addressability

DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or  $V_{REF}$  values on DRAM devices on a given rank.

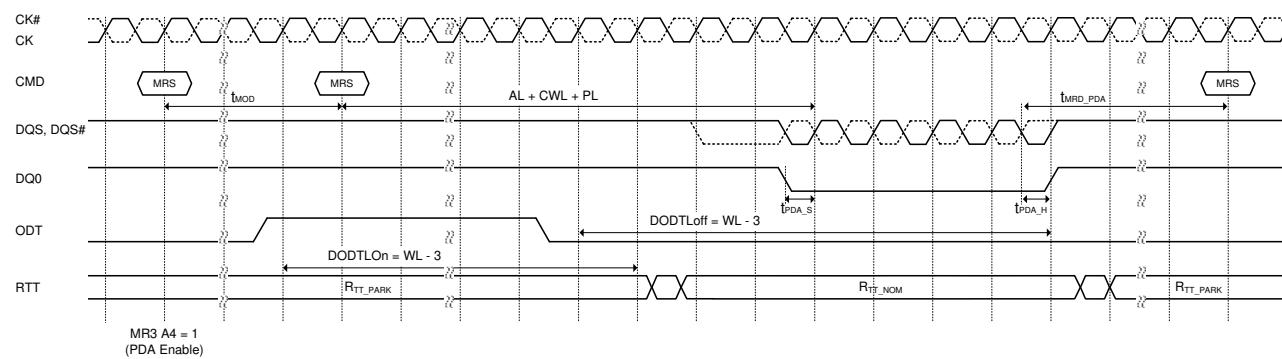
1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
  - BL8 or BC4 may be used.
2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.
  - $R_{TT\_PARK}$  MR5 A[8:6] = Enable
  - $R_{TT\_NOM}$  MR1 A[10:8] = Enable
3. Enable 'per DRAM addressability (PDA)' mode using MR3 A[4] = 1.
4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is low, the DRAM executes the MRS command. If the value on DQ0 is high, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired devices and mode registers using MRS command and DQ0.
6. In the 'per DRAM addressability' mode, only MRS commands are allowed.
7. The mode register set command cycle time at PDA mode,  $AL + CWL + BL/2 - 0.5t_{CK} + t_{MRD\_PDA} + (PL)$  is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the device from 'per DRAM addressability' mode by setting MR3 A[4] = 0. (This command will require DQ0 = 0)

**Note:** Removing a device from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls.

In per DRAM addressability mode, device captures DQ0 using DQS signals the same as in a normal write operation; However, Dynamic ODT is not supported. Extra care required for the ODT setting. If  $R_{TT\_NOM}$  MR1 A[10:8] = Enable, device data termination need to be controlled by ODT pin and apply the same timing parameters (defined below).  $V_{REFDQ}$  value must be set to either its midpoint or  $V_{cent\_DQ}$  (midpoint) in order to capture DQ0 low level for entering PDA mode.

**Table 27. Applied ODT Timing Parameter to PDA Mode**

Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTloff	Direct ODT turn off latency
$t_{ADC}$	$R_{TT}$ change timing skew
$t_{AO_NAS}$	Asynchronous $R_{TT\_NOM}$ turn-on delay
$t_{AO_FAS}$	Asynchronous $R_{TT\_NOM}$ turn-off delay



NOTE:  $R_{TT\_PARK}$  = Enable,  $R_{TT\_NOM}$  = Enable, Write Preamble Set = 2  $t_{CK}$  and DLL = ON, CA parity is used.

**Figure 53. MRS w/ per DRAM addressability (PDA) issuing before MRS**

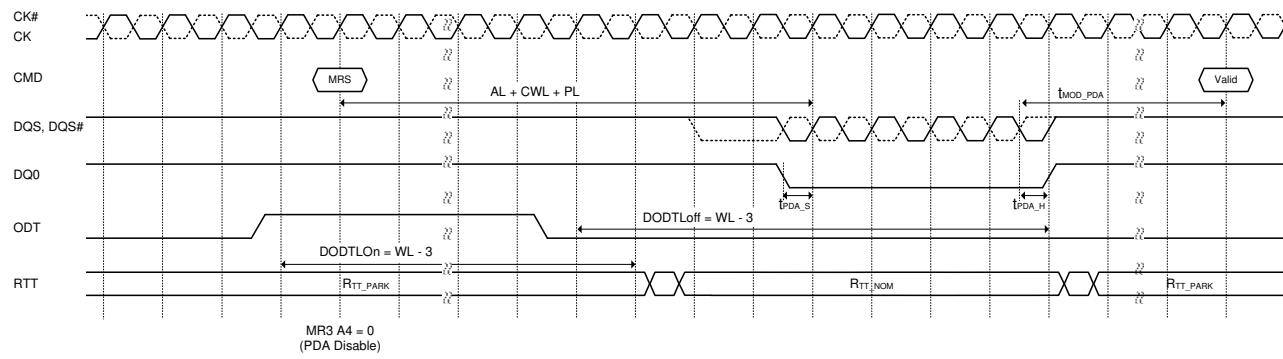


Figure 54. MRS w/ per DRAM addressability (PDA) Exit

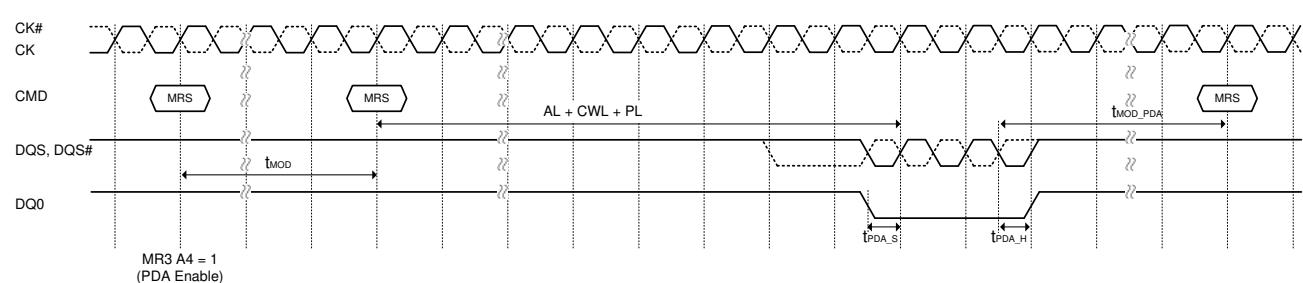


Figure 55. PDA using Burst Chop 4

Since PDA mode may be used to program optimal  $V_{REF}$  for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges.

This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

## Command Address Parity (CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register (MR5, A2:A0) when C/A Parity is enabled (PL: Parity Latency) and is applied to commands that are latched via the rising edge of CK when CS# is low. The command is held for the time of the Parity Latency before it is executed inside the device. This means that issuing timing of internal command is determined with PL. When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers ACT#, RAS#/A16, CAS#/A15, WE#/A14 and the address bus including bank address and bank group bits. The control signals CKE, ODT and CS# are not included. (e.g., for a 4 Gbit x8 monolithic device, parity is computed across BG0, BA1, BA0, A16/RAS#, A15/CAS#, A14/WE#, A13-A0 and ACT#). (The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even.

If a DRAM detects a C/A parity error in any command as qualified by CS# then it must perform the following steps:

- Ignore the erroneous command. Commands in max NnCK window (tPAR\_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a Read command in this NnCK window is not executed, the DRAM does not activate DQS outputs.
- Log the error by storing the erroneous command and address bits in the error log.
- Set the Parity Error Status bit in the mode register to 1. The Parity Error Status bit must be set before the ALERT# signal is released by the DRAM (i.e. tPAR\_ALERT\_ON + tPAR\_ALERT\_PW(min)).
- Assert the ALERT# signal to the host (ALERT# is active low) within tPAR\_ALERT\_ON time.
- Wait for all in-progress commands to complete. These commands were received tPAR\_UNKOWN before the erroneous command. If a parity error occurs on a command issued between the tXS\_Fast and tXS window after self-refresh exit then the DRAM may delay the de-assertion of ALERT# signal as a result of any internal ongoing refresh.
- Wait for tRAS\_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR\_ALERT\_ON + tPAR\_ALERT\_PW).
- After tPAR\_ALERT\_PW\_min has been satisfied, the DRAM may de-assert ALERT#.
- After the device has returned to a known pre-charged state it may de-assert ALERT#.
- After (tPAR\_ALERT\_ON + tPAR\_ALERT\_PW), the device is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a zero. (The DRAM will execute any erroneous commands until the bit is cleared).
- It is possible that the device might have ignored a refresh command during the (tPAR\_ALERT\_ON + tPAR\_ALERT\_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.
- The Parity Error Status bit may be read any time after (tPAR\_ALERT\_ON + tPAR\_ALERT\_PW) to determine which DRAM had the error. The device maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to zero.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The device controller can only program the Parity Error Status bit to zero. If the DRAM controller illegally attempts to write a '1' to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

DDR4 SDRAM supports MR bit for Persistent Parity Error Mode. This mode is enabled by setting MR5 A[9] = 1 and when it is enabled, DRAM resumes checking CA Parity after the ALERT# is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the error log in MPR page 1 should be treated as 'Don't Care'. In Persistent Parity Error Mode the ALERT# pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR\_ALERT\_PW. The controller must issue Deselect commands once it detects the ALERT# signal, this response time is defined as tPAR\_ALERT\_RSP. The following figure captures the flow of events on the C/A bus and the ALERT# signal.

**Table 28. Mode Registers for C/A Parity**

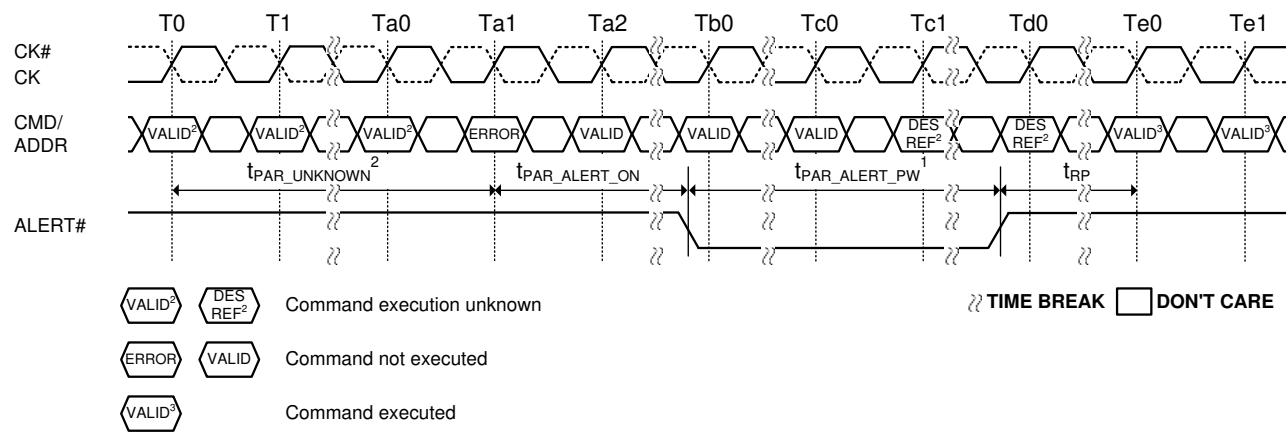
C/A Parity Latency MR5[2:0]*	Speed bins	C/A Parity Error Status MR5[4]	Errant C/A Frame
000 = Disabled	-	MR5[4] 0 = Clear MR5[4] 1 = Error	ACT#, BG0, BA0, BA1, PAR, A16/RAS#, A15/CAS#, A14/WE#, A13:A0
001= 4 Clocks	1600,1866,2133		
010= 5 Clocks	2400,2666		
011= 6 Clocks	2999,3200		
100= 8 Clocks	RFU		

Note 1. Parity Latency is applied to all commands.

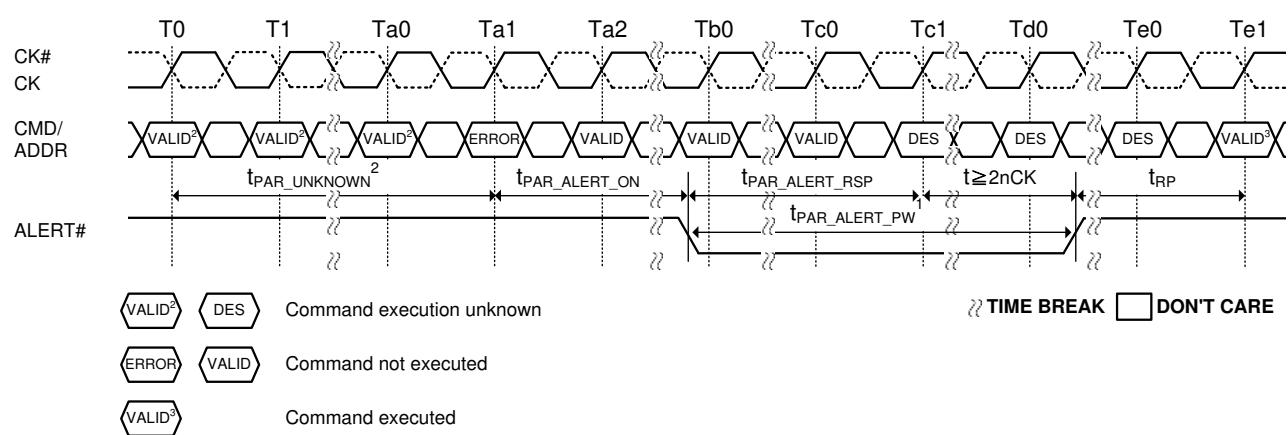
Note 2. Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL= 4 to PL= 5 is not allowed.

Correct sequence is PL= 4 to disabled to PL= 5.

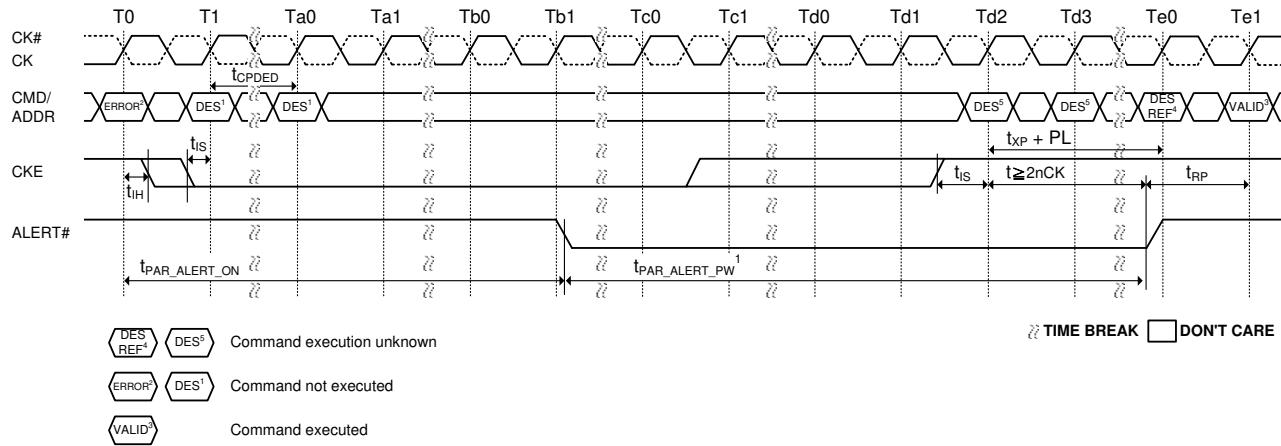
Note 3. Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.



**Figure 56. Normal CA Parity Error Checking Operation**



**Figure 57. Persistent CA Parity Error Checking Operation**



NOTE 1. Deselect command only allowed.

NOTE 2. Error could be Precharge or Activate.

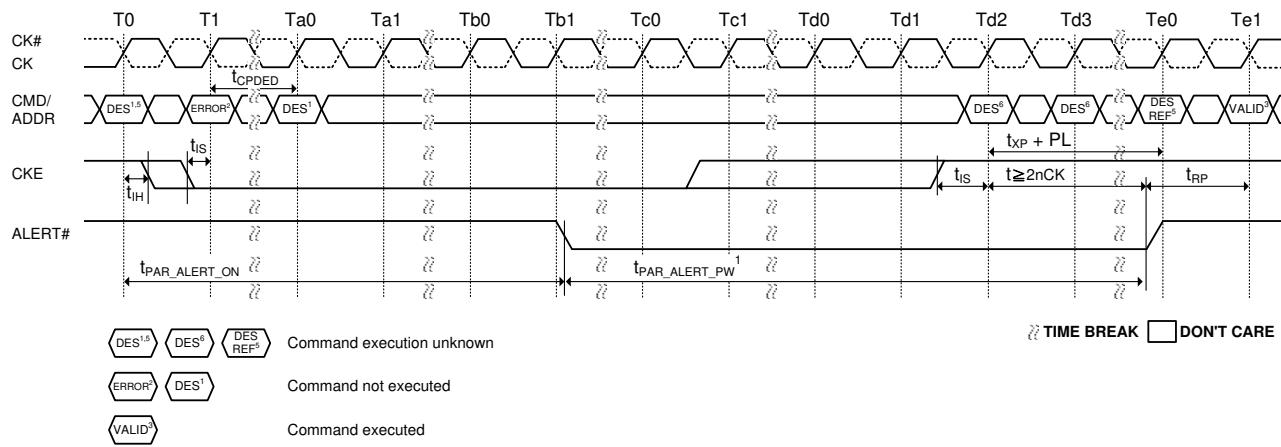
NOTE 3. Normal operation with parity latency (CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.

NOTE 4. Command execution is unknown the corresponding DRAM internal state change may or may not occur.

The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 5. Deselect command only allowed CKE may go high prior to Td2 as long as DES commands are issued.

**Figure 58. CA Parity Error Checking - PDE/PDX**



NOTE 1. Deselect command only allowed.

NOTE 2. SelfRefresh command error. DRAM masks the intended SRE command enters Precharge Power Down.

NOTE 3. Normal operation with parity latency(CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.  
NOTE 4. Control register initial value is 0x00000000. It is recommended to write 0x00000000 into CA Parity Persistent Error Mode register.

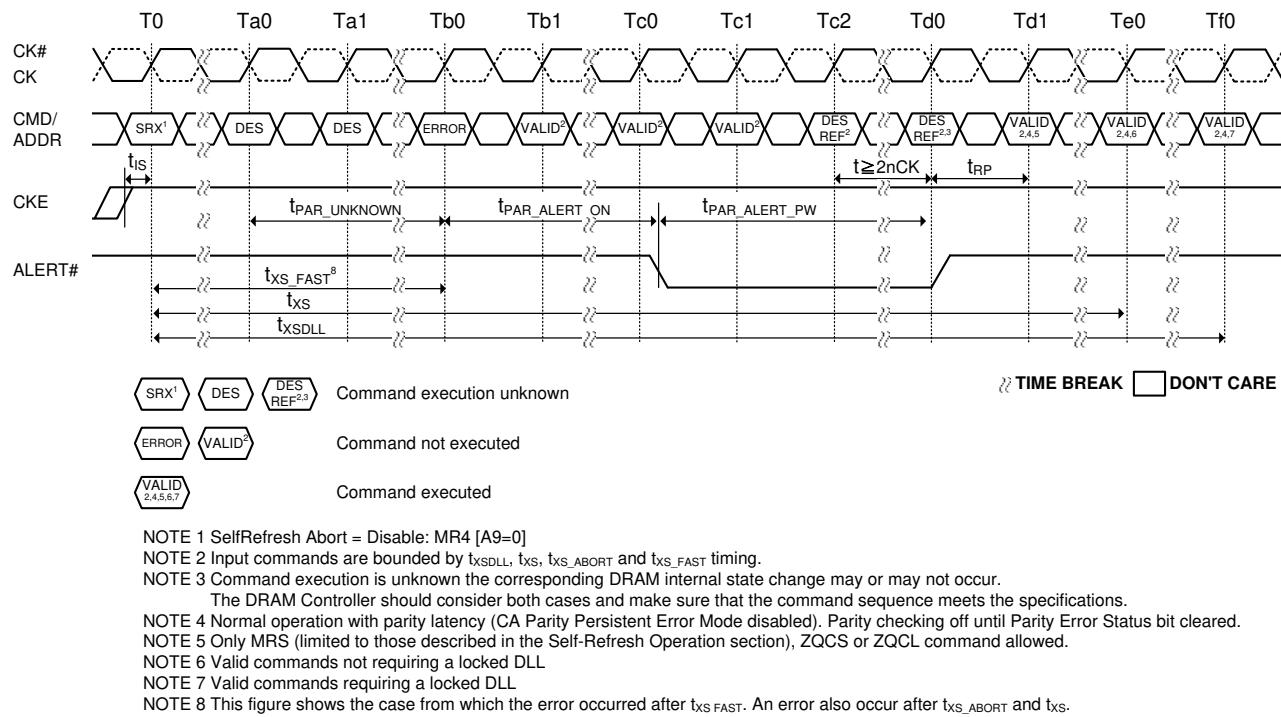
NOTE 4. Controller can not disable clock until it has been able to have detected a possible C/A Parity error.

NOTE 5. Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should be designed so that the command sequence is not corrupted.

NOTE 6: The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications. Preload command only allowed CKE may go high prior to Tc2 as long as PES commands are issued.

NOTE 6. Deselect command only allowed CKE may go high prior to Tc2 as long as DES commands are issued

**Figure 59. CA Parity Error Checking - SRE Attempt**



**Figure 60. CA Parity Error Checking - SRX**

## Command/Address parity entry and exit timings

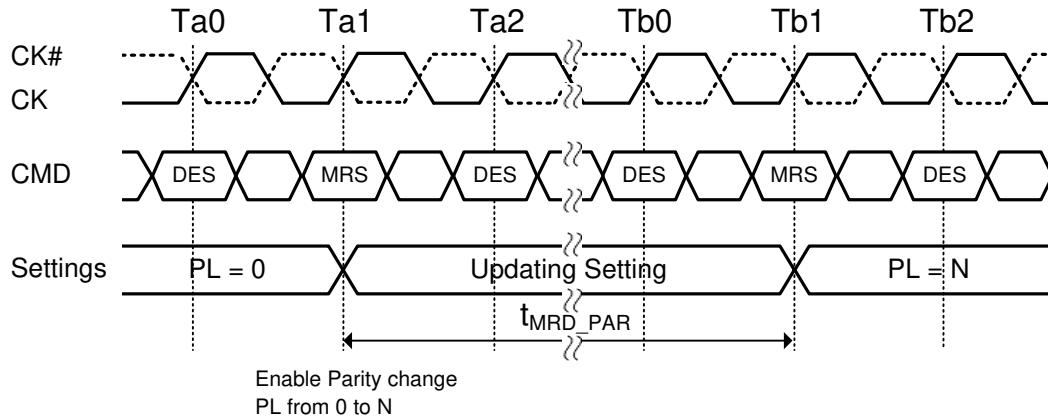
When in CA Parity mode, including entering and exiting CA Parity mode, users must wait  $t_{MRD\_PAR}$  before issuing another MRS command, and wait  $t_{MOD\_PAR}$  before any other commands.

$$t_{MOD\_PAR} = t_{MOD} + PL$$

$$t_{\text{MRD PAR}} = t_{\text{MOD}} + PL$$

For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.

For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.

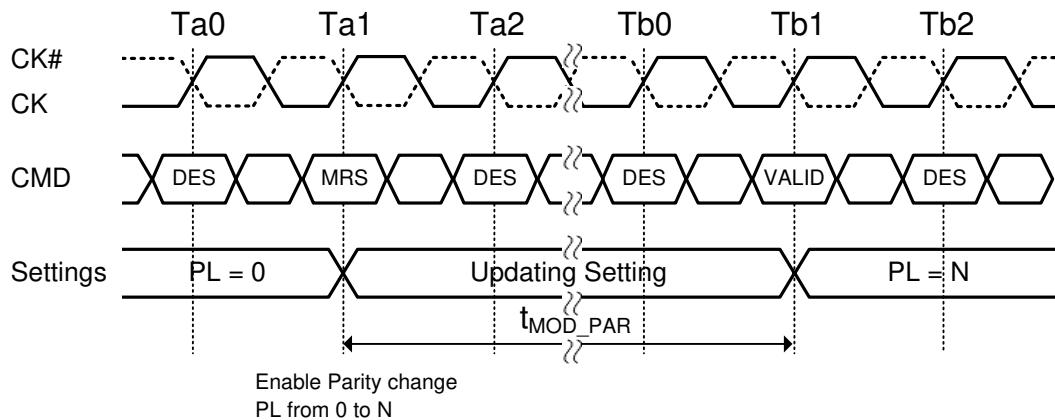


NOTE 1.  $t_{MRD\_PAR} = t_{MOD} + N$ ; where N is the programmed parity latency with the MRS command entering CA parity mode.

NOTE 2. Parity check is not available at Ta1 of MRS command due to PL=0 being valid.

NOTE 3. In case parity error happens at Tb1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is 'N[nCK] + 6[ns]'.

**Figure 61. Parity entry timing example -  $t_{MBD\_PAR}$**

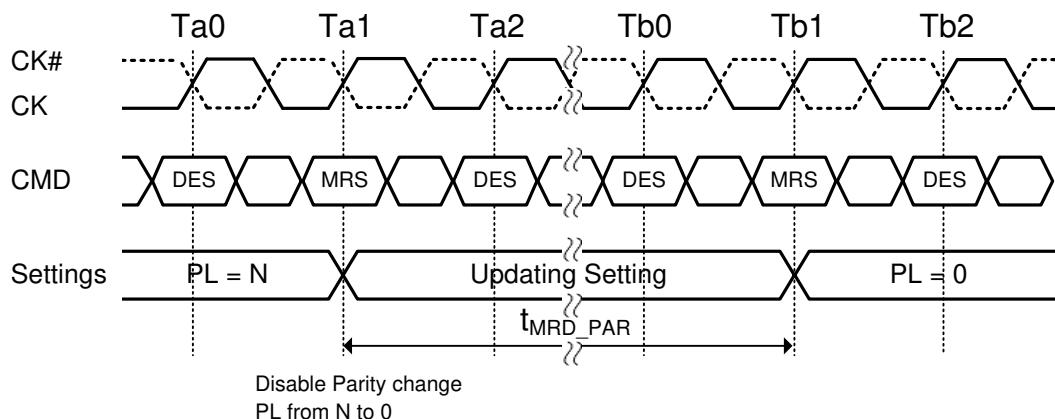


NOTE 1.  $t_{MOD\_PAR} = t_{MOD} + N$ ; where  $N$  is the programmed parity latency with the MRS command entering CA parity mode.

NOTE 2. Parity check is not available at Ta1 of MRS command due to PL=0 being valid.

NOTE 3. In case parity error happens at Tb1 of VALID command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

Figure 62. Parity entry timing example -  $t_{MOD\_PAR}$

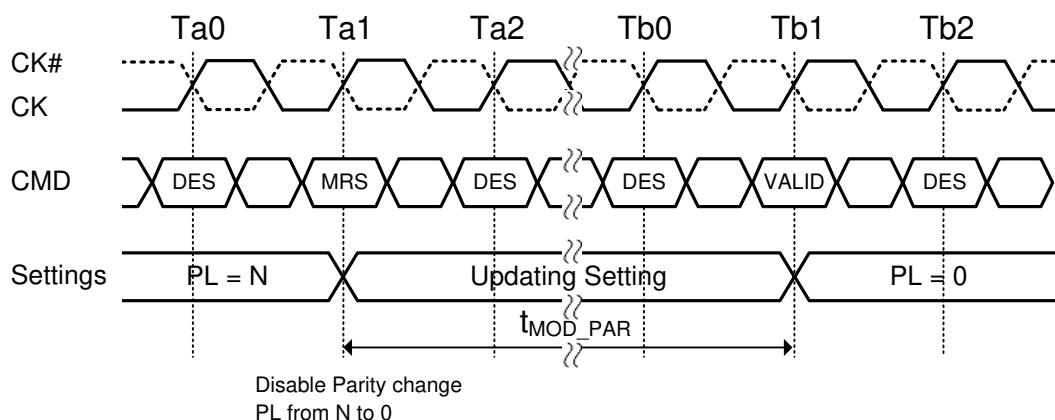


NOTE 1.  $t_{MRD\_PAR} = t_{MOD} + N$ ; where  $N$  is the programmed parity latency prior to the MRS command exiting CA parity mode.

NOTE 2. In case parity error happens at Ta1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

NOTE 3. Parity check is not available at Tb1 of MRS command due to disabling parity mode.

Figure 63. Parity exit timing example -  $t_{MRD\_PAR}$



NOTE 1.  $t_{MOD\_PAR} = t_{MOD} + N$ ; where  $N$  is the programmed parity latency prior to the MRS command exiting CA parity mode.

NOTE 2. In case parity error happens at Ta1 of MRS command,  $t_{PAR\_ALERT\_ON}$  is ' $N[nCK] + 6[ns]$ '.

NOTE 3. Parity check is not available at Tb1 of VALID command due to disabling parity mode.

Figure 64. Parity exit timing example -  $t_{MOD\_PAR}$

## Multipurpose Register

The Multipurpose Register (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3.

MPR mode enable and page selection is done with MRS commands. Data bus inversion (DBI) is not allowed during MPR Read operation. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and  $t_{RP}$  met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

Once the MPR access mode is enabled (MR3 A[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and Reset; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. The mode register location is specified with the Read command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode and Self Refresh command are not allowed during MPR enable mode.

No other command can be issued within  $t_{RFC}$  after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a Refresh command.

### MR3 Setting for the MPR Access Mode

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS#, RAS#/A16, CAS#/A15 and WE#/A14 low, ACT#, BA0 and BA1 high and BG0 low while controlling the states of the address pins. Refer to the MR3 definition table for more detail.

**Table 29. DRAM Address to MPR UI Translation**

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – Ax	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UIx	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

**Table 30. MPR Data Format**

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note	
MPR page0 (Training Pattern)											
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value)	
	01 = MPR1	0	0	1	1	0	0	1	1		
	10 = MPR2	0	0	0	0	1	1	1	1		
	11 = MPR3	0	0	0	0	0	0	0	0		
MPR page1 (CA Parity Error Log)											
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only	
	01 = MPR1	CAS#/A15	WE#/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]		
	10 = MPR2	PAR	ACT#	-	BG[0]	BA[1]	BA[0]	don't care	RAS#/A16		
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency <sup>*1</sup>			don't care	don't care	don't care		
MPR page2 (MRS Readout)											
BA1:BA0	00 = MPR0	hPPR	sPPR	R <sub>TT_WR</sub>	Temperature sensor <sup>*2</sup>			CRC Write Enable	R <sub>TT_WR</sub>	Read-only	
		-	-	MR2	-	-	MR2	MR2	MR2		
		-	-	A11	-	-	A12	A10	A9		
	01 = MPR1	V <sub>REFDQ</sub> Training range	V <sub>REFDQ</sub> Training Value						Geardown Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency				RFU	CAS Write Latency				
		MR0				-	MR2				
		A6	A5	A4	A2	-	A5	A4	A3		
	11 = MPR3	R <sub>TT_NOM</sub>			R <sub>TT_PARK</sub>			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A8	A8	A7	A6	A2	A1		
MPR page3 (RFU) <sup>*3</sup>											
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only	
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care		
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care		
	11 = MPR3	don't care	don't care	don't care	don't care	MAC	MAC	MAC	MAC		

Note 1. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

Note 2. MR bit for Temperature Sensor Readout

- MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.
- MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0 bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh ( > t <sub>REFI</sub> )
0	1	1X refresh rate(= t <sub>REFI</sub> )
1	0	2X refresh rate(1/2 x t <sub>REFI</sub> )
1	1	Reserved

Note 3. Restricted, except for MPR3 [3:0]

## MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR Read operation; the device will ignore the Read DBI enable setting in MR5 [A12] when in MPR mode. Read commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in MPR Data Format table. MPR page 0 can be rewritten via an MPR Write command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use  $t_{CCD\_S}$  or  $t_{CCD\_L}$  timing between Read commands.
- Reads (back-to-back) from Pages 1, 2, or 3 may not use  $t_{CCD\_S}$  timing between Read commands;  $t_{CCD\_L}$  must be used for timing between Read commands. The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).
  1. The DLL must be locked if enabled.
  2. Precharge all; wait until  $t_{RP}$  is satisfied.
  3. MRS command to MR3 A[2] = 1 (Enable MPR data flow), MR3 A[12:11] = MPR read format, and MR3 A[1:0] MPR page.
    - a. MR3 A[12:11] MPR read format:
      - 1) 00 = Serial read format
      - 2) 01 = Parallel read format
      - 3) 10 = Staggered read format
      - 4) 11 = RFU
    - b. MR3[1:0] MPR page:
      - 1) 00 = MPR Page 0
      - 2) 01 = MPR Page 1
      - 3) 10 = MPR Page 2
      - 4) 11 = MPR Page 3
  4.  $t_{MRD}$  and  $t_{MOD}$  must be satisfied.
  5. Redirect all subsequent Read commands to specific MPRx location.
  6. Issue RD or RDA command.
    - a. BA1 and BA0 indicate MPRx location:
      - 1) 00 = MPR0
      - 2) 01 = MPR1
      - 3) 10 = MPR2
      - 4) 11 = MPR3
    - b. A12/BC# = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
      - 1) If BL = 8 and MR0 A[1:0] = 01, A12/BC# must be set to 1 during MPR Read commands.
    - c. A2 = burst-type dependant:
      - 1) BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      - 2) BL8: A2 = 1 not allowed
      - 3) BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      - 4) BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
    - d. A[1:0] = 00, data burst is fixed nibble start at 00.
    - e. Remaining address inputs, including A10, BG0 are "Don't Care."
  7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3 A[12:10] and MR3 A[1:0].
  8. Steps 5 through 7 may be repeated to read additional MPRx locations.
  9. After the last MPRx Read burst,  $t_{MPRR}$  must be satisfied prior to exiting.
  10. Issue MRS command to exit MPR mode; MR3 A[2] = 0.
  11. After the  $t_{MOD}$  sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

## MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MRx, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings). Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

**Table 31. MPR Readout Serial Format**

x4 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
x8 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
x16 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

## **MPR Readout Parallel Format**

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). The x16 configuration, the same pattern is repeated on both the upper and lower bytes.

**Table 32. MPR Readout Parallel Format**

x4 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
x8 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
x16 Device								
Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

**MPR Readout Staggered Format**

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations. For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on, as shown below. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on. Examples of different starting locations are also shown.

**Table 33. MPR Readout Staggered Format, x4**

x4 Read MPR0 Command		x4 Read MPR1 Command		x4 Read MPR2 Command		x4 Read MPR3 Command	
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

**Table 34. MPR Readout Staggered Format, x4 – Consecutive Reads**

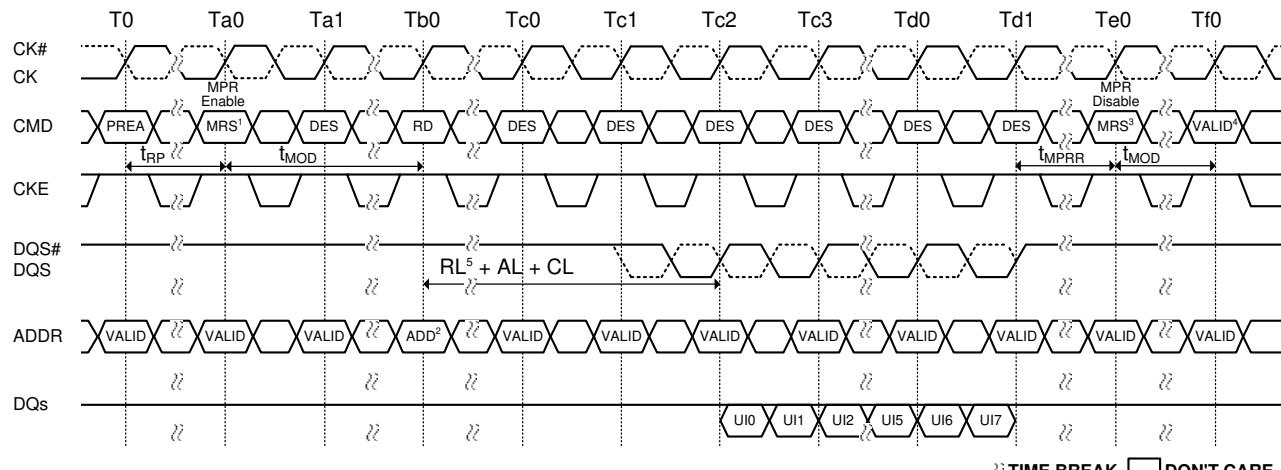
Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

**Table 35. MPR Readout Staggered Format, x8 and x16**

x8 Read MPR0 Command		x16 Read MPR0 Command			
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

## MPR Read Waveforms



NOTE 1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

- Redirect all subsequent read and writes to MPR locations

NOTE 2. Address setting

- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)

- A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

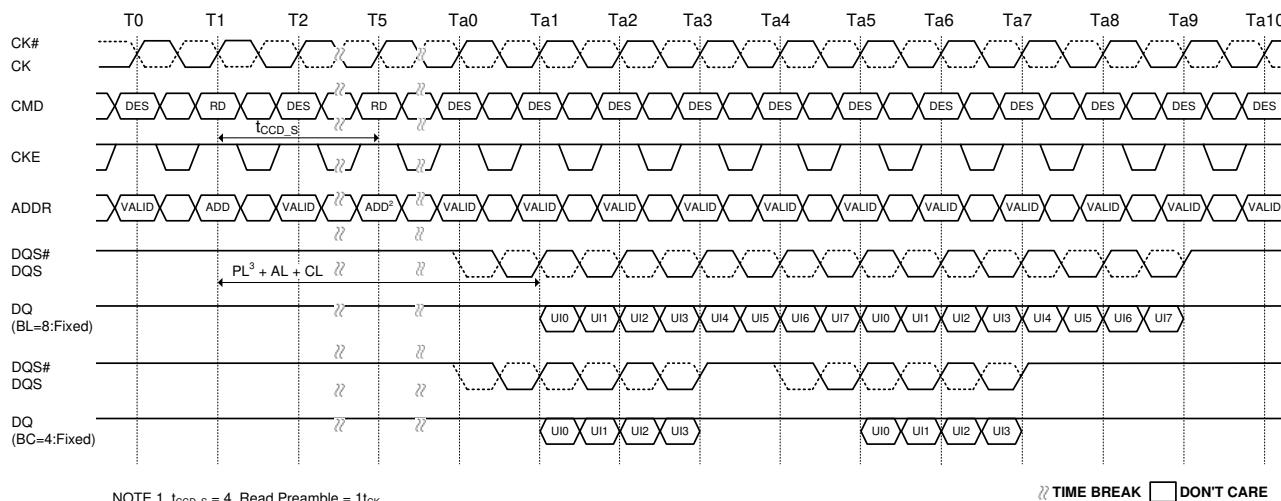
- A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00" or "10", and must be '1'b when MR0 A[1:0] = "01"

NOTE 3. Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)

NOTE 4. Continue with regular DRAM command.

NOTE 5. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 65. MPR Read Timing



NOTE 1.  $t_{CCD\_S} = 4$ , Read Preamble =  $1t_{CK}$

NOTE 2. Address setting

- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)

- A[2] = "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

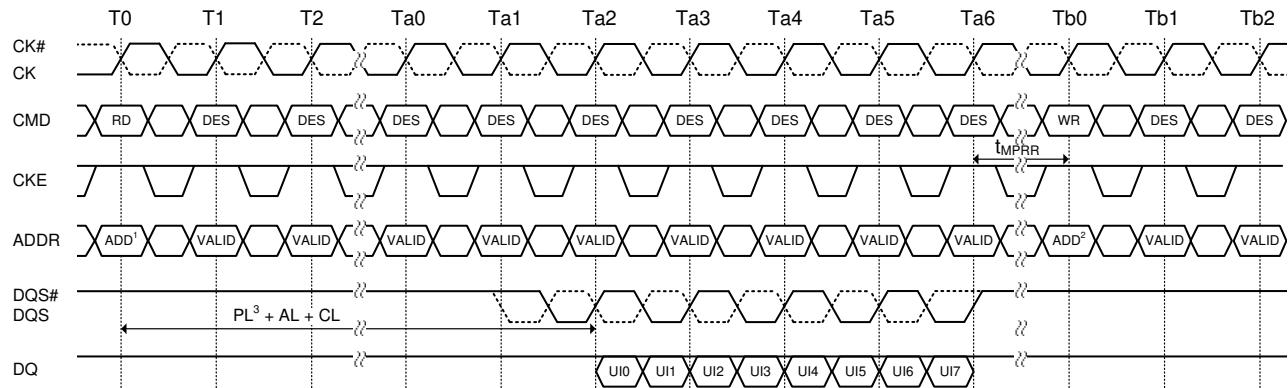
(For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00" or "10", and must be '1'b when MR0 A[1:0] = "01"

NOTE 3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 66. MPR Back to Back Read Timing



NOTE 1. Address setting

- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG0. A12 is don't care when MR0 A[1:0] = "00", and must be '1'b when MR0 A[1:0] = "01"

NOTE 2. Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 67. MPR Read to Write Timing

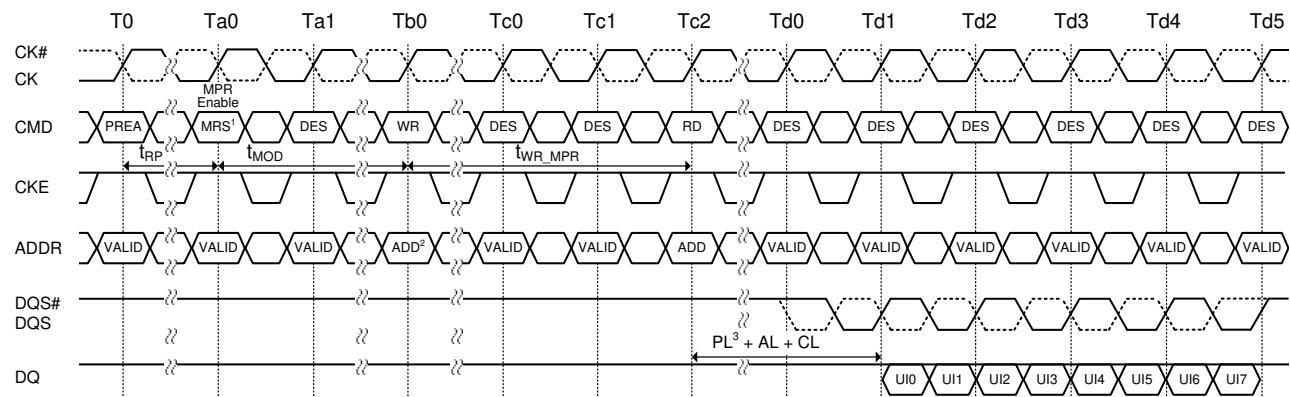
## **MPR Writes**

MPR access mode allows 8-bit writes to the MPR Page 0 using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR Write operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked if enabled.
2. Precharge all; wait until  $t_{RP}$  is satisfied.
3. MRS command to MR3 A[2] = 1 (enable MPR data flow) and MR3 A[1:0] = 00 (MPR Page 0); writes to 01, 10, and 11 are not allowed.
4.  $t_{MRD}$  and  $t_{MOD}$  must be satisfied.
5. Redirect all subsequent Write commands to specific MPRx location.
6. Issue WR or WRA command:
  - a. BA1 and BA0 indicate MPRx location
    - 1) 00 = MPR0
    - 2) 01 = MPR1
    - 3) 10 = MPR2
    - 4) 11 = MPR3
  - b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
  - c. Remaining address inputs, including A10, and BG0 are "Don't Care"
7.  $t_{WR\_MPR}$  must be satisfied to complete MPR Write.
8. Steps 5 through 7 may be repeated to write additional MPRx locations.
9. After the last MPRx write,  $t_{MPRR}$  must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3 A[2] = 0.
11. When the  $t_{MOD}$  sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

## MPR Write Waveforms



NOTE 1. Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

NOTE 2. Address setting - BA1 and BA0 indicate the MPR location

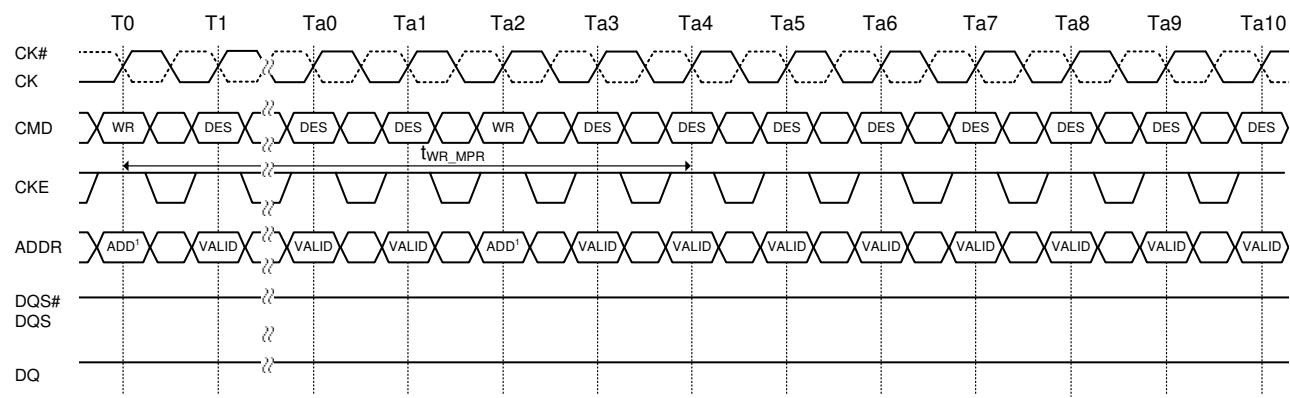
- A [7:0] = data for MPR

- A10 and other address pins are don't care.

NOTE 3. PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

TIME BREAK DON'T CARE

Figure 68. MPR Write Timing and Write to Read Timing



NOTE 1. Address setting

- BA1 and BA0 indicate the MPR location

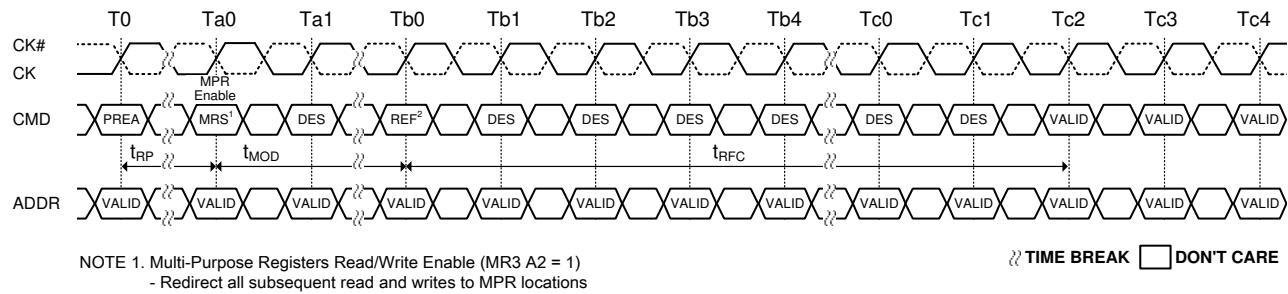
- A [7:0] = data for MPR

- A10 and other address pins are don't care.

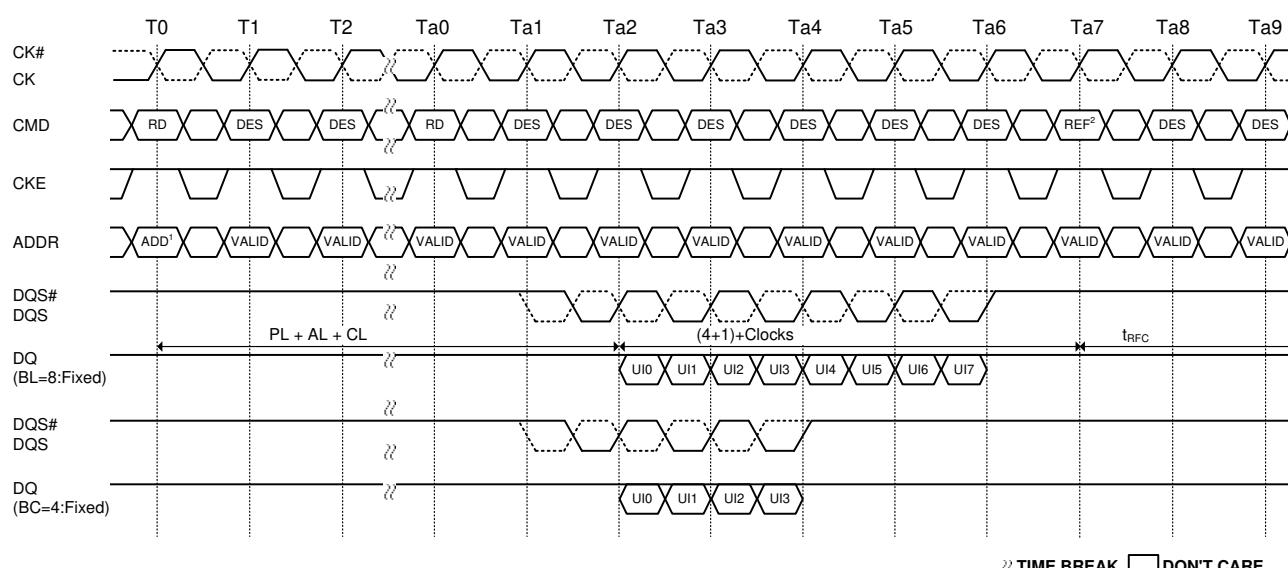
TIME BREAK DON'T CARE

Figure 69. MPR Back to Back Write Timing

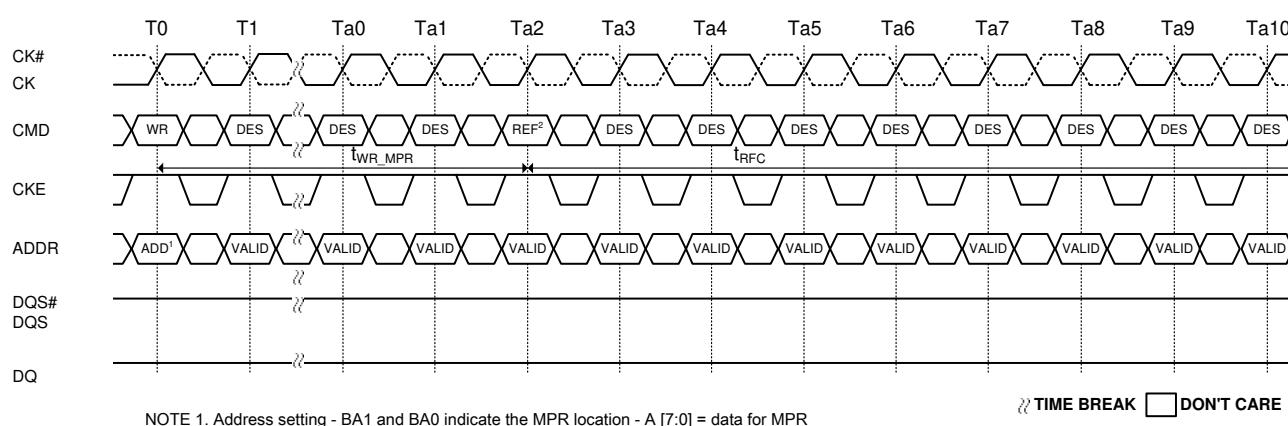
## MPR Refresh Waveforms



**Figure 70. Refresh Command Timing**

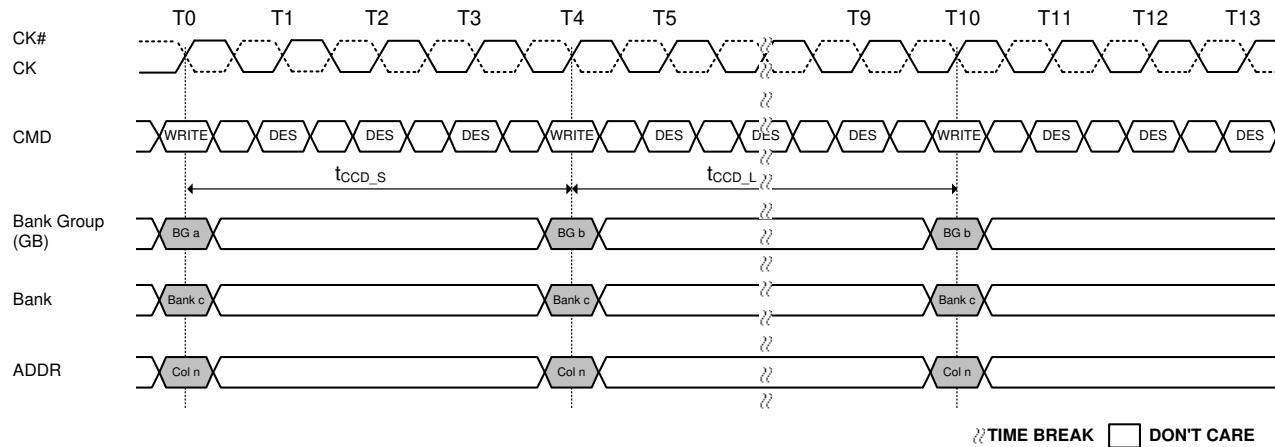


**Figure 71. Read to Refresh Command Timing**



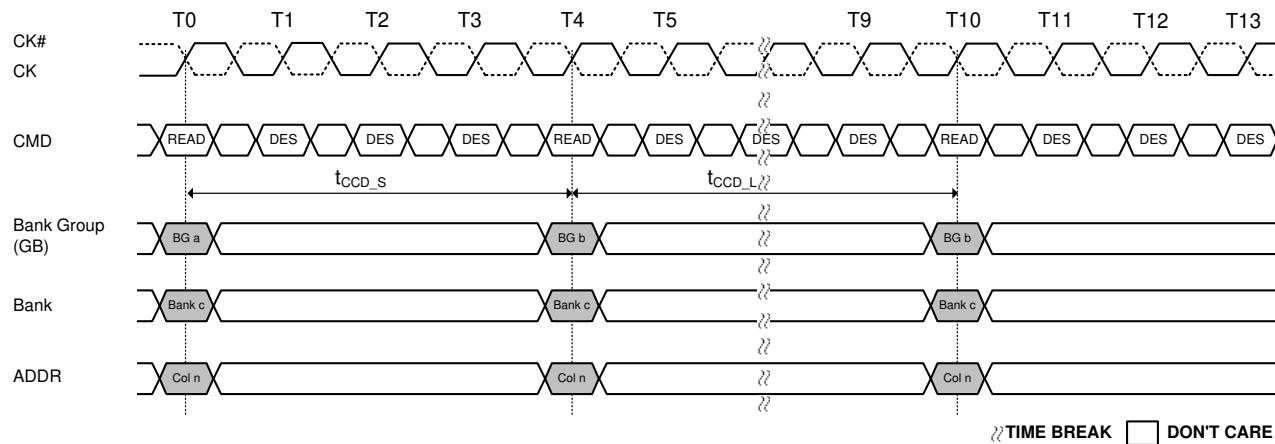
**Figure 72. Write to Refresh Command Timing**

## DDR4 Key Core Timing



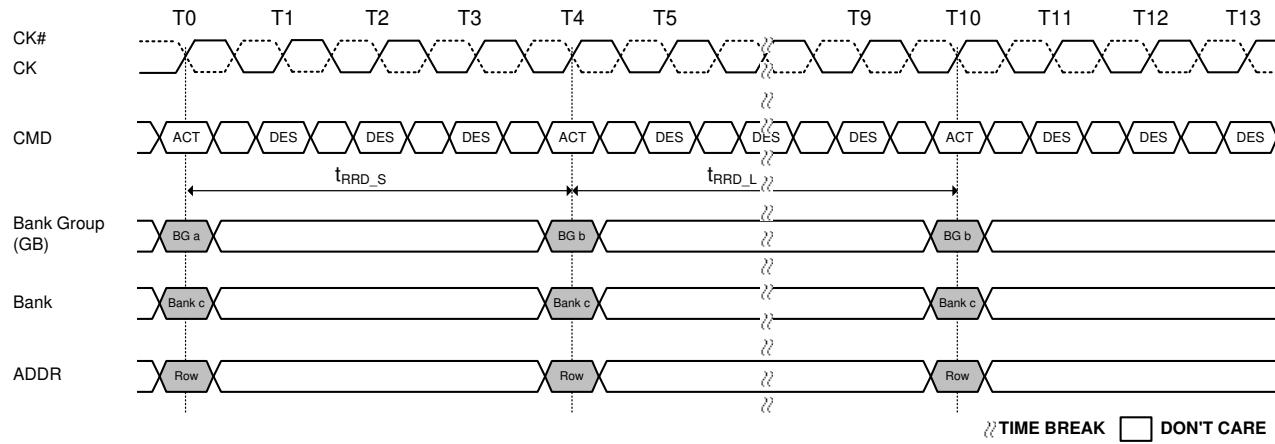
NOTE 1.  $t_{CCD\_S}$  : CAS#-to-CAS# delay (short) : Applies to consecutive CAS# to different Bank Group (i.e., T0 to T4).  
 NOTE 2.  $t_{CCD\_L}$  : CAS#-to-CAS# delay (long) : Applies to consecutive CAS# to the same Bank Group (i.e., T4 to T10).

Figure 73.  $t_{CCD}$  Timing (WRITE to WRITE Example)



NOTE 1.  $t_{CCD\_S}$  : CAS#-to-CAS# delay (short) : Applies to consecutive CAS# to different Bank Group (i.e., T0 to T4)  
 NOTE 2.  $t_{CCD\_L}$  : CAS#-to-CAS# delay (long) : Applies to consecutive CAS# to the same Bank Group (i.e., T4 to T10)

Figure 74.  $t_{CCD}$  Timing (READ to READ Example)



NOTE 1.  $t_{RRD\_S}$  : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e., T0 to T4).

NOTE 2.  $t_{RRD\_L}$  : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group (i.e., T4 to T10).

Figure 75.  $t_{RRD}$  Timing

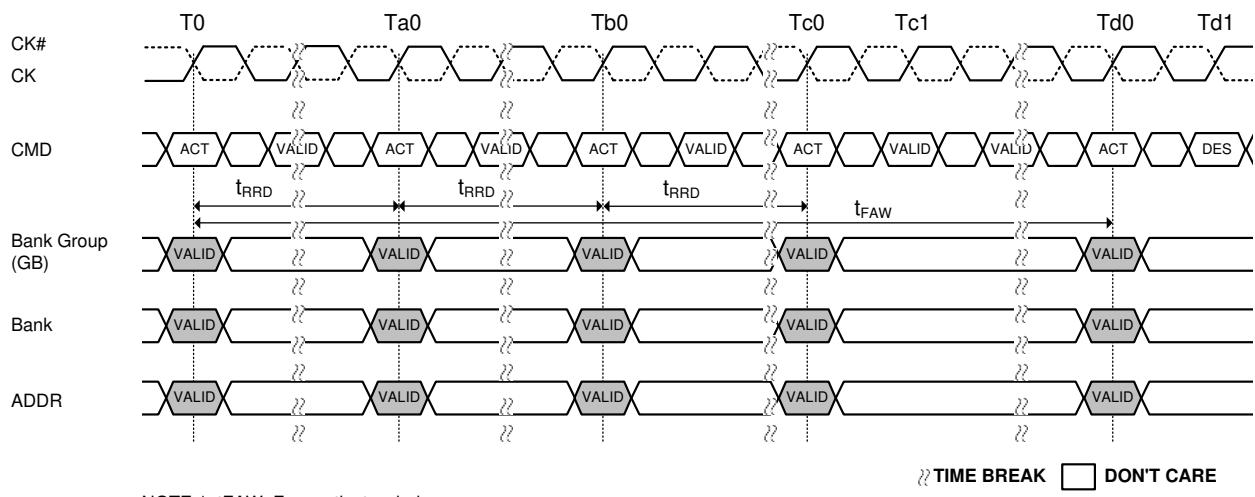


Figure 76. t<sub>FAW</sub> Timing

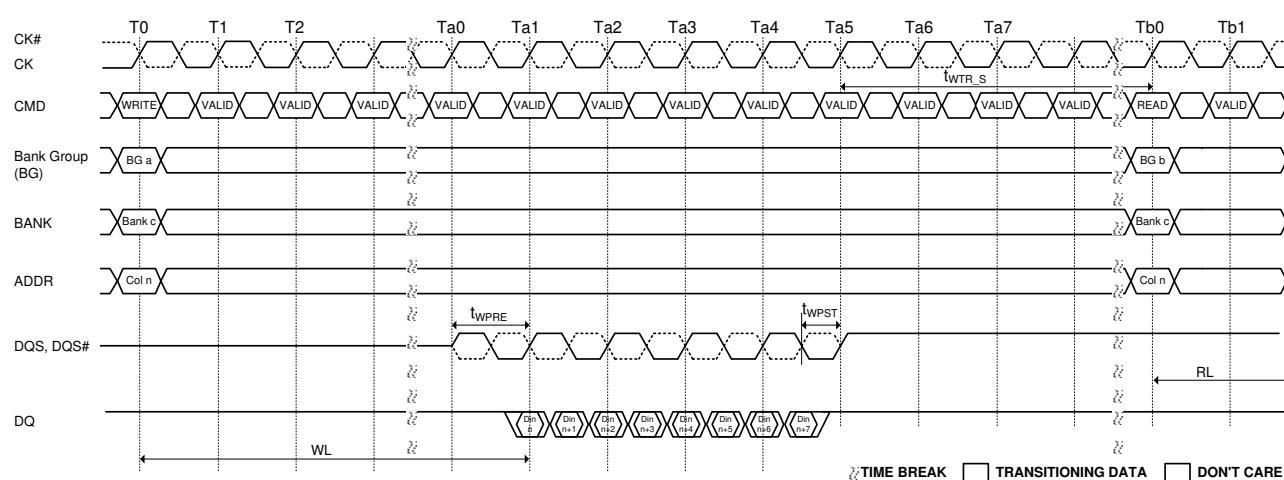


Figure 77. t<sub>WTR\_S</sub> Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)

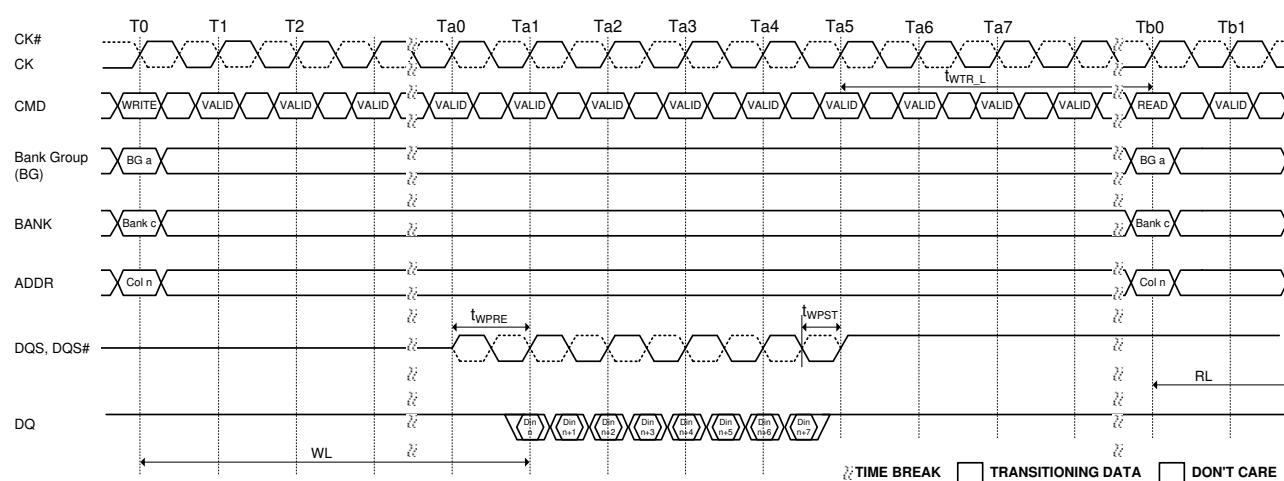


Figure 78. t<sub>WTR\_L</sub> Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)

## Programmable Preamble

The DQS preamble can be programmed to one or the other of 1  $t_{CK}$  and 2  $t_{CK}$  preamble; selectable via MRS (MR4 A[12:11]). The 1  $t_{CK}$  preamble applies to all speed-Grade and The 2  $t_{CK}$  preamble is valid for DDR4-2666 /3200 speed-Grade.

### Write Preamble

DDR4 supports a programmable write preamble. The 1  $t_{CK}$  or 2  $t_{CK}$  Write Preamble is selected via MR4 A[12]. Write preamble modes of 1  $t_{CK}$  and 2  $t_{CK}$  are shown below.

When operating in 2  $t_{CK}$  Write preamble mode in MR2 CWL (CAS Write Latency), CWL of 1<sup>st</sup> Set needs to be incremented by 2 nCK and CWL of 2<sup>nd</sup> Set does not need increment of it.  $t_{WTR}$  must be increased by one clock cycle from the  $t_{WTR}$  required in the applicable speed bin table. WR must be programmed to a value one or two clock cycle(s), depending on available settings, greater than the WR setting required per the applicable speed bin table.

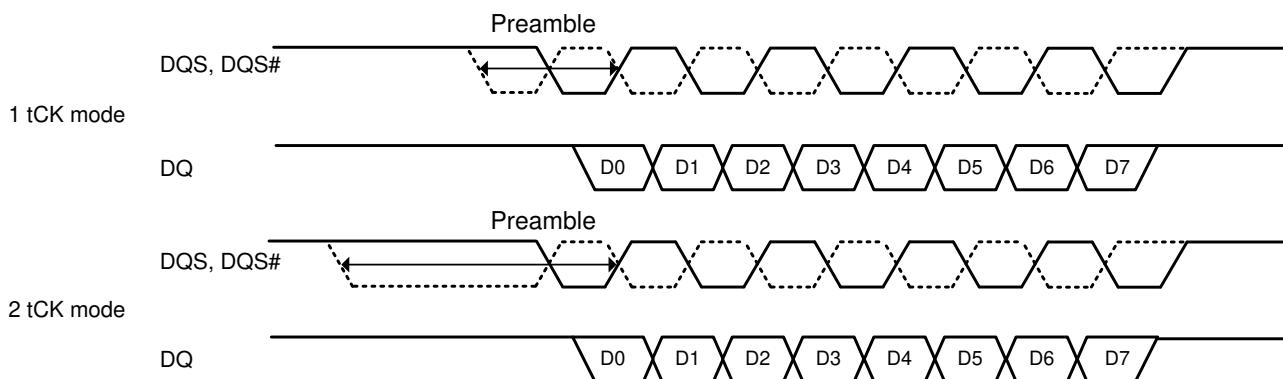


Figure 79. 1 $t_{CK}$  vs. 2 $t_{CK}$  WRITE Preamble Mode

The timing diagrams contained in  $t_{CCD}=4$  (AL=PL=0),  $t_{CCD}=5$  and  $t_{CCD}=6$  (AL=PL=0) illustrate 1 and 2  $t_{CK}$  preamble scenarios for consecutive write commands with  $t_{CCD}$  timing of 4, 5 and 6 nCK, respectively. Setting  $t_{CCD}$  to 5nCK is not allowed in 2  $t_{CK}$  preamble mode.

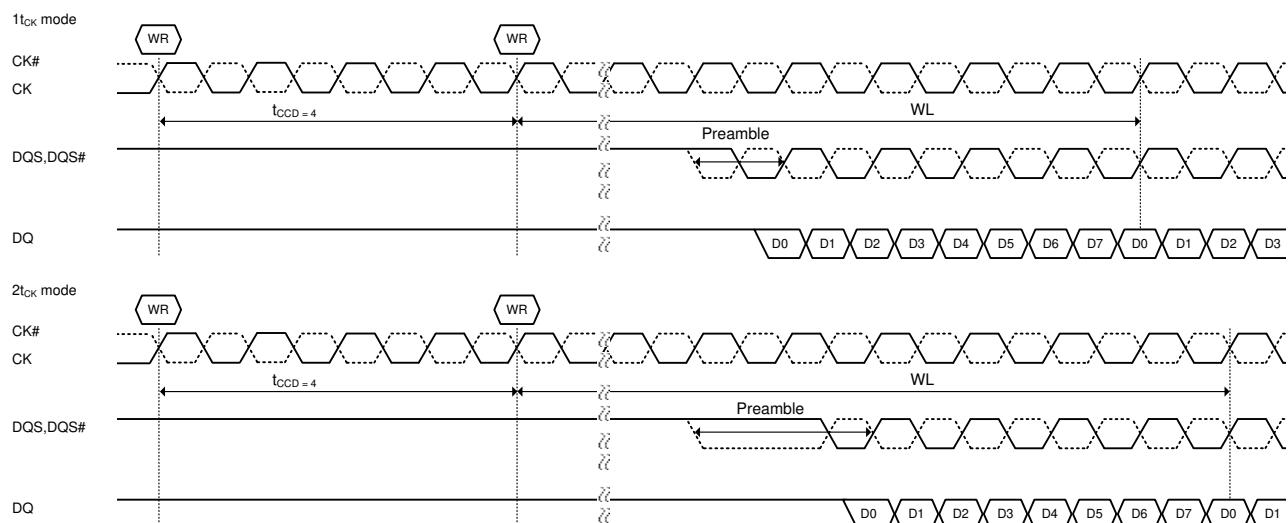
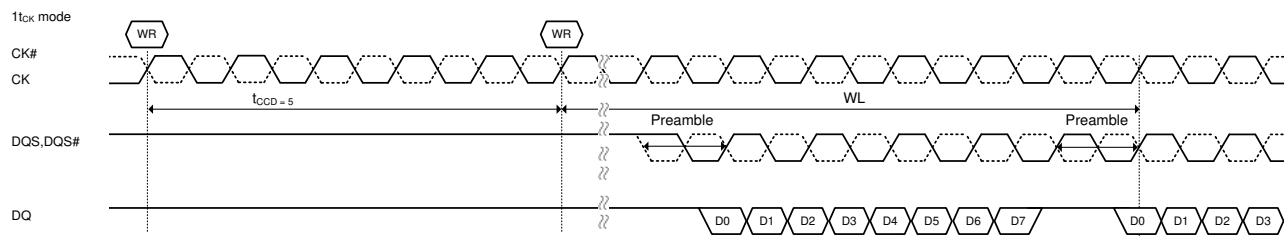
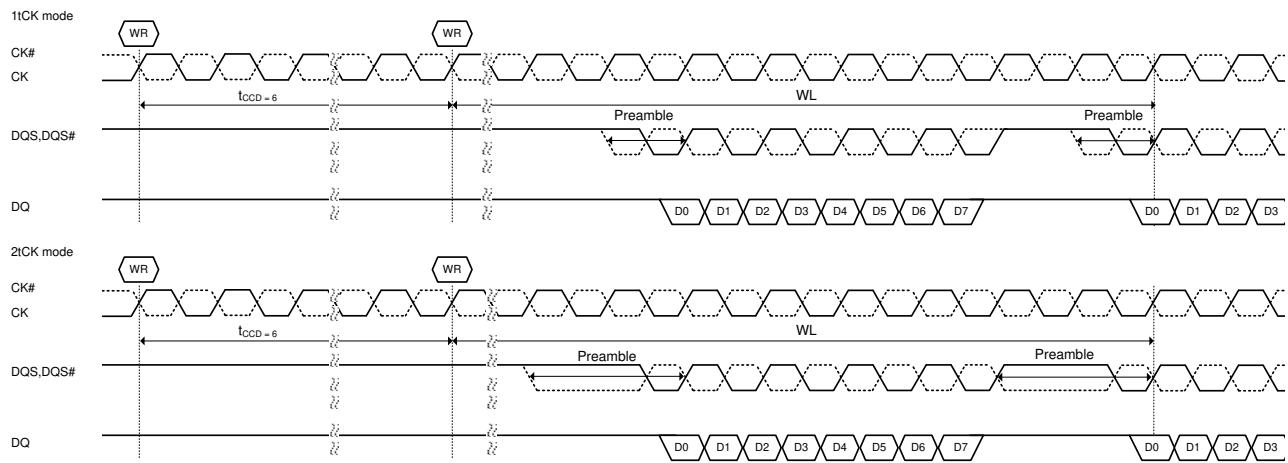


Figure 80.  $t_{CCD}=4$  (AL=PL=0)



2tCK mode:  $t_{CCD}=5$  is not allowed in 2tCK mode

**Figure 81.  $t_{CCD}=5$  ( $AL=PL=0$ )**



**Figure 82.  $t_{CCD}=6$  ( $AL=PL=0$ )**

## Read Preamble

DDR4 supports a programmable read preamble. The  $1 t_{CK}$  and  $2 t_{CK}$  Read preamble is selected via MR4 A[11]. Read preamble modes of  $1 t_{CK}$  and  $2 t_{CK}$  are shown as follows:

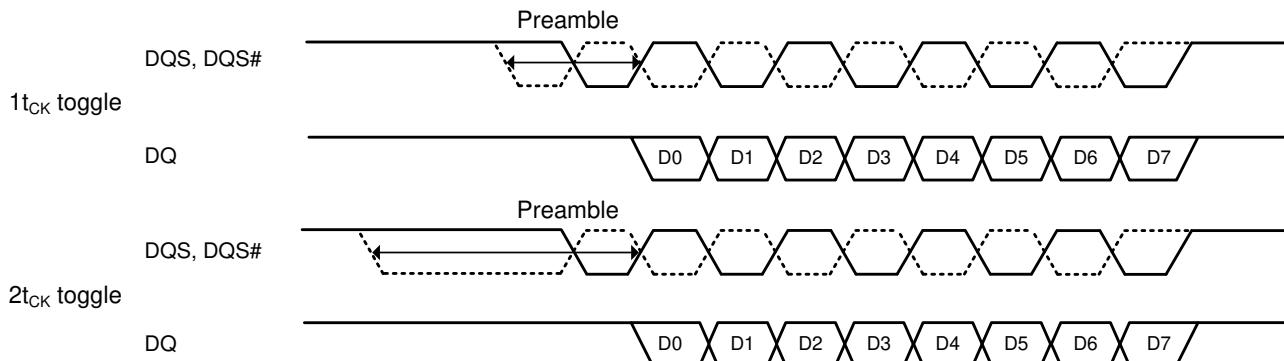
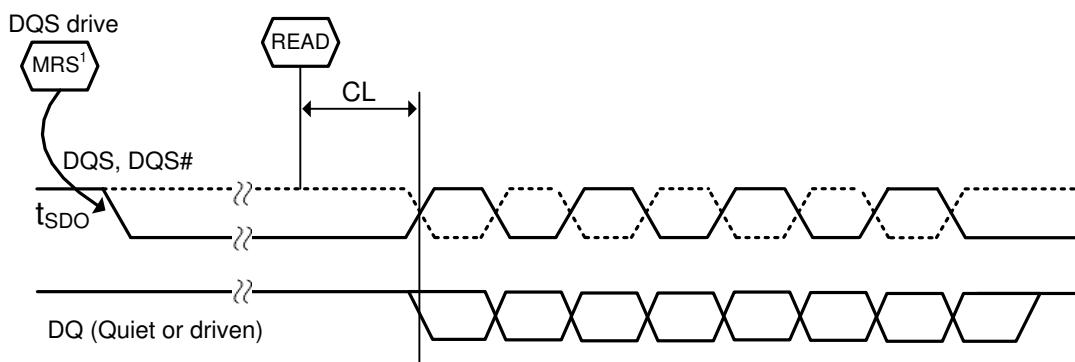


Figure 83.  $1t_{CK}$  vs.  $2t_{CK}$  READ Preamble Mode

## Read Preamble Training

DDR4 supports Read preamble training via MPR reads; that is, Read preamble training is allowed only when the DRAM is in the MPR access mode. The Read preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers. Read preamble training is entered via an MRS command (MR4 A[10] = 1 is enabled and MR4 A[10] = 0 is disabled). After the MRS command is issued to enable Read preamble training, the DRAM DQS signals are driven to a valid level by the time  $t_{SDO}$  is satisfied. During this time, the data bus DQ signals are held quiet, i.e. driven high. The DQS signal remains driven low and the DQS# signal remains driven high until an MPR Page0 Read command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit Read preamble training mode, an MRS command must be issued, MR4 A[10] = 0.



NOTE 1. Read Preamble Training mode is enabled by MR4 A10 = [1]

Figure 84. READ Preamble Training

Table 36. AC Timing Table

Symbol	Parameter	Min.	Max.	Unit
$t_{SDO}$	Delay from MRS Command to Data Strobe Drive Out	-	$t_{MOD} + 9\text{ns}$	

## Postamble

### Read Postamble

Whether the 1  $t_{CK}$  or 2  $t_{CK}$  Read Preamble Mode is selected, the Read Postamble remains the same at 1/2  $t_{CK}$ . DDR4 will support a fixed read postamble.

Read postamble of nominal 0.5  $t_{CK}$  for preamble modes 1,2  $t_{CK}$  are shown below:

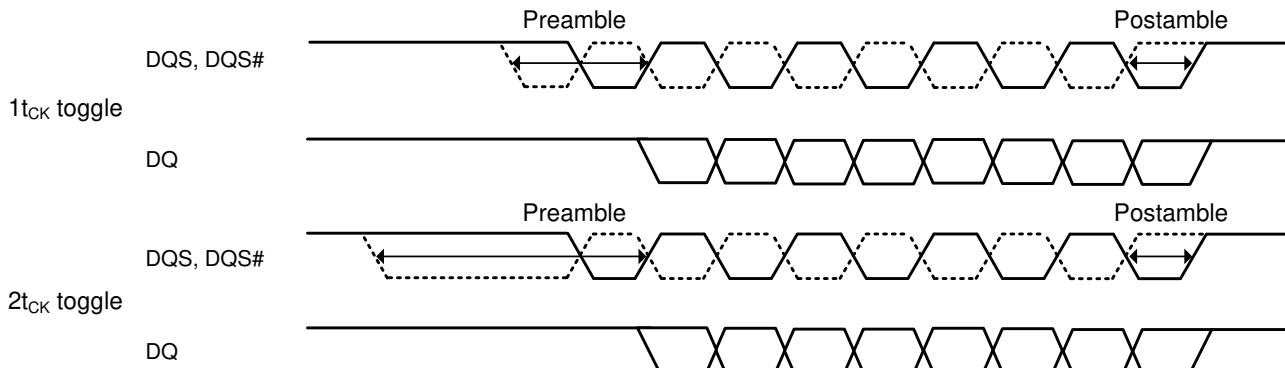


Figure 85. READ Postamble

### Write Postamble

Whether the 1  $t_{CK}$  or 2  $t_{CK}$  Write preamble mode is selected, the Write postamble remains the same at 1/2  $t_{CK}$ . DDR4 will support a fixed Write postamble.

Write postamble nominal is 0.5  $t_{CK}$  for preamble modes 1,2  $t_{CK}$  are shown below:

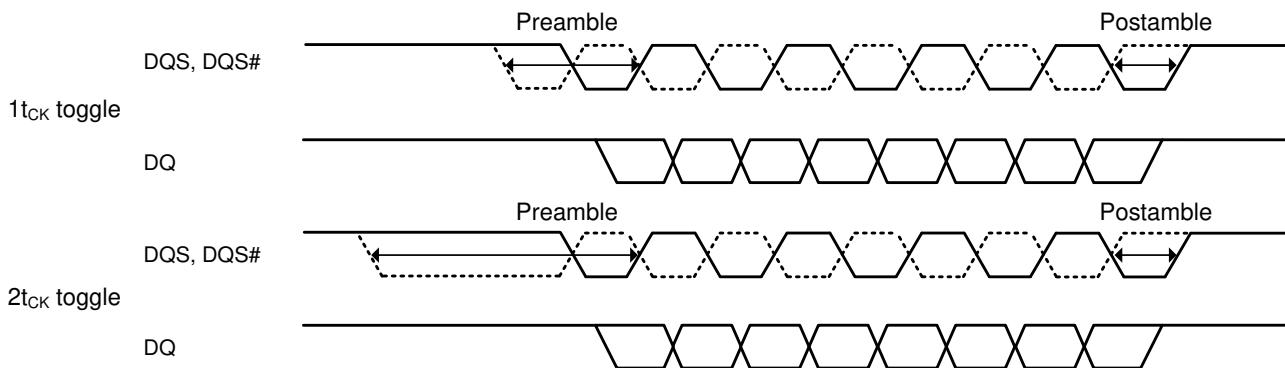


Figure 86. WRITE Postamble

## Activate Command

The Activate command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0 in x16 select the bank group; BA0-BA1 inputs selects the bank within the bank group, and the address provided on inputs A0-A16 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

## Precharge Command

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time ( $t_{RP}$ ) after the Precharge command is issued, except in the case of concurrent auto precharge, where a Read or Write command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A Precharge command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last Precharge command issued to the bank.

If A10 is high when Read or Write command is issued, then auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed ( $t_{RAS}$  satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. The bank will be available for a subsequent row activation a specified time ( $t_{RP}$ ) after hidden Precharge command (AutoPrecharge) is issued to that bank.

## Read Operation

## Read Timing Definitions

Read timings are shown below and are applicable in normal operation mode, i.e. when the DLL is enabled and locked.

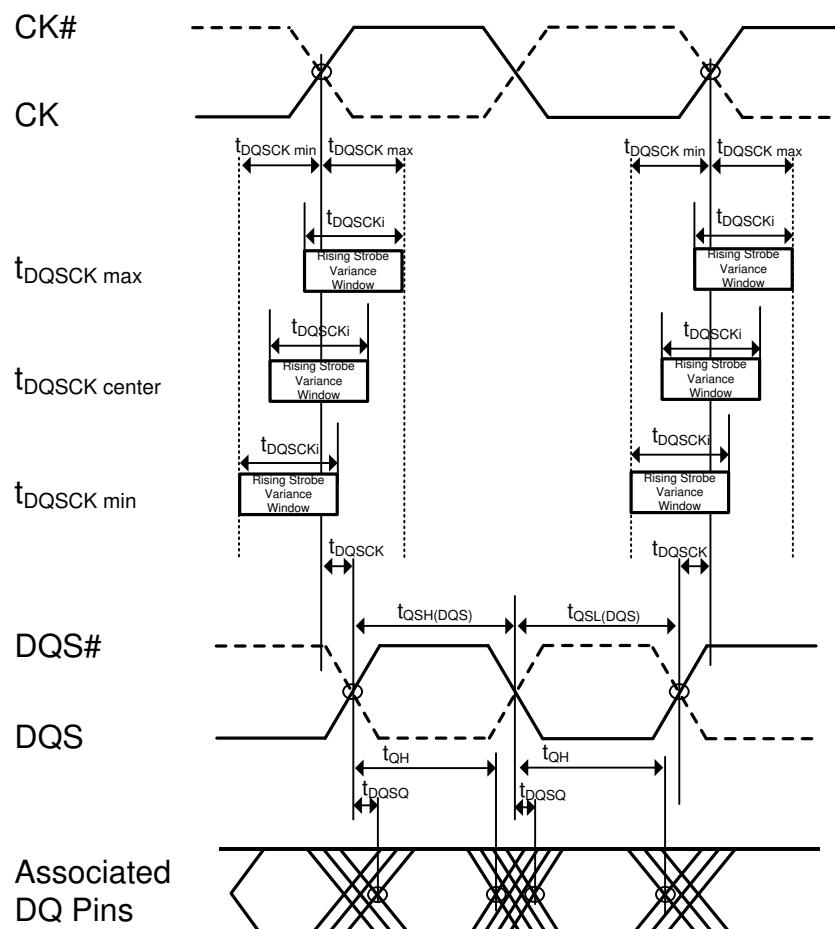
### Rising data strobe edge parameters:

- $t_{DQSCK}$  min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- $t_{DQSCK}$  is the actual position of a rising strobe edge relative to CK, CK#.
- $t_{QSH}$  describes the DQS, DQS# differential output high time.
- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

### Falling data strobe edge parameters:

- $t_{QSL}$  describes the DQS, DQS# differential output low time.
- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

$t_{DQSO}$ ; both rising/falling edges of DQS, no  $t_{AC}$  defined.



**Figure 87. READ Timing Definition**

## Read Timing; Clock to Data Strobe relationship

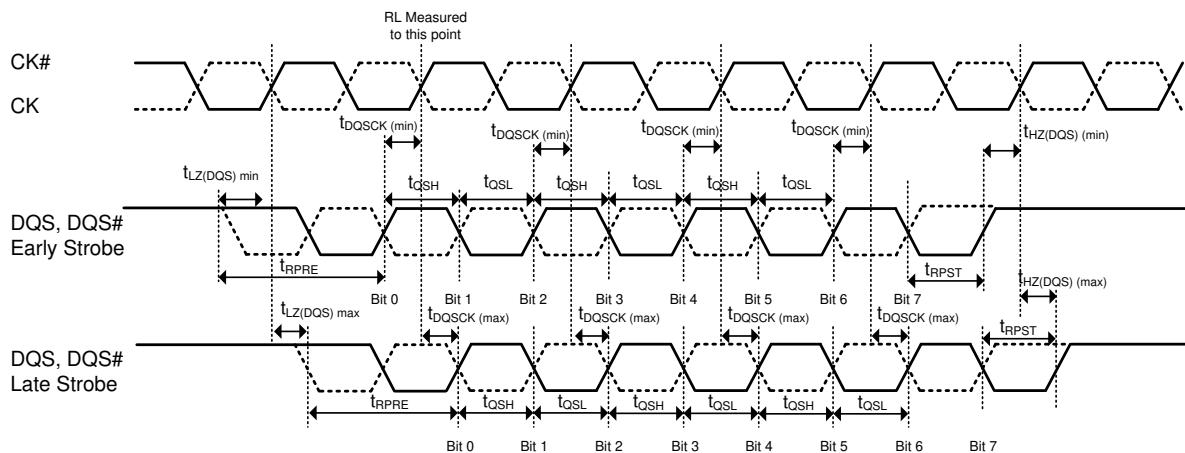
The clock to data strobe relationship is shown below and is applicable in normal operation mode, i.e. when the DLL is enabled and locked.

Rising data strobe edge parameters:

- $t_{DQSK}$  min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- $t_{DQSK}$  is the actual position of a rising strobe edge relative to CK, CK#.
- $t_{QSH}$  describes the data strobe high pulse width.

Falling data strobe edge parameters:

- $t_{QSL}$  describes the data strobe low pulse width.
- $t_{LZ(DQS)}$ ,  $t_{HZ(DQS)}$  for preamble/postamble.



NOTE 1. Within a burst, rising strobe edge can be varied within  $t_{DQSK}$  while at the same voltage and temperature. However incorporate the device, voltage and temperature variation, rising strobe edge variance window,  $t_{DQSK}$  can shift between  $t_{DQSK(\min)}$  and  $t_{DQSK(\max)}$ . A timing of this window's right inside edge ( latest ) from rising CK, CK# is limited by a device's actual  $t_{DQSK(\max)}$ . A timing of this window's left inside edge (earliest) from rising CK, CK# is limited by  $t_{DQSK(\min)}$ .

NOTE 2. Notwithstanding note 1, a rising strobe edge with  $t_{DQSK(\max)}$  at T(n) can not be immediately followed by a rising strobe Edge with  $t_{DQSK(\min)}$  at T(n+1). This is because other timing relationships ( $t_{QSH}$ ,  $t_{QSL}$ ) exist: if  $t_{DQSK(n+1)} < 0$ :

$$t_{DQSK(n)} < 1.0 t_{CK} - (t_{QSH\min} + t_{QSL\min}) - |t_{DQSK(n+1)}|$$

NOTE 3. The DQS, DQS# differential output high time is defined by  $t_{QSH}$  and the DQS, DQS# differential output low time is defined by  $t_{QSL}$ .

NOTE 4. LikeWise,  $t_{LZ(DQS)}$ min and  $t_{HZ(DQS)}$ min are not tied to  $t_{DQSK\min}$  (early strobe case) and  $t_{LZ(DQS)}$ max and  $t_{HZ(DQS)}$ max are not tied to  $t_{DQSK\max}$  (late strobe case).

NOTE 5. The minimum pulse width of read preamble is defined by  $t_{RPRE(\min)}$ .

NOTE 6. The maximum read postamble is bound by  $t_{DQSK(\min)}$  plus  $t_{QSH(\min)}$  on the left side and  $t_{HZDQS(\max)}$  on the right side.

NOTE 7. The minimum pulse width of read postamble is defined by  $t_{RPST(\min)}$ .

NOTE 8. The maximum read preamble is bound by  $t_{LZDQS(\min)}$  on the left side and  $t_{DQSK(\max)}$  on the right side.

**Figure 88. Clock to Data Strobe Relationship**

## Read Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

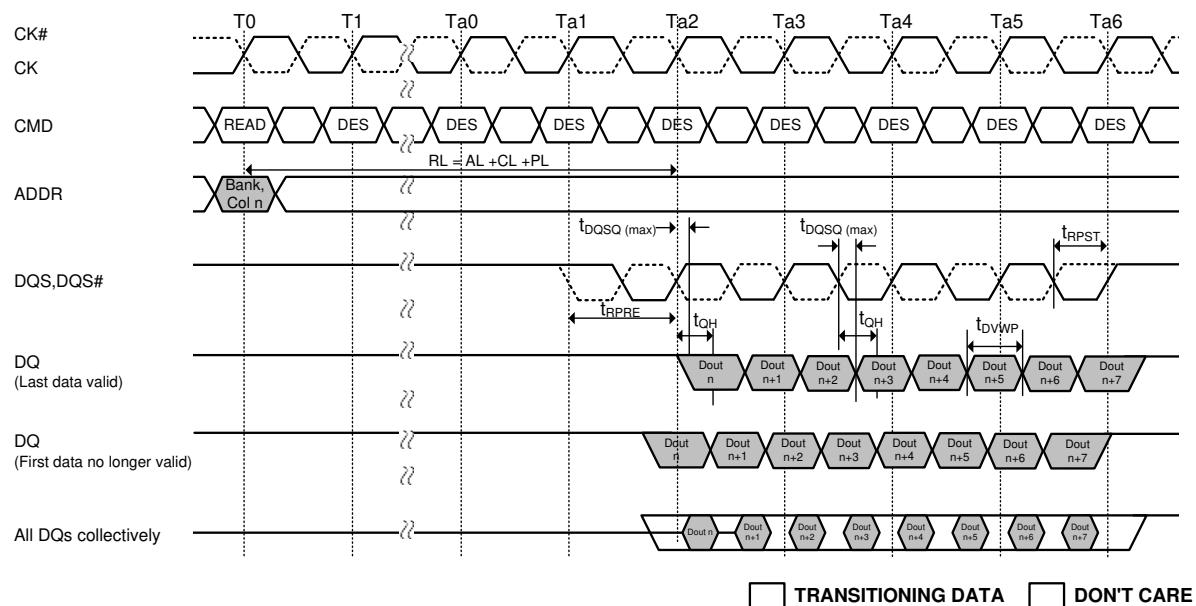
Falling data strobe edge parameters:

- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

$t_{DQSQ}$ ; both rising/falling edges of DQS, no tAC defined.

Data Valid Window:

- $t_{DVW_d}$  is the Data Valid Window per device per UI and is derived from  $(t_{QH} - t_{DQSQ})$  of each UI on a given DRAM. This parameter will be characterized and guaranteed by design.
- $t_{DVW_p}$  is Data Valid Window per pin per UI and is derived from  $(t_{QH} - t_{DQSQ})$  of each UI on a pin of a given DRAM. This parameter will be characterized and guaranteed by design.



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble =  $1_{CK}$

NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5. Output timings are referenced to VDDQ, and DLL on for locking.

NOTE 6.  $t_{DQSQ}$  defines the skew between DQS, DQS# to Data and does not define DQS, DQS# to Clock.

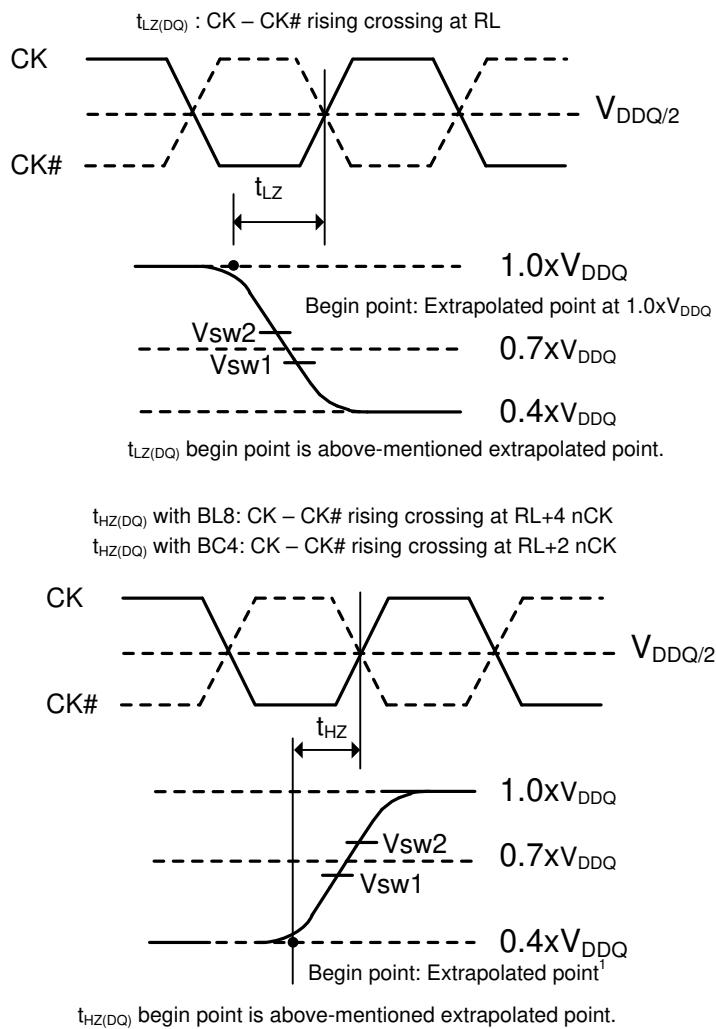
NOTE 7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

**Figure 89. Data Strobe to Data Relationship**

### **t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, t<sub>HZ(DQS)</sub>, t<sub>HZ(DQ)</sub> Calculation**

t<sub>HZ</sub> and t<sub>LZ</sub> transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving t<sub>HZ(DQS)</sub> and t<sub>HZ(DQ)</sub>, or begins driving t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>.

t<sub>LZ</sub> shows a method to calculate the point when the device is no longer driving t<sub>HZ(DQS)</sub> and t<sub>HZ(DQ)</sub>, or begins driving t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters t<sub>LZ(DQS)</sub>, t<sub>LZ(DQ)</sub>, t<sub>HZ(DQS)</sub>, and t<sub>HZ(DQ)</sub> are defined as single ended.



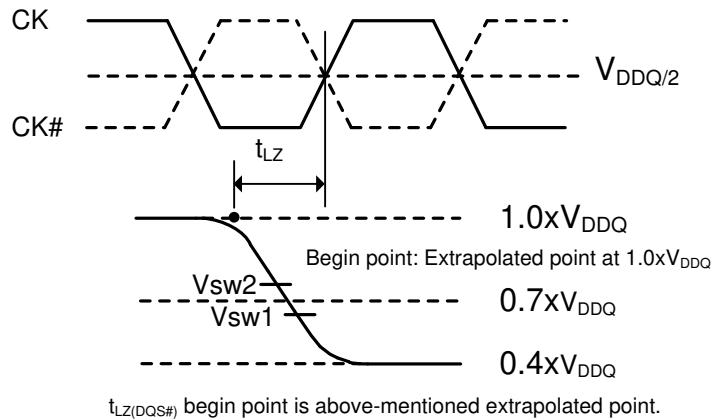
NOTE 1. Extrapolated point (Low Level) =  $V_{DDQ}/(50+34) \times 34$   
 $= V_{DDQ} \times 0.40$   
- A driver impedance :  $RZQ/7(34\text{ohm})$   
- An effective test load :  $50 \text{ ohm}$  to  $V_{TT} = V_{DDQ}$

**Figure 90. tLZ(DQ) and tHZ(DQ) method for calculating transitions and begin points**

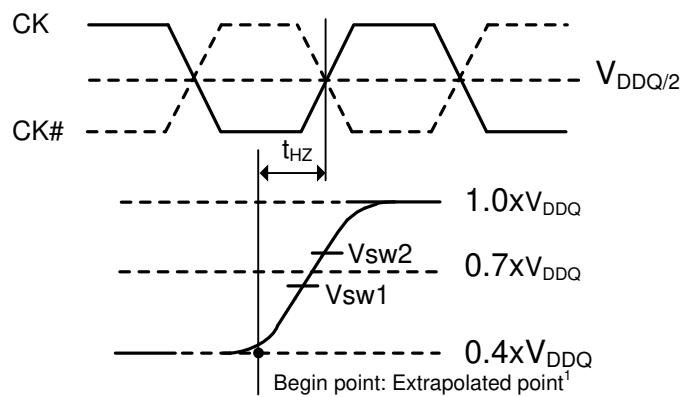
**Table 37. Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements**

Symbol	Parameter	V <sub>sw1</sub>	V <sub>sw2</sub>	Unit
t <sub>LZ(DQ)</sub>	DQ low-impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V
t <sub>HZ(DQ)</sub>	DQ high impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V

$t_{LZ(DQS\#)}$  : CK – CK# rising crossing at RL-1 with  $1t_{CK}$  Preamble  
 $t_{LZ(DQS\#)}$  : CK – CK# rising crossing at RL-2 with  $1t_{CK}$  Preamble



$t_{HZ(DQS)}$  with BL8: CK – CK# rising crossing at RL+4 nCK  
 $t_{HZ(DQS)}$  with BC4: CK – CK# rising crossing at RL+2 nCK

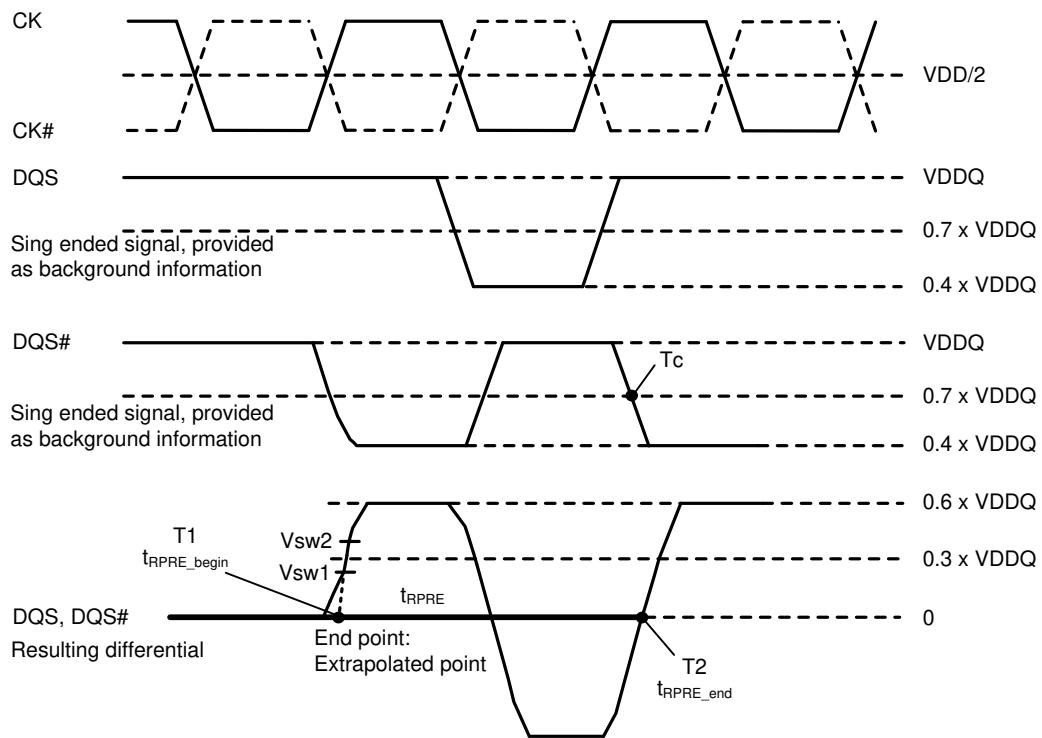


NOTE 1. Extrapolated point (Low Level) =  $V_{DDQ}/(50+34) \times 34$   
=  $V_{DDQ} \times 0.40$   
- A driver impedance : RZQ/7(34ohm)  
- An effective test load : 50 ohm to  $V_{TT} = V_{DDQ}$

Figure 91.  $t_{LZ(DQS\#)}$  and  $t_{HZ(DQS)}$  method for calculating transitions and begin

Table 38. Reference Voltage for  $t_{LZ(DQS\#)}$ ,  $t_{HZ(DQS)}$  Timing Measurements

Symbol	Parameter	$V_{sw1}$	$V_{sw2}$	Unit
$t_{LZ(DQS\#)}$	DQS# low-impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V
$t_{HZ(DQS)}$	DQS high impedance time from CK, CK#	$(0.70 - 0.04) \times V_{DDQ}$	$(0.70 + 0.04) \times V_{DDQ}$	V



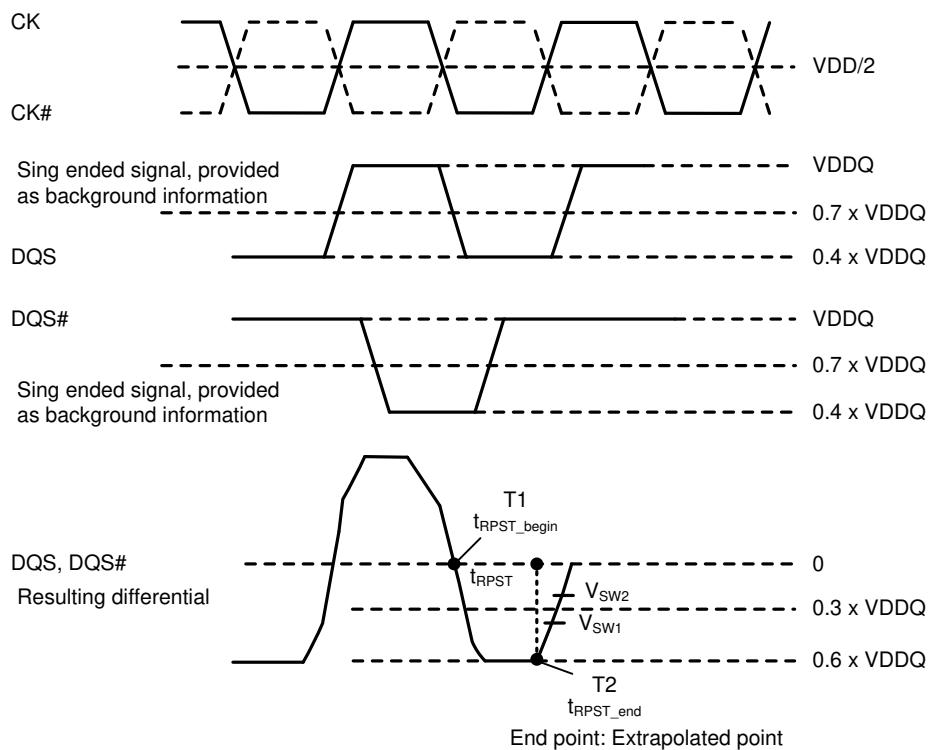
NOTE 1. Low Level of DQS and DQS# =  $V_{DDQ}/(50+34) \times 34$   
 $= V_{DDQ} \times 0.40$

- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to  $V_{TT} = V_{DDQ}$

**Figure 92. Method for calculating tRPRE transitions and endpoints**

**Table 39. Reference Voltage for tRPRE Timing Measurements**

Symbol	Parameter	V <sub>sw1</sub>	V <sub>sw2</sub>	Unit
t <sub>RPRE</sub>	DQS, DQS# differential Read Preamble	$(0.30 - 0.04) \times V_{DDQ}$	$(0.30 + 0.04) \times V_{DDQ}$	V



NOTE 1. Low Level of DQS and DQS# =  $V_{DDQ}/(50+34) \times 34$   
 $= V_{DDQ} \times 0.40$

- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to  $V_{TT} = V_{DDQ}$

**Figure 93. Method for calculating tRPST transitions and endpoints**

**Table 40. Reference Voltage for tRPST Timing Measurements**

Symbol	Parameter	$V_{sw1}$	$V_{sw2}$	Unit
$t_{RPST}$	DQS, DQS# differential Read Postamble	$(-0.30 - 0.04) \times V_{DDQ}$	$(-0.30 + 0.04) \times V_{DDQ}$	V

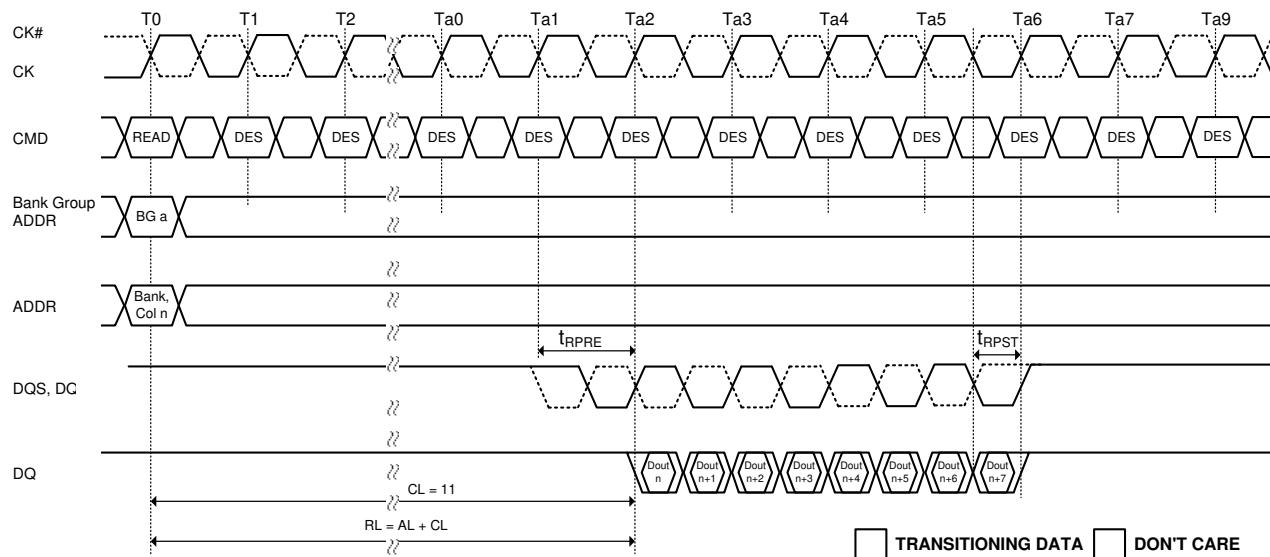
## Read Burst Operation

DDR4 Read command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF during the Read or Write (auto-precharge can be enabled or disabled).

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

Read commands can issue precharge automatically with a read with auto-precharge command (RDA); and is enabled by A10 high.

- Read command with A10 = 0 (RD) performs standard Read, bank remains active after read burst.
- Read command with A10 = 1 (RDA) performs Read with auto-precharge, bank goes in to precharge after read burst.



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1t<sub>CK</sub>

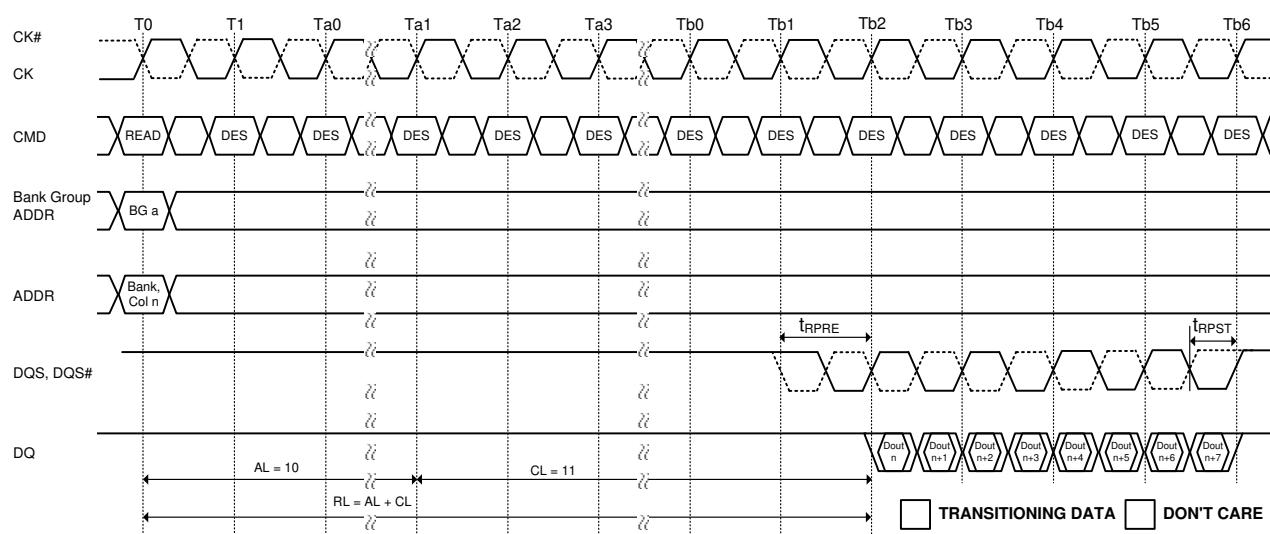
NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:0 = 00] or MRO[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 94. READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)**



NOTE 1. BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1t<sub>CK</sub>

NOTE 2. Dout n = data-out from column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:0 = 00] or MRO[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 95. READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)**

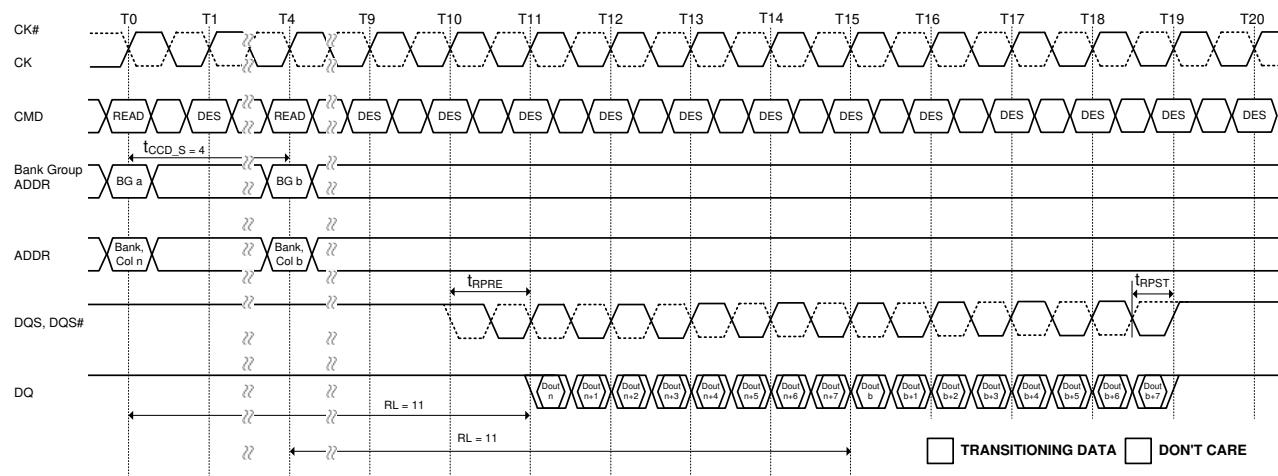


Figure 96. Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group

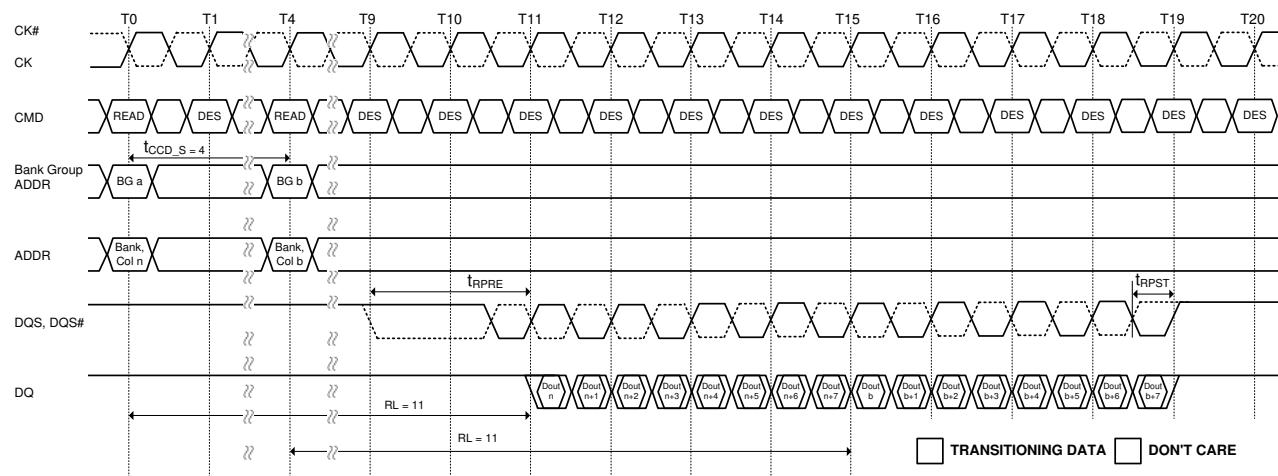
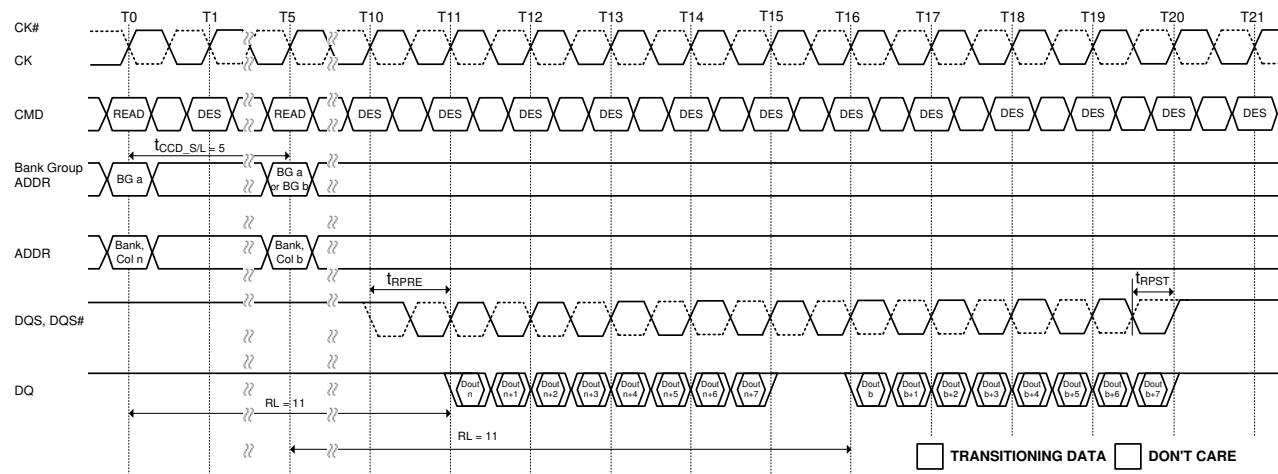


Figure 97. Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK,  $t_{CCD\_SL} = 5$

NOTE 2. Dout n (or b) = data-out from column n (or column b).

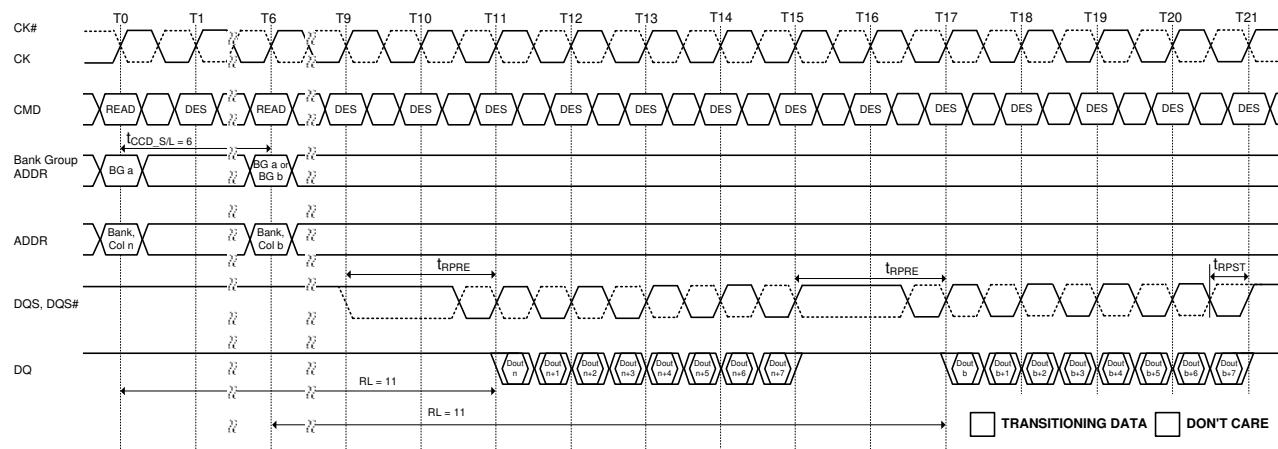
NOTE 4. PL0 settings activated by either MP0[A1:A2=0:0] or MP0[A1:A2=0:1] and A12=1 during RECALL.

NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T5.

NOTE 5. CA Parity: Pin 18, CS to CA, Interleave: Pin 17, Read BL1, Pin 11.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

**Figure 98. Nonconsecutive READ (BL8) with 1t<sub>CK</sub> Preamble in Same or Different Bank Group**



NOTE 1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK,  $t_{CCD\_S/L} = 6$

NOTE 2. Dout n (or b) = data-out from column n (or column b).

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 4. PL/SQL routines created by either MR01(A1,A2...2,0) or MR01(A1,A2...2,1) via REAM

NOTE 4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T6.

NOTE 5. CA-Beritx = Disble, CS = CA-Letency = Disble, Read-DPL = Disble

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable  
NOTE 6.  $t_{CKP} \geq -5$  isn't allowed in  $2t_{CK}$  preamble mode

NOTE 6.  $t_{CCD\_S/L} = 5$  isn't allowed in  $2t_{CK}$  preamble mode.

Figure 99. Nonconsecutive READ (BL8) with  $2t_{CK}$  Preamble in Same or Different Bank Group

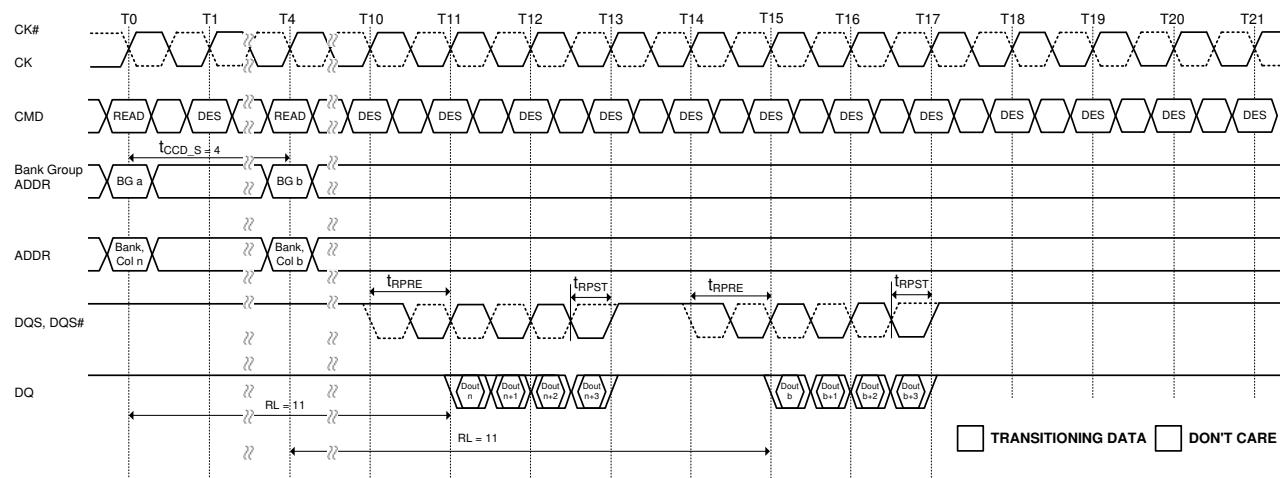


Figure 100. READ (BC4) to READ (BC4) with  $1t_{CK}$  Preamble in Different Bank Group

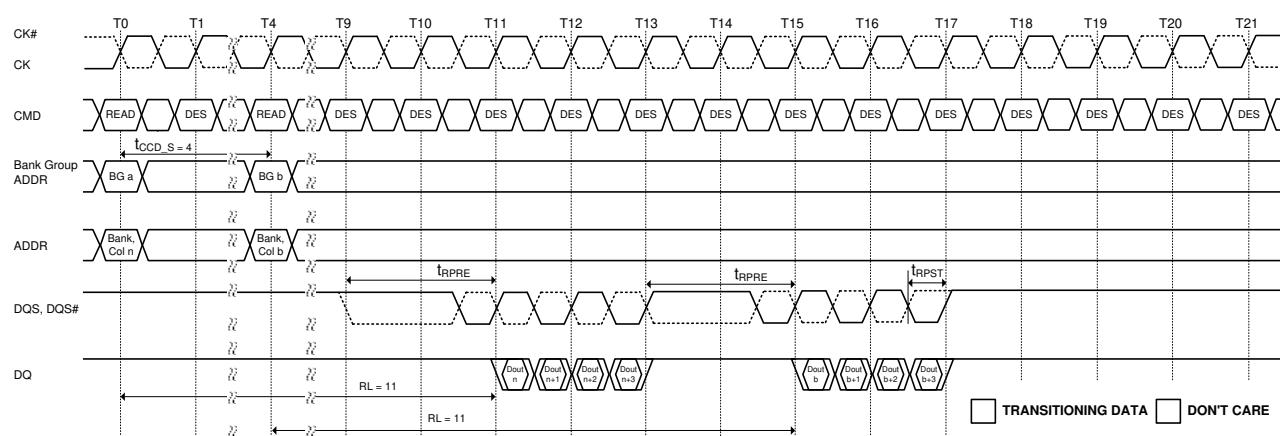


Figure 101. READ (BC4) to READ (BC4) with  $2t_{CK}$  Preamble in Different Bank Group

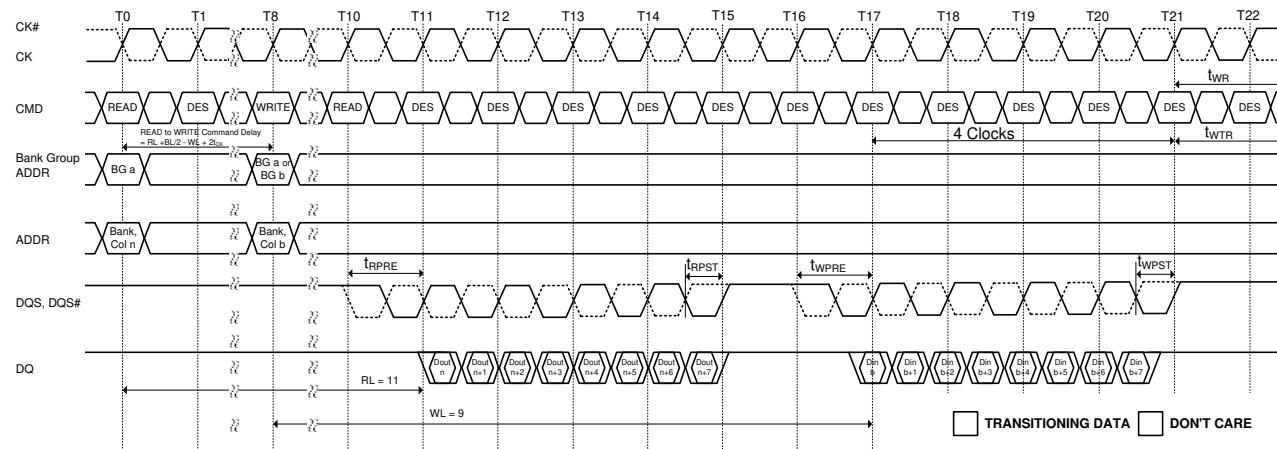


Figure 102. READ (BL8) to WRITE (BL8) with  $1t_{CK}$  Preamble in Same or Different Bank Group

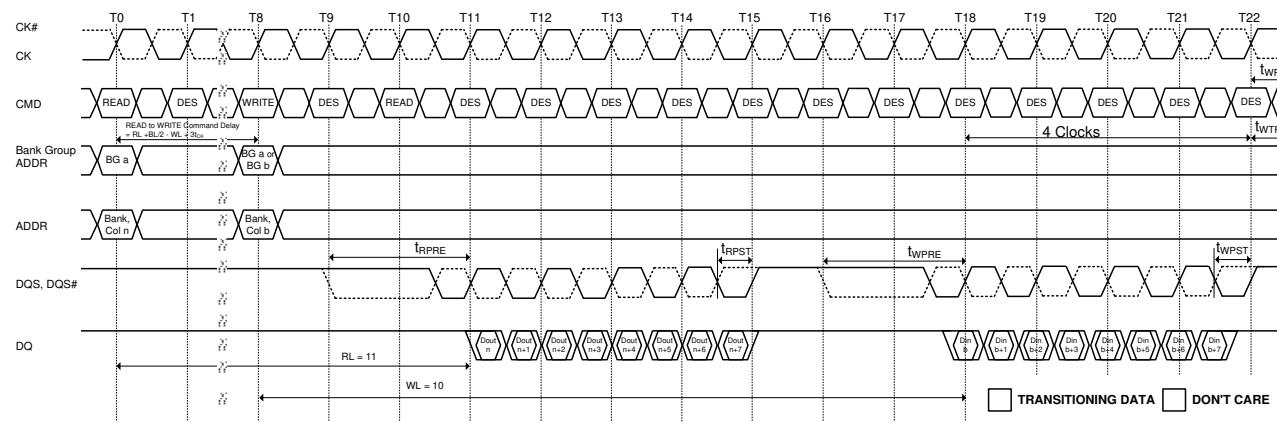
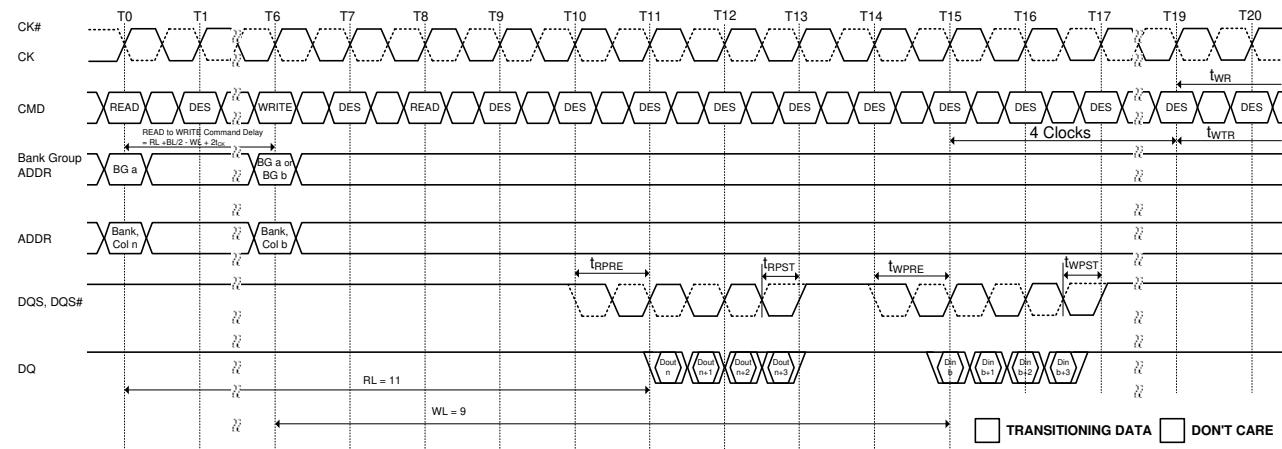
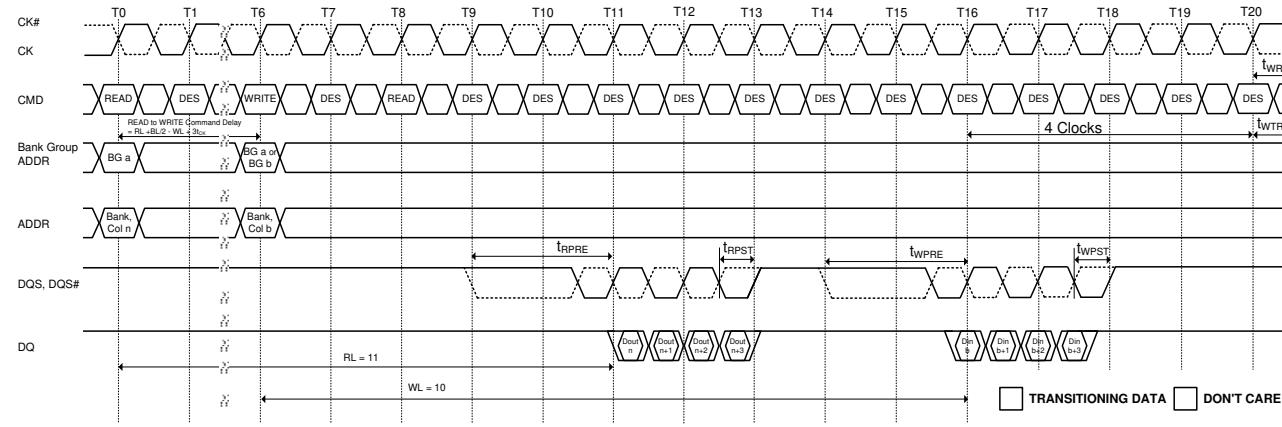


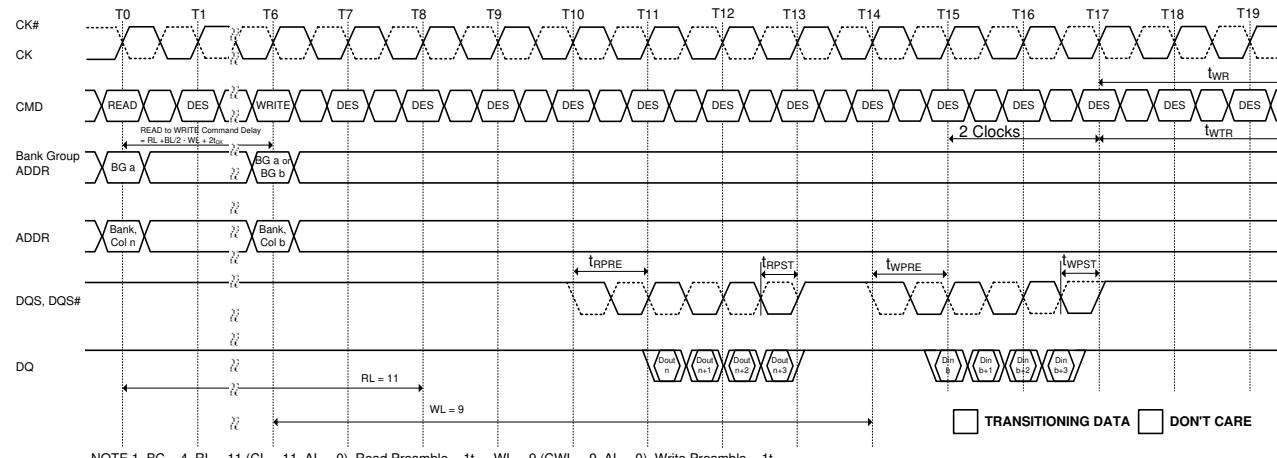
Figure 103. READ (BL8) to WRITE (BL8) with  $2t_{CK}$  Preamble in Same or Different Bank Group



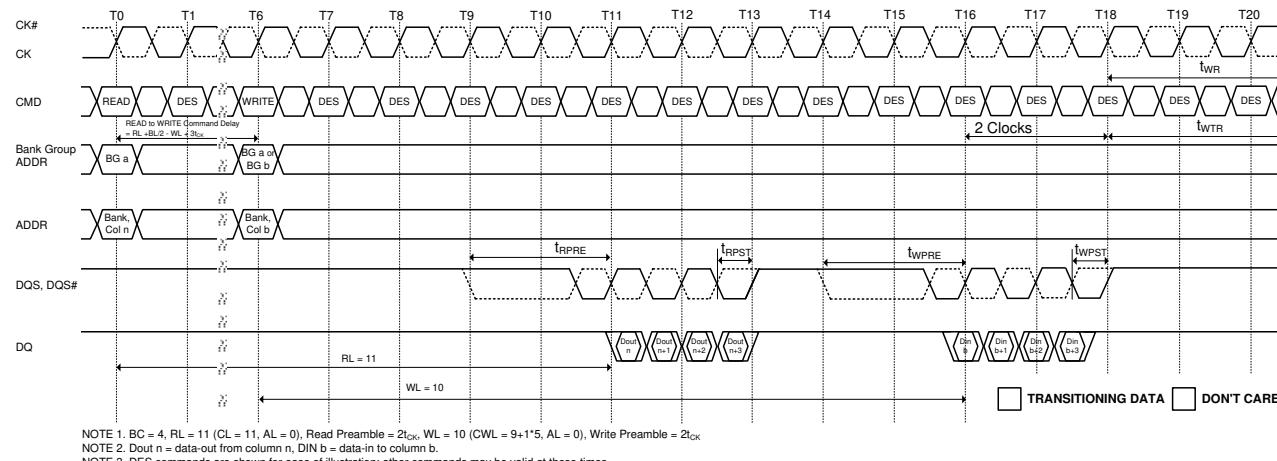
**Figure 104. READ (BC4) OTF to WRITE (BC4) OTF with  $1t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 105. READ (BC4) OTF to WRITE (BC4) OTF with  $2t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 106. READ (BC4) Fixed to WRITE (BC4) Fixed with  $1t_{CK}$  Preamble in Same or Different Bank Group**



**Figure 107. READ (BC4) Fixed to WRITE (BC4) Fixed with  $2t_{CK}$  Preamble in Same or Different Bank Group**

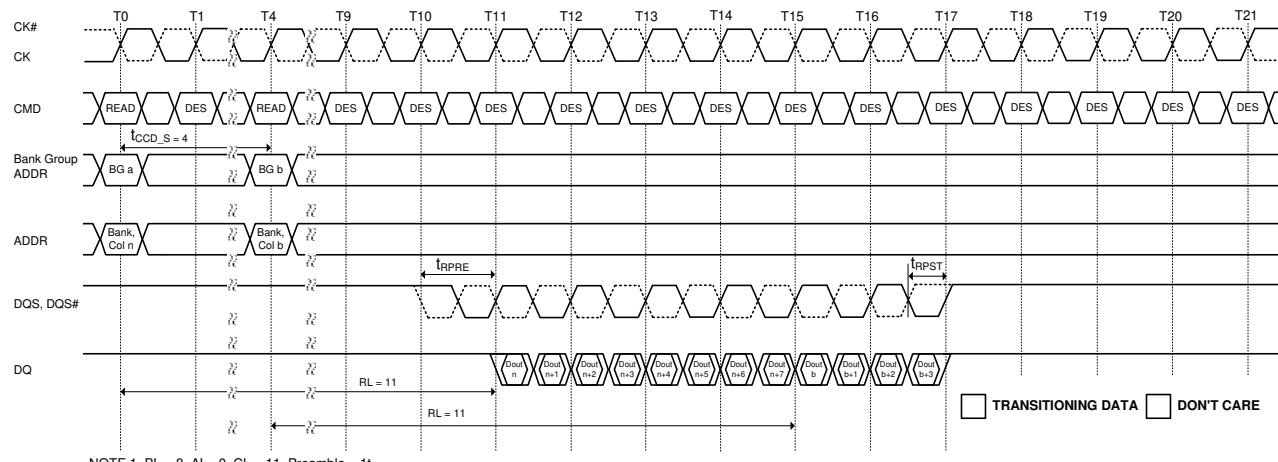


Figure 108. READ (BL8) to READ (BC4) OTF with 1t<sub>CK</sub> Preamble in Different Bank Group

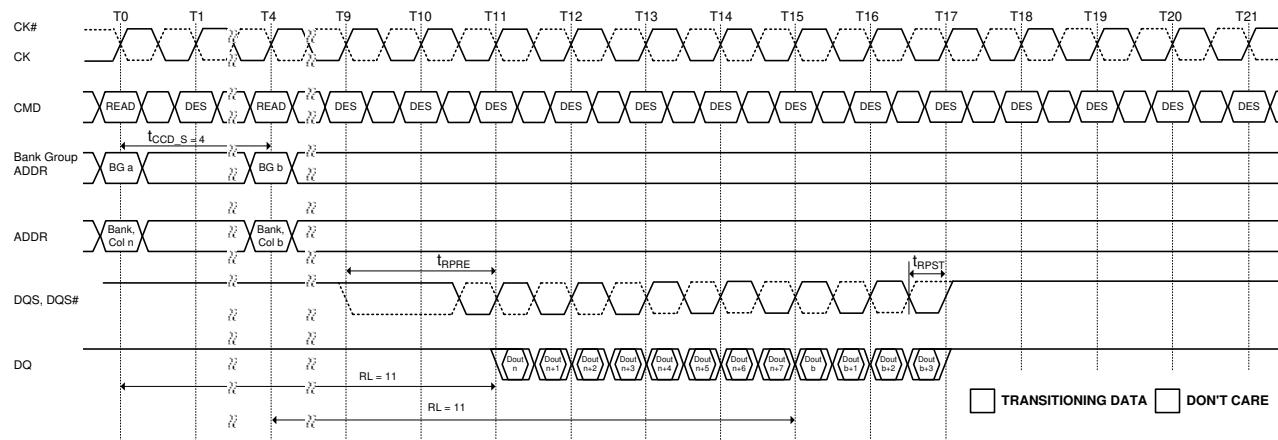


Figure 109. READ (BL8) to READ (BC4) OTF with 2t<sub>CK</sub> Preamble in Different Bank Group

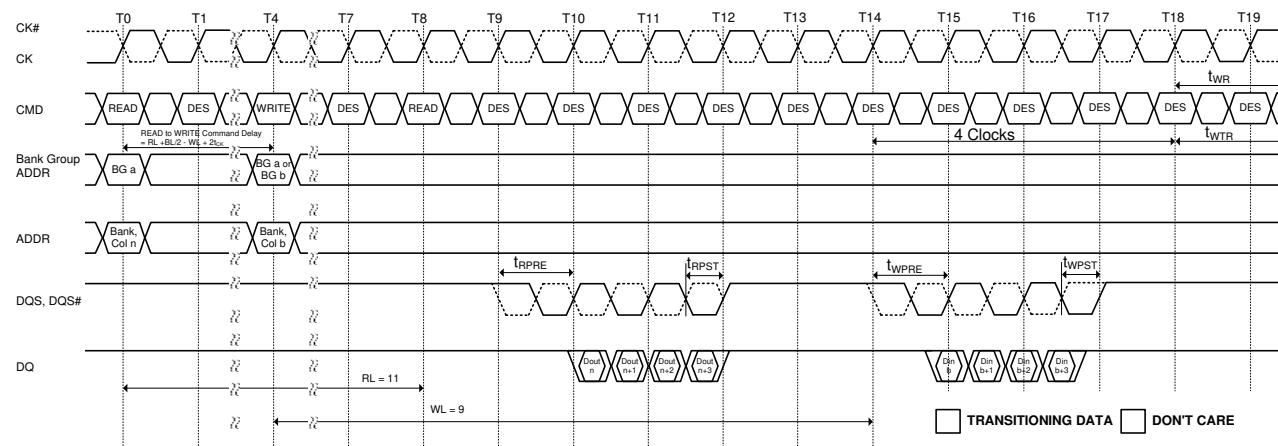


Figure 110. READ (BC4) to READ (BL8) OTF with  $1t_{CK}$  Preamble in Different Bank Group

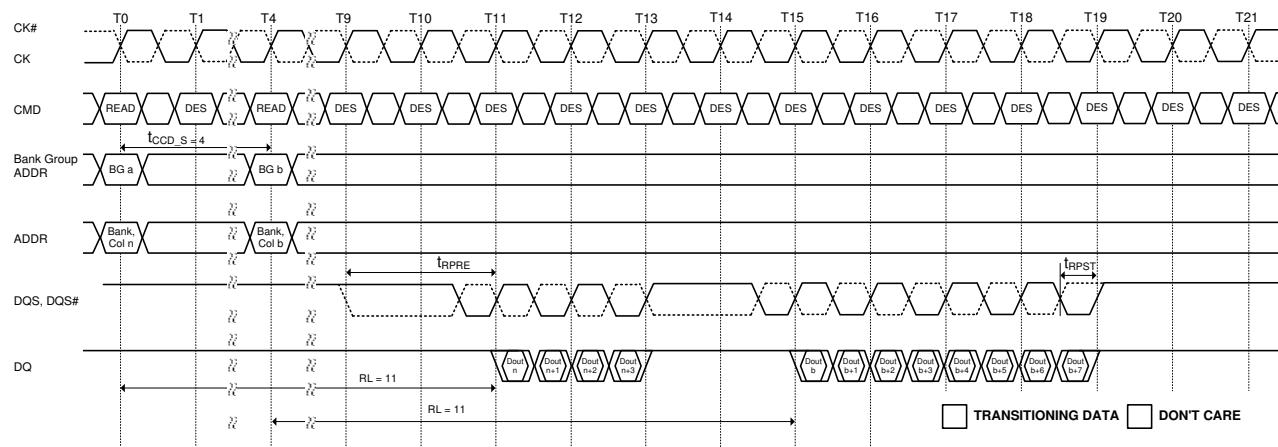


Figure 111. READ (BC4) to READ (BL8) OTF with  $2t_{CK}$  Preamble in Different Bank Group

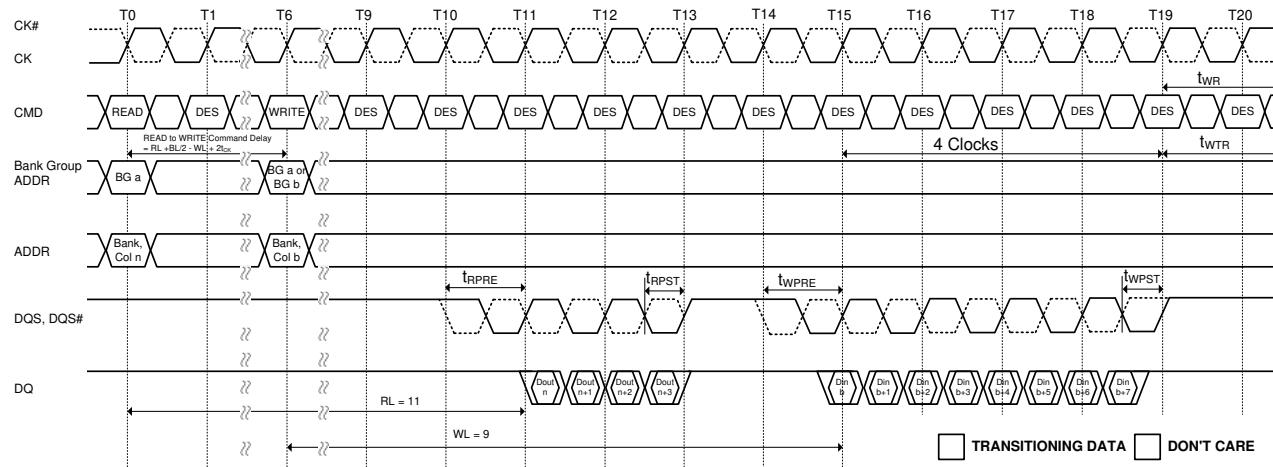


Figure 112. READ (BC4) to WRITE (BL8) OTF with  $1t_{CK}$  Preamble in Same or Different Bank Group

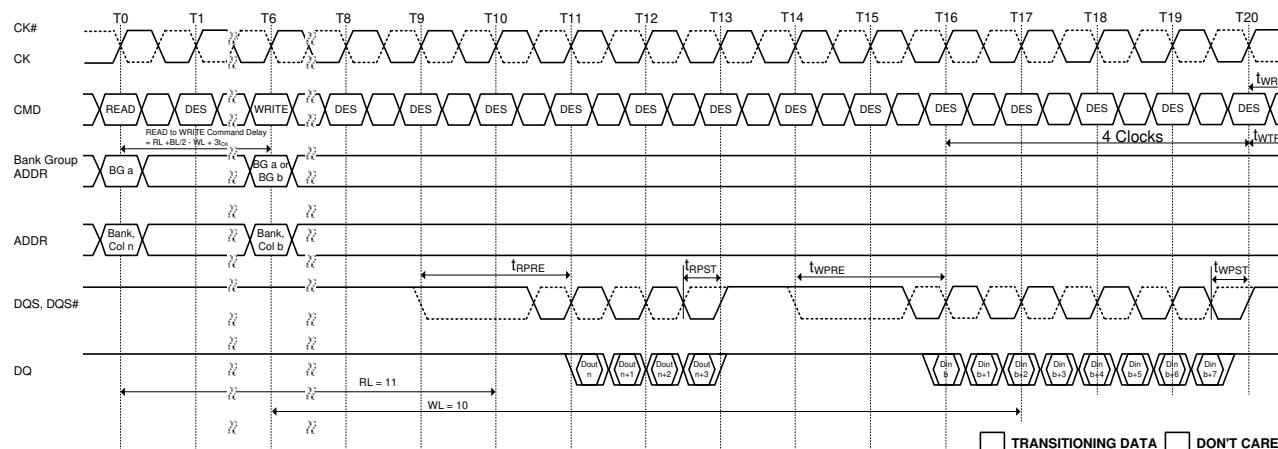


Figure 113. READ (BC4) to WRITE (BL8) OTF with  $2t_{CK}$  Preamble in Same or Different Bank Group

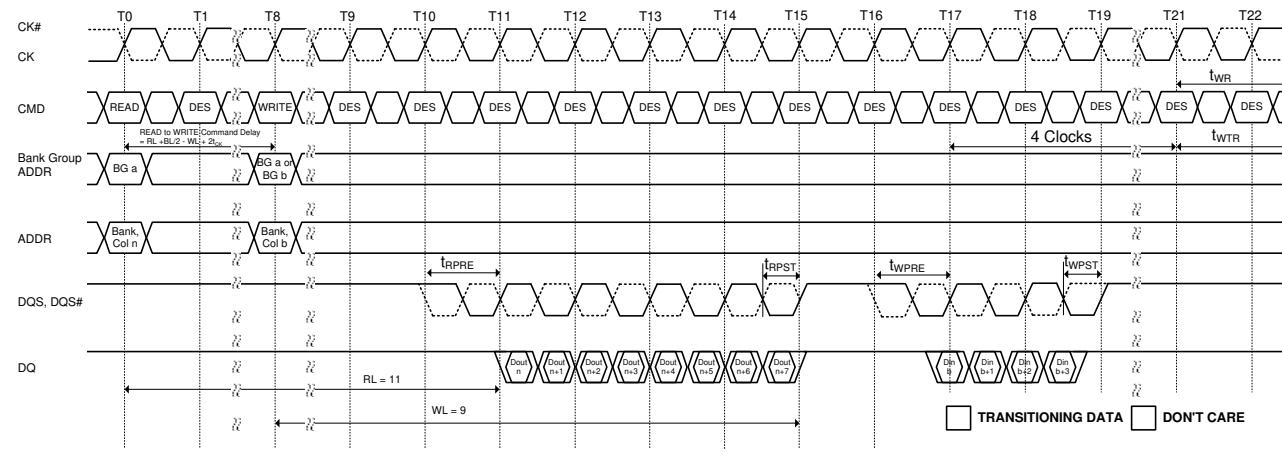


Figure 114. READ (BL8) to WRITE (BC4) OTF with 1t<sub>CK</sub> Preamble in Same or Different Bank Group

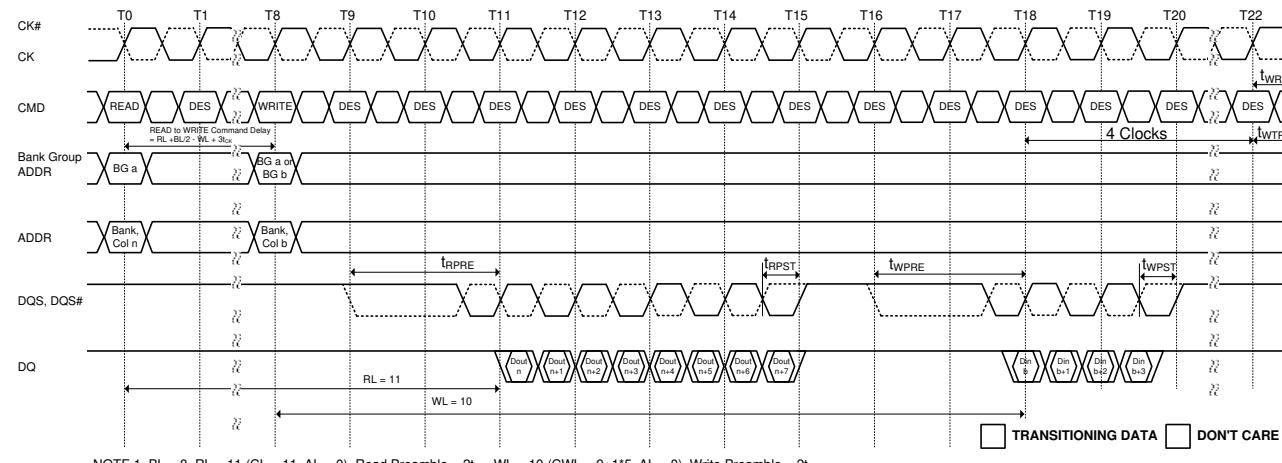


Figure 115. READ (BL8) to WRITE (BC4) OTF with 2t<sub>CK</sub> Preamble in Same or Different Bank Group

## Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to  $AL + t_{RTP}$  with  $t_{RTP}$  being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing,  $t_{RAS}$ , must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by  $t_{RTP(min)}$ . A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time ( $t_{RP(min)}$ ) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time ( $t_{RC(min)}$ ) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Read to Precharge with  $1t_{CK}$  Preamble to Read to Precharge with Additive Latency and  $1t_{CK}$  Preamble.

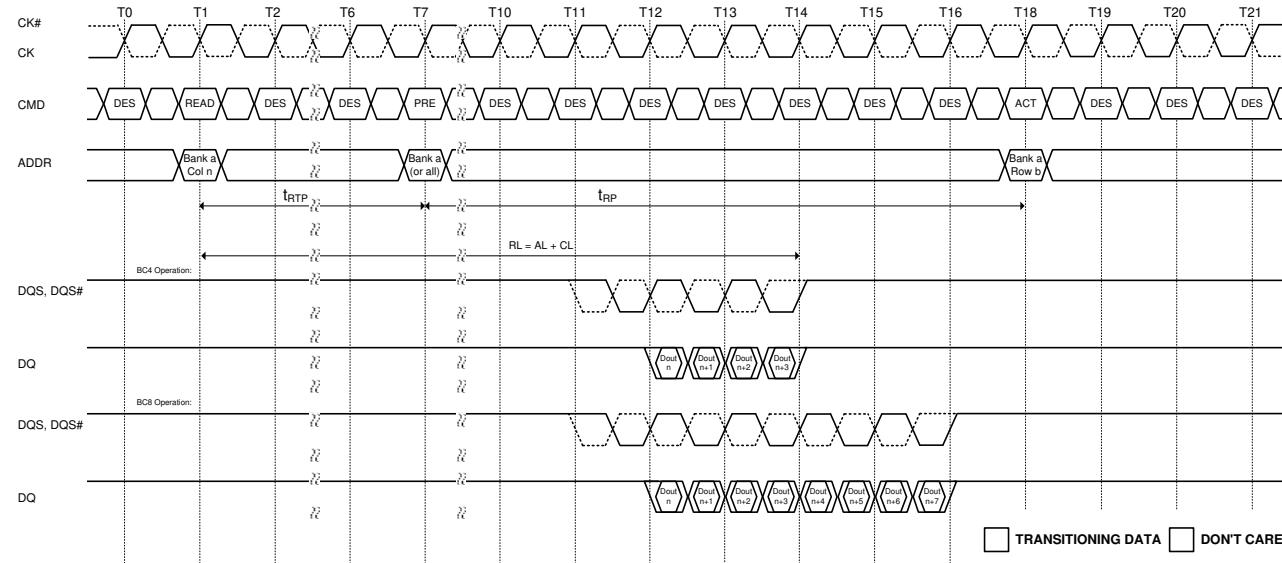


Figure 116. READ to PRECHARGE with  $1t_{CK}$  Preamble

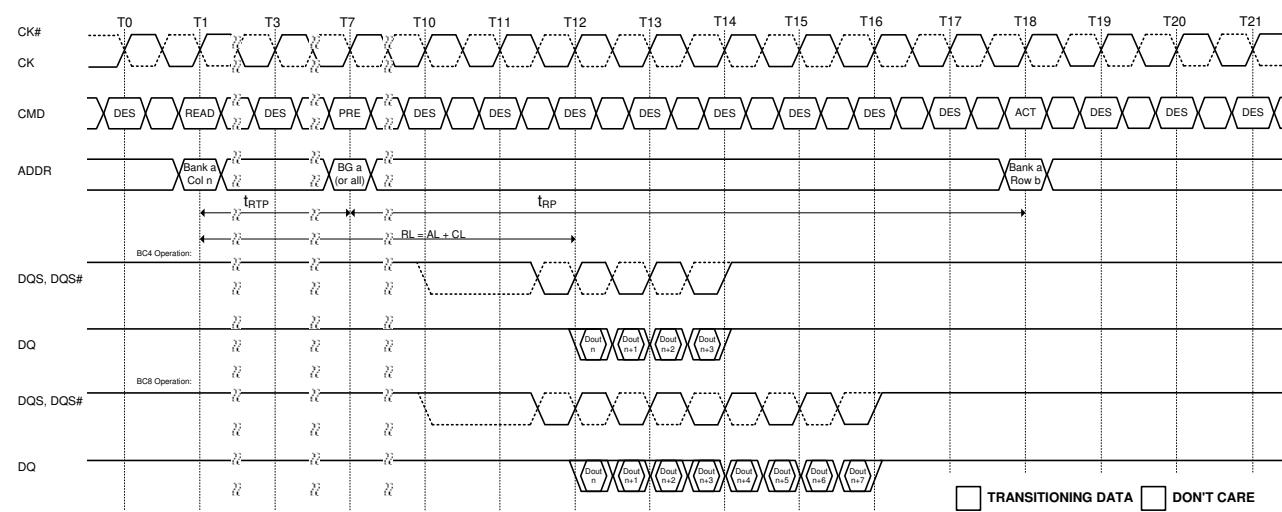


Figure 117. READ to PRECHARGE with  $2t_{CK}$  Preamble

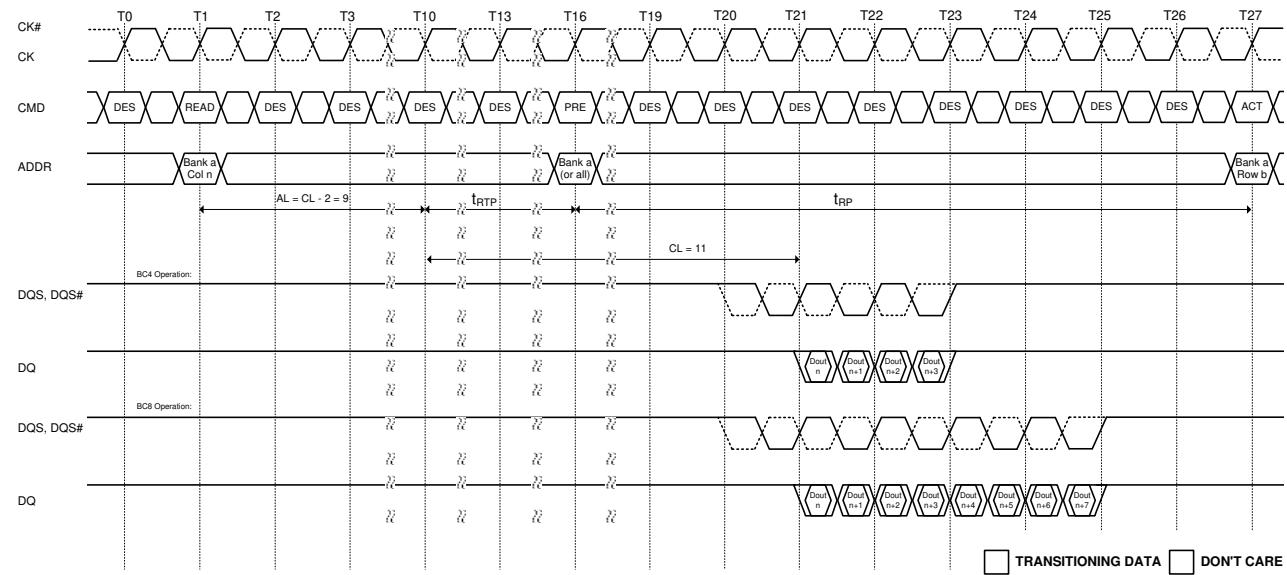


Figure 118. READ to PRECHARGE with Additive Latency and 1t<sub>CK</sub> Preamble

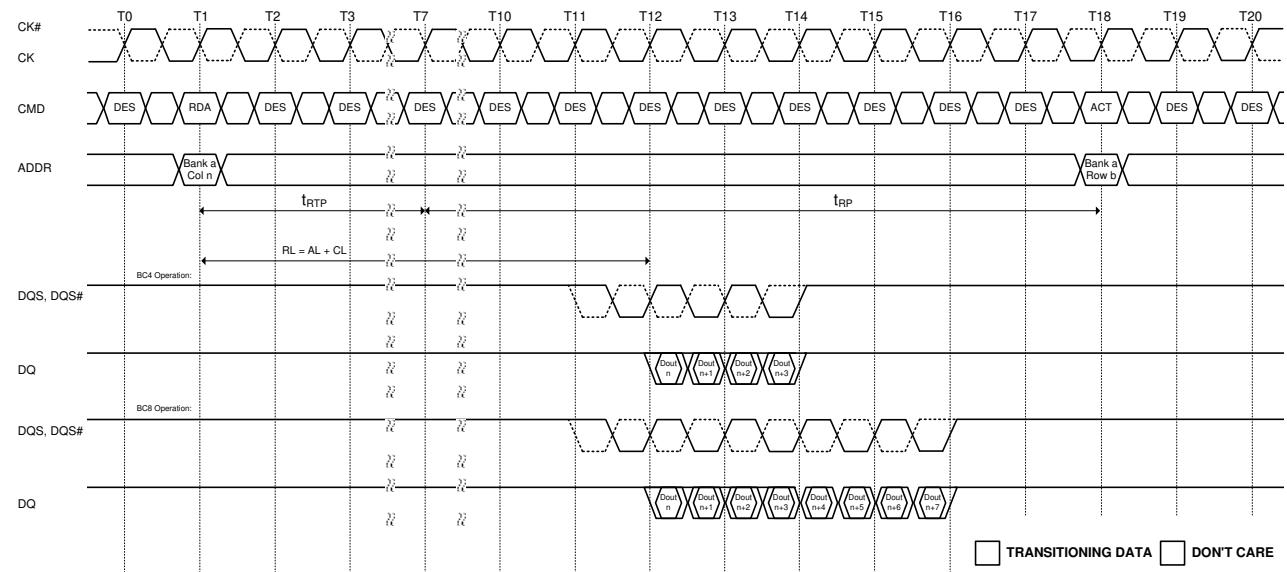


Figure 119. READ with Auto Precharge and 1t<sub>CK</sub> Preamble

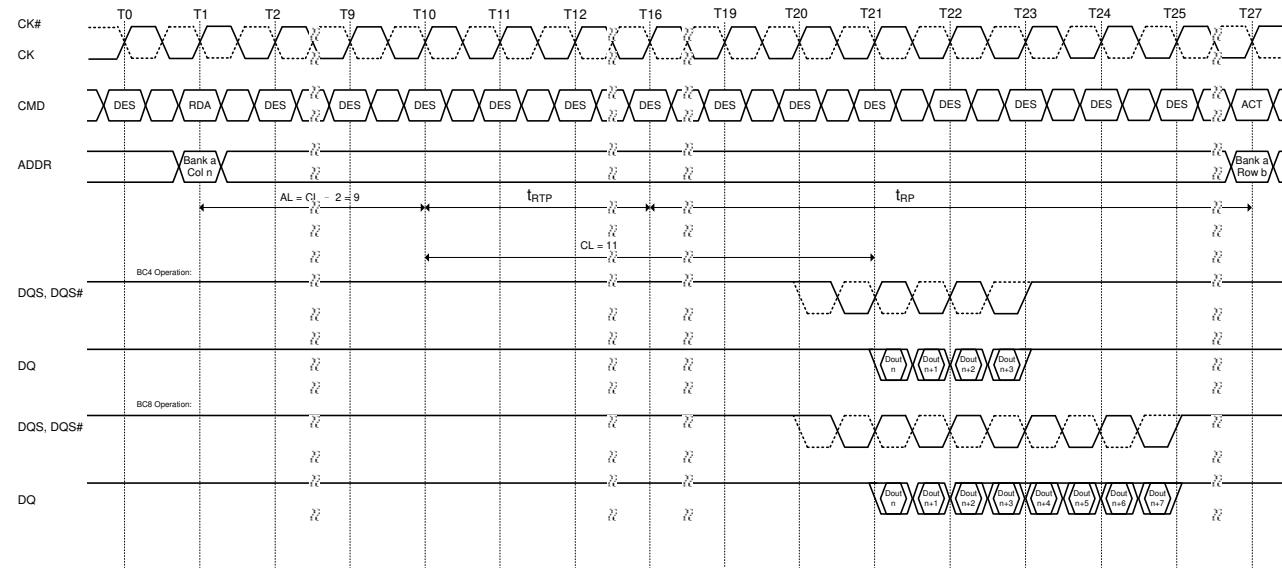
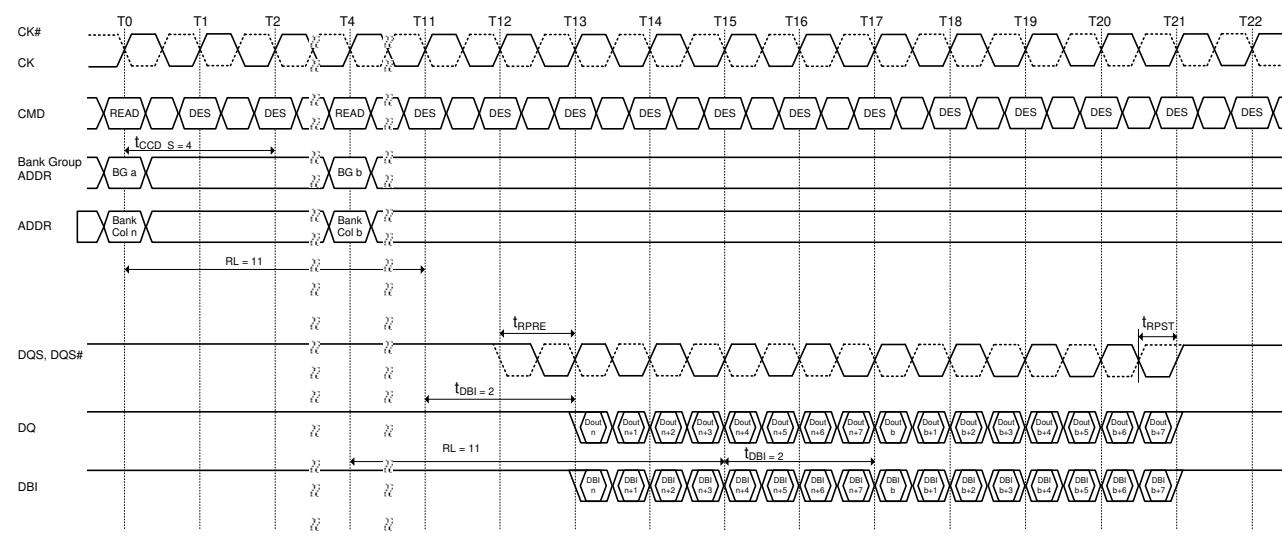


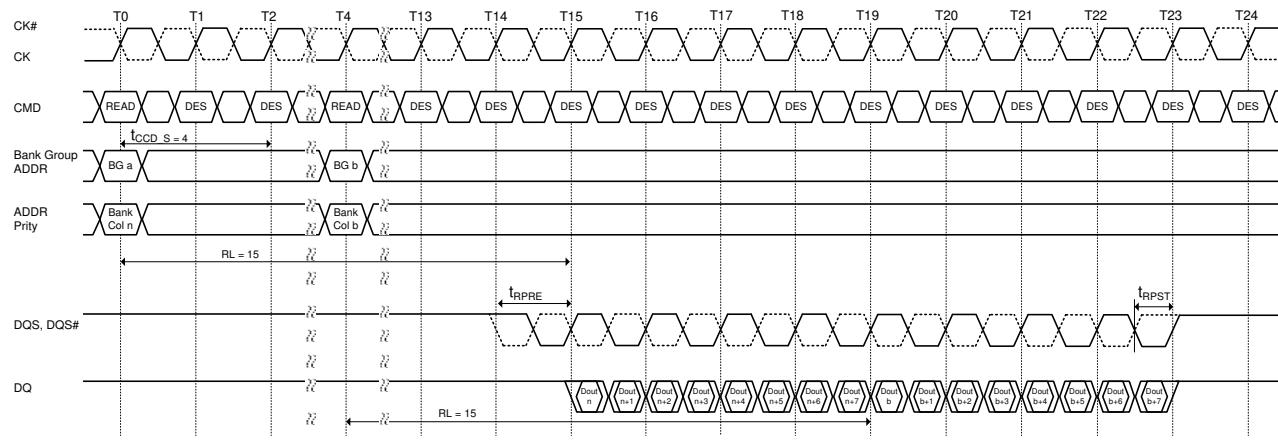
Figure 120. READ with Auto Precharge, Additive Latency and  $1t_{CK}$  Preamble

## Burst Read Operation with Read DBI (Data Bus Inversion)



**Figure 121. Consecutive READ (BL8) with 1t<sub>CK</sub> Preamble and DBI in Different Bank Group**

## Burst Read Operation with Command/Address Parity



NOTE 1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK

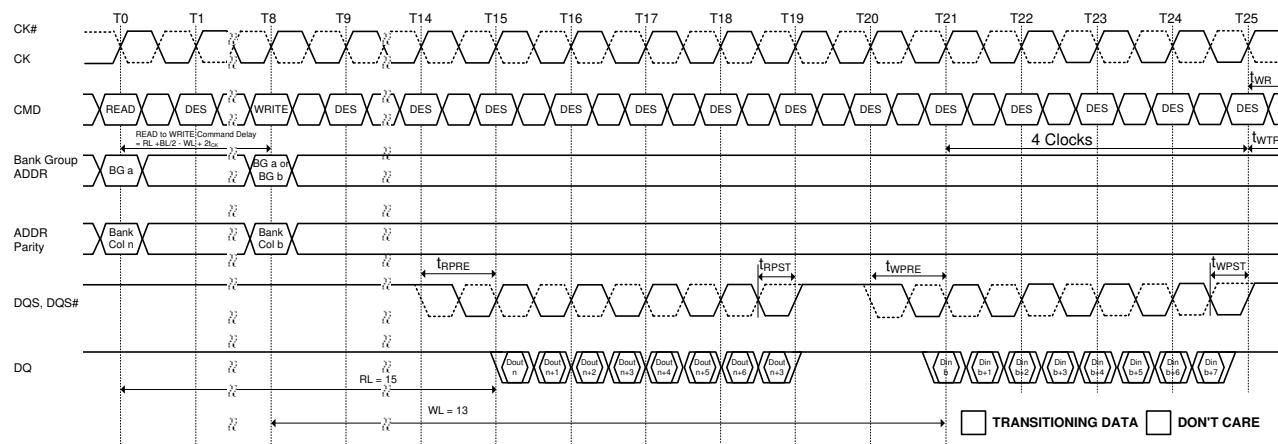
NOTE 2. Dout n (or b) = data-out from column n (or column b).

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5. CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 122. Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1. BC = 4, RL = 11(CL = 11, AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

NOTE 2. Dout n = data-out from column n, Din b = data-in to column b.

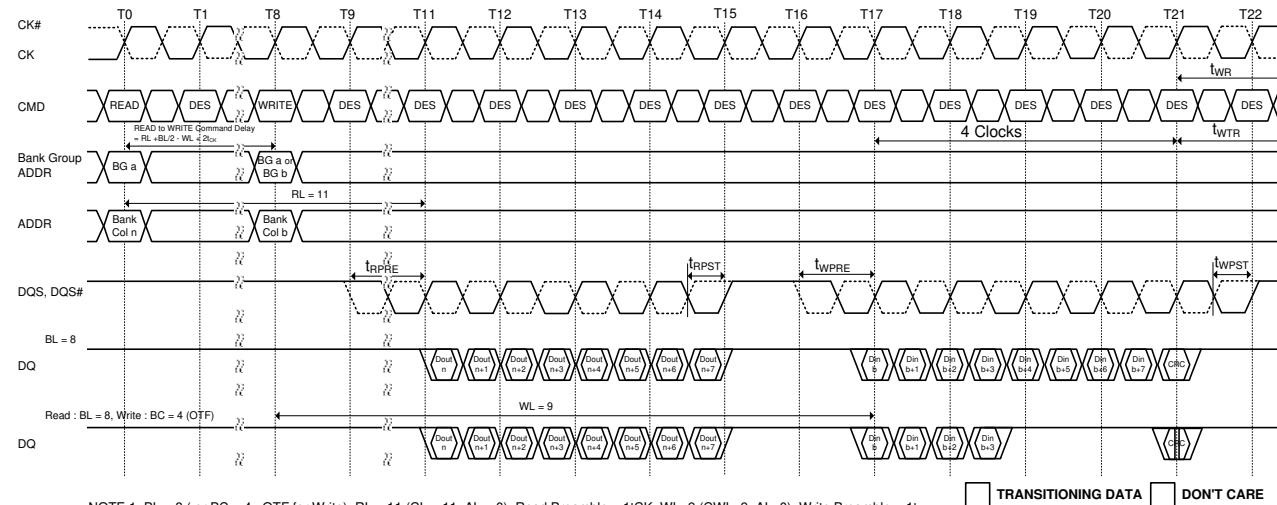
NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MRO[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.

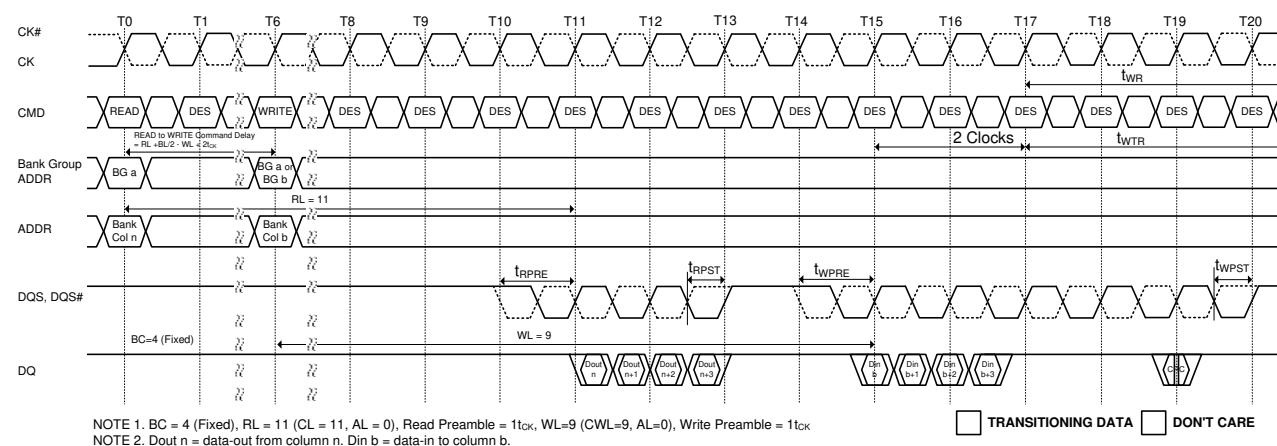
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 123. READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group

## Read to Write with Write CRC

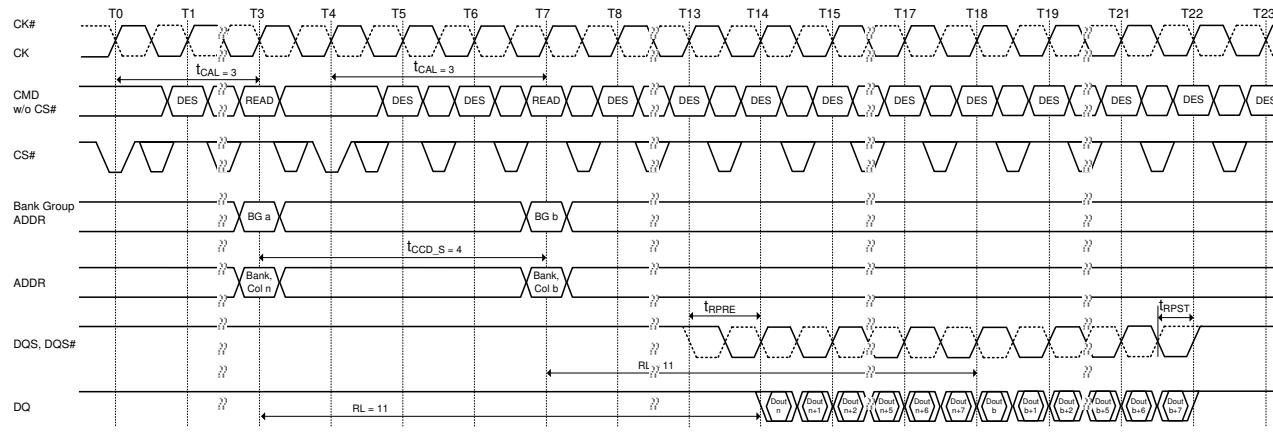


**Figure 124. READ (BL8) to WRITE (BL8 or BC4: OTF) with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**



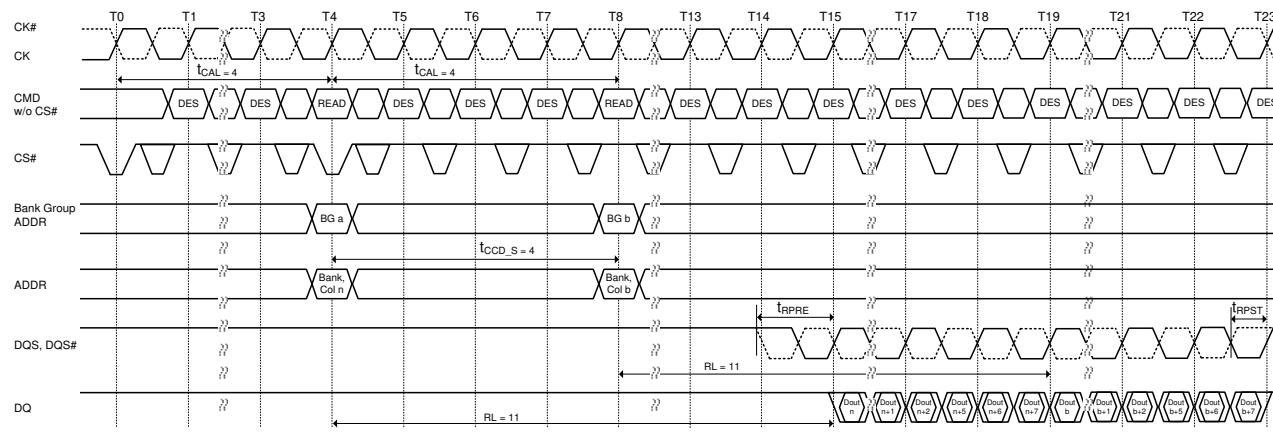
**Figure 125. READ (BC4:Fixed) to WRITE (BC4: Fixed) with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**

## Read to Read with CS to CA Latency



NOTE 1. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1t<sub>CK</sub>  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during READ command at T3 and T7.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.  
 NOTE 6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Figure 126. Consecutive READ (BL8) with CAL(3) and 1t<sub>CK</sub> Preamble in Different Bank Group



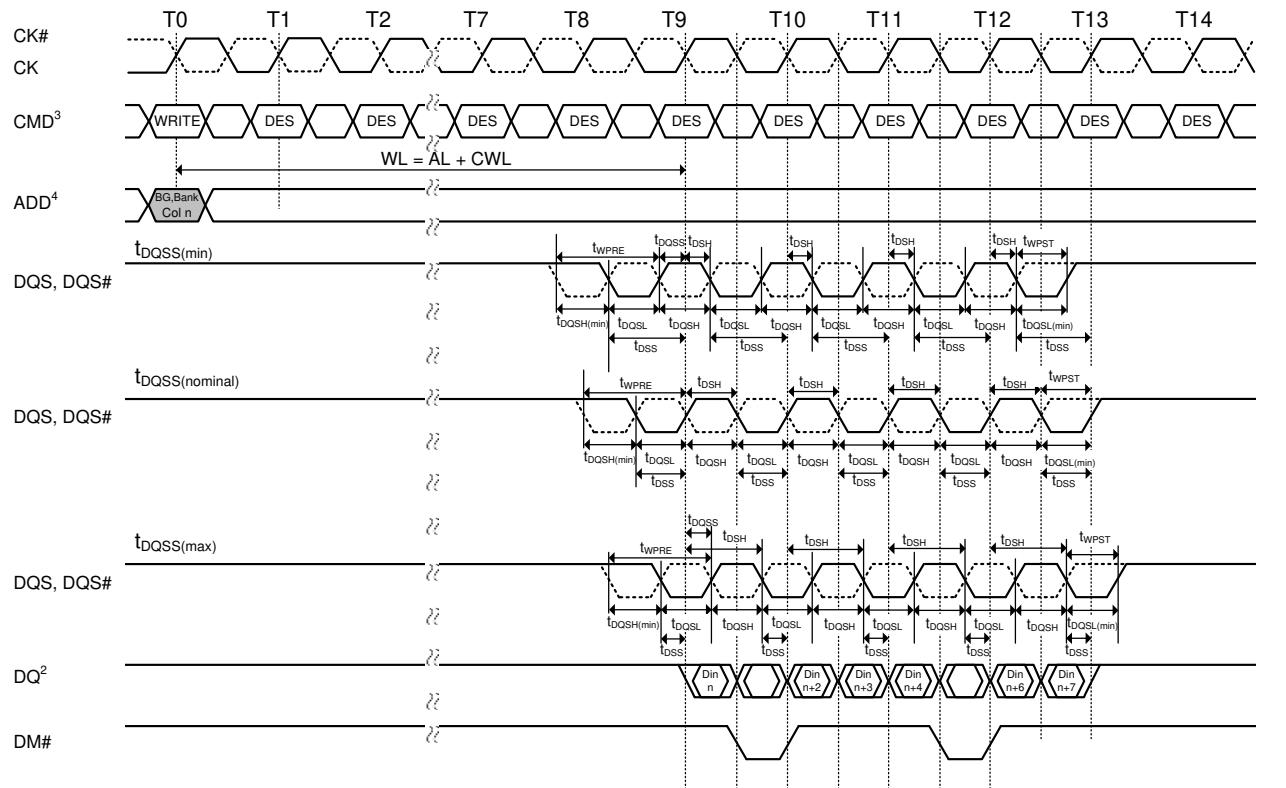
NOTE 1. BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1t<sub>CK</sub>  
 NOTE 2. Dout n (or b) = data-out from column n (or column b).  
 NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.  
 NOTE 5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.  
 NOTE 6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Figure 127. Consecutive READ (BL8) with CAL(4) and 1t<sub>CK</sub> Preamble in Different Bank Group

## Write Operation

## Write Timing Definitions

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).



NOTE 1. BL8, WL = 9 (AL = 0, CWL = 9)

NOTE 2. Dim n = data-in from column n.

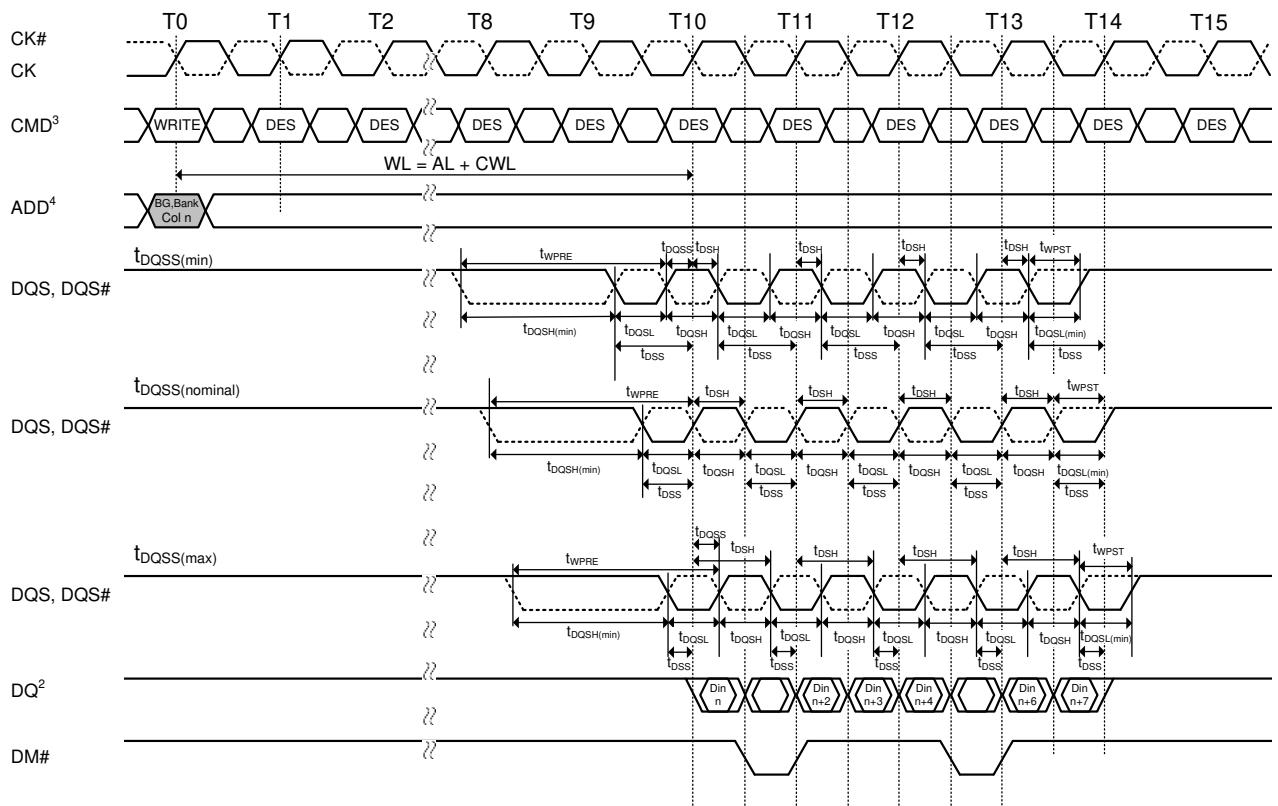
NOTE 3. DES commands are shown for ease of illustration : other commands may be valid at these times.

NOTE 3. BL0 commands are shown for ease of illustration. Other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:0=0] or MRO[A1:0=1] and A12=1 during WRITE command at T0.

NOTE 5.  $t_{POSS}$  must be met at each rising clock edge.

**Figure 128. Write Timing Definition and Parameters with 1t<sub>CK</sub> Preamble**



**Figure 129. Write Timing Definition and Parameters with  $2t_{ck}$  Preamble**

## Write Data Mask

One write data mask (DM#) pin for each 8 data bits (DQ) will be supported on DDR4 SDRAMs, consistent with the implementation on DDR3 SDRAMs. It has identical timings on write operations as the data bits as shown above, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM# is not used during read cycles, however, x16 organization as DBI# during write cycles if enabled by the MR5[A11] setting. For more detail see section "Data Mask (DM), Data Bus Inversion (DBI)".

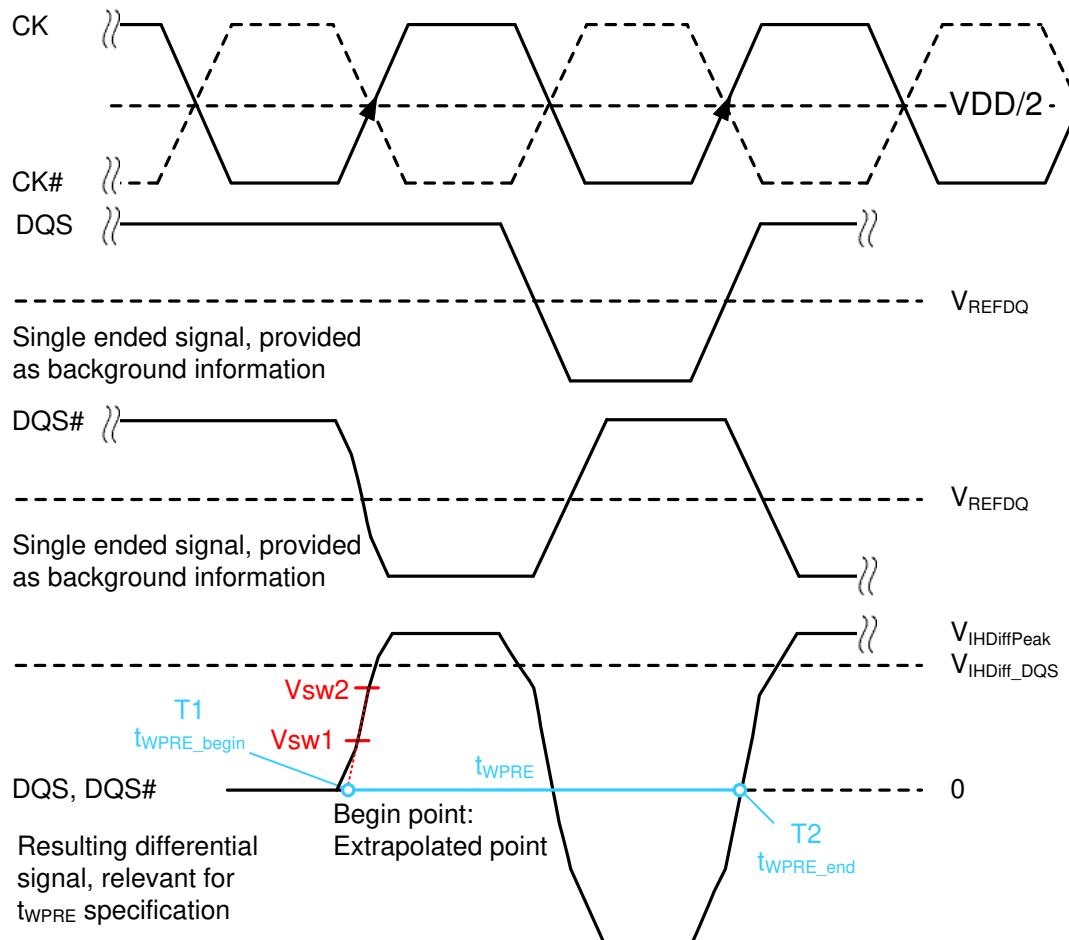


Figure 130. Method for calculating  $t_{WPRE}$  transitions and endpoints

Table 41. Reference Voltage for  $t_{WPRE}$  Timing Measurements

Symbol	Parameter	$V_{sw1}$	$V_{sw2}$	Unit
$t_{WPRE}$	DQS, DQS# differential Write Preamble	$V_{IHDiff\_DQS} \times 0.1$	$V_{IHDiff\_DQS} \times 0.9$	V

The method for calculating differential pulse widths for  $t_{WPRE2}$  is same as  $t_{WPRE}$ .

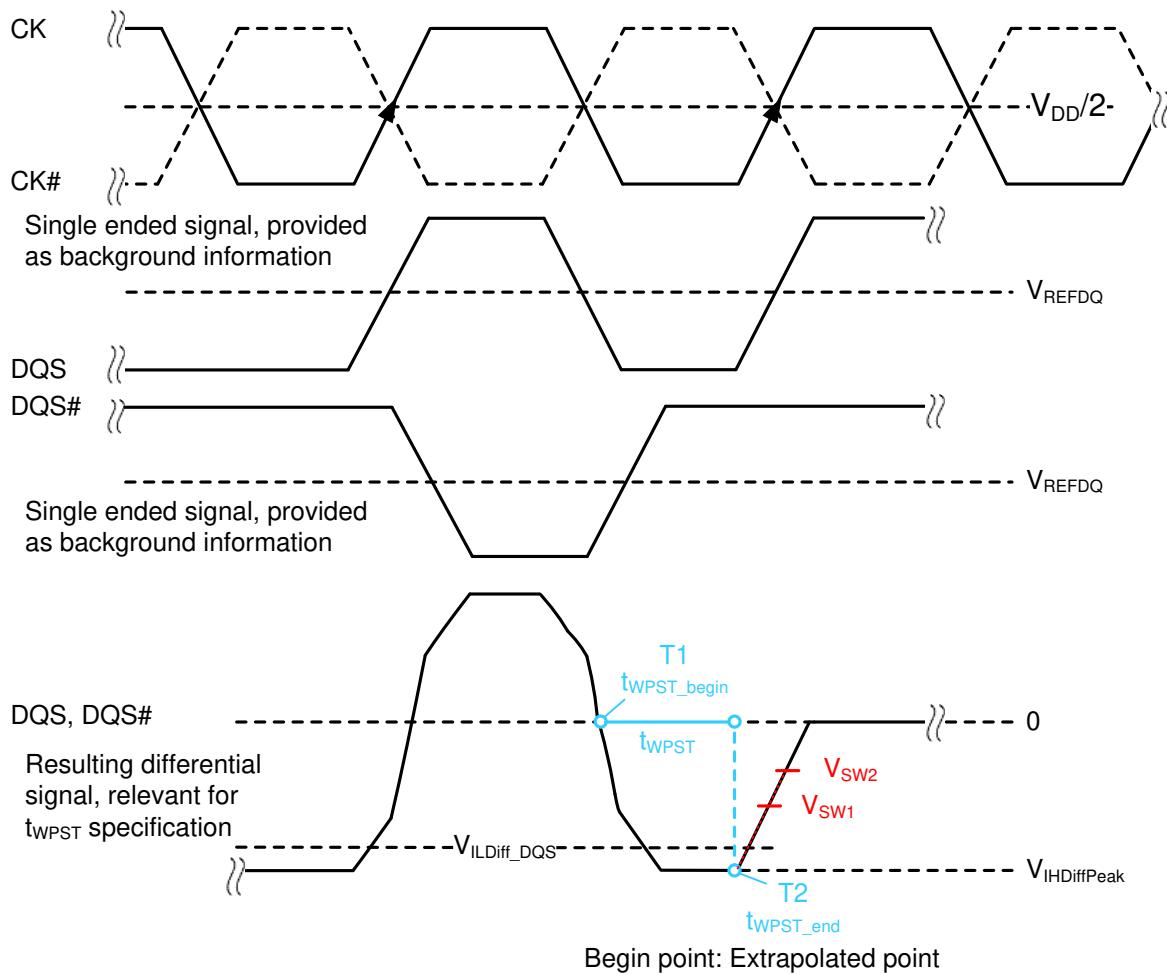


Figure 131. Method for calculating  $t_{WPST}$  transitions and endpoints

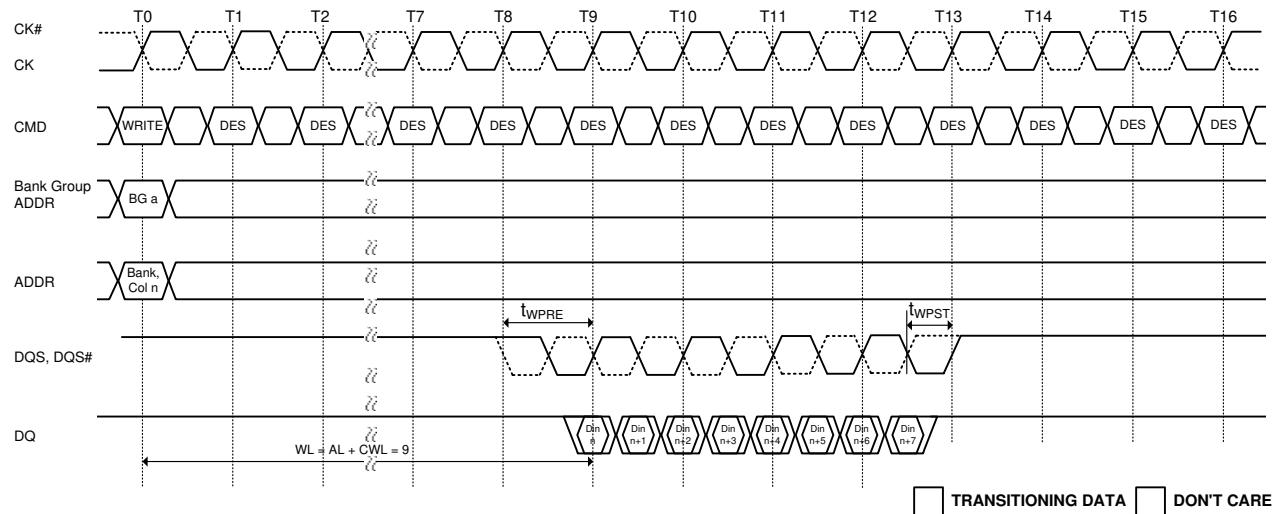
Table 42. Reference Voltage for  $t_{WPST}$  Timing Measurements

Symbol	Parameter	$V_{SW1}$	$V_{SW2}$	Unit
$t_{WPST}$	DQS, DQS# differential Write Postamble	$V_{IHDiffDQS} \times 0.9$	$V_{IHDiffDQS} \times 0.1$	V

## Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1.  $BL = 8$ ,  $WL = 9$ ,  $AL = 0$ ,  $CWL = 9$ , Preamble =  $1t_{CK}$

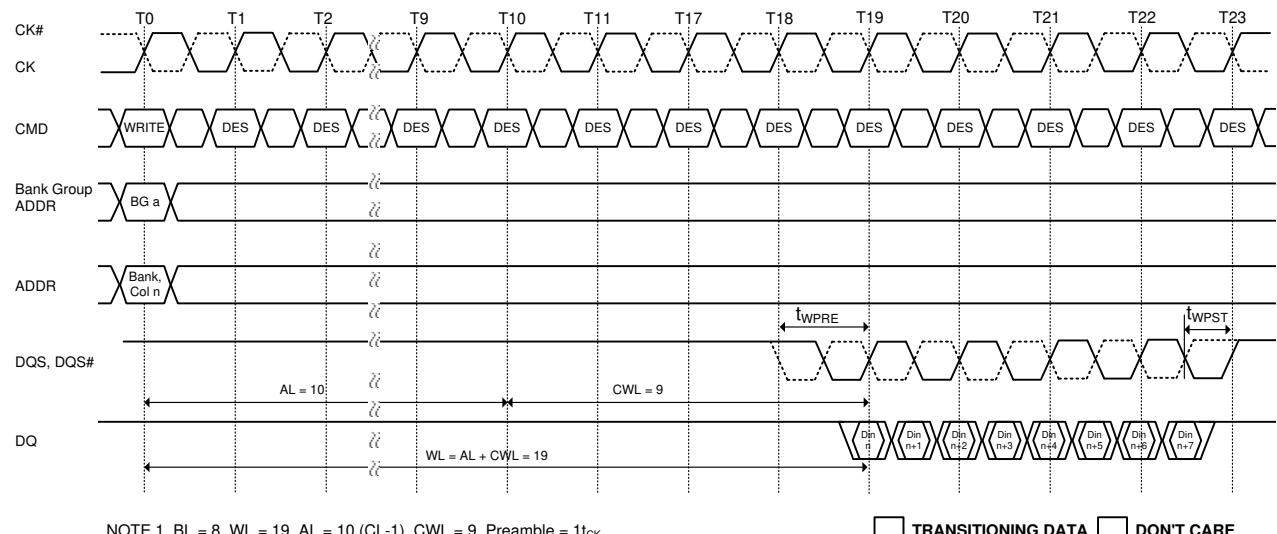
NOTE 2.  $Din n$  = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either  $MRO[A1:A0 = 0:0]$  or  $MRO[A1:A0 = 0:1]$  and  $A12 = 1$  during WRITE command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

**Figure 132. WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)**



NOTE 1.  $BL = 8$ ,  $WL = 19$ ,  $AL = 10$  (CL-1),  $CWL = 9$ , Preamble =  $1t_{CK}$

NOTE 2.  $Din n$  = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either  $MRO[A1:A0 = 0:0]$  or  $MRO[A1:A0 = 0:1]$  and  $A12 = 1$  during WRITE command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

**Figure 133. WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)**

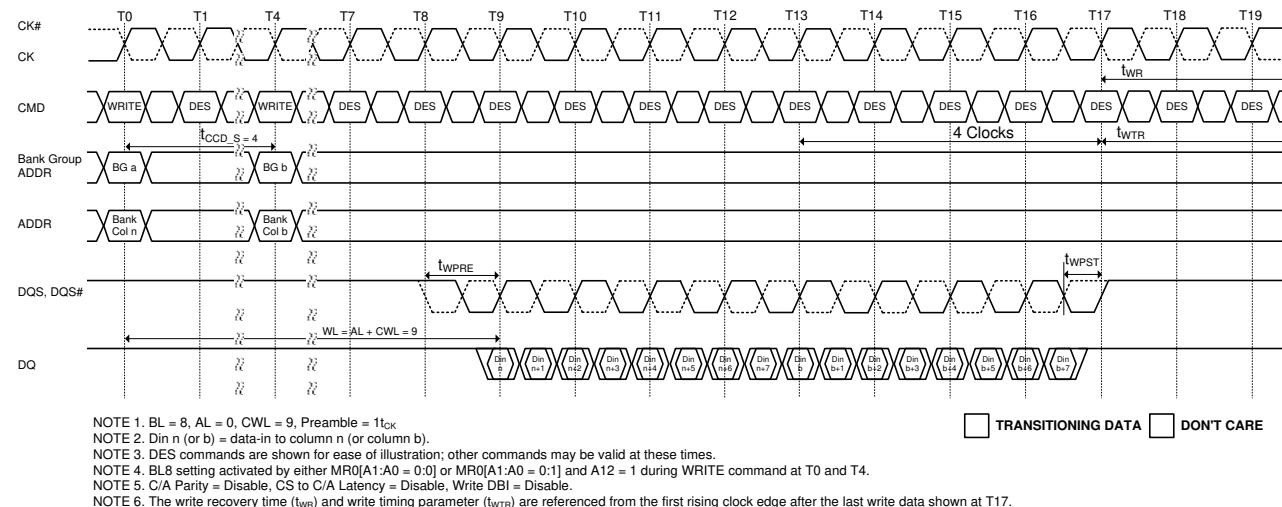


Figure 134. Consecutive WRITE (BL8) with 1t<sub>CK</sub> Preamble in Different Bank Group

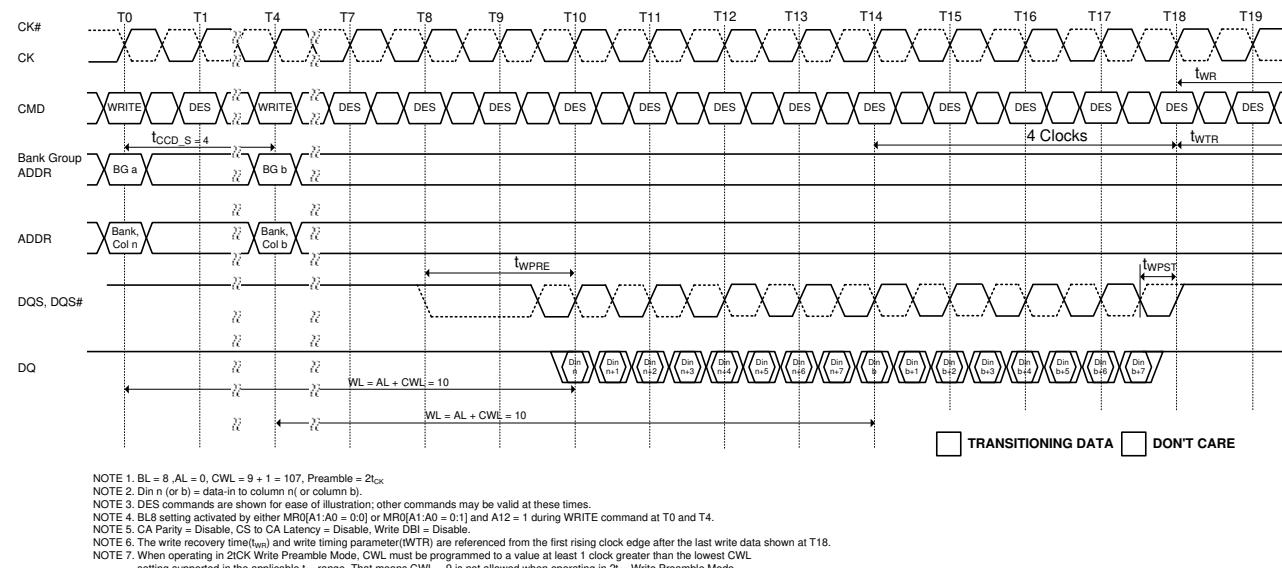


Figure 135. Consecutive WRITE (BL8) with 2t<sub>CK</sub> Preamble in Different Bank Group

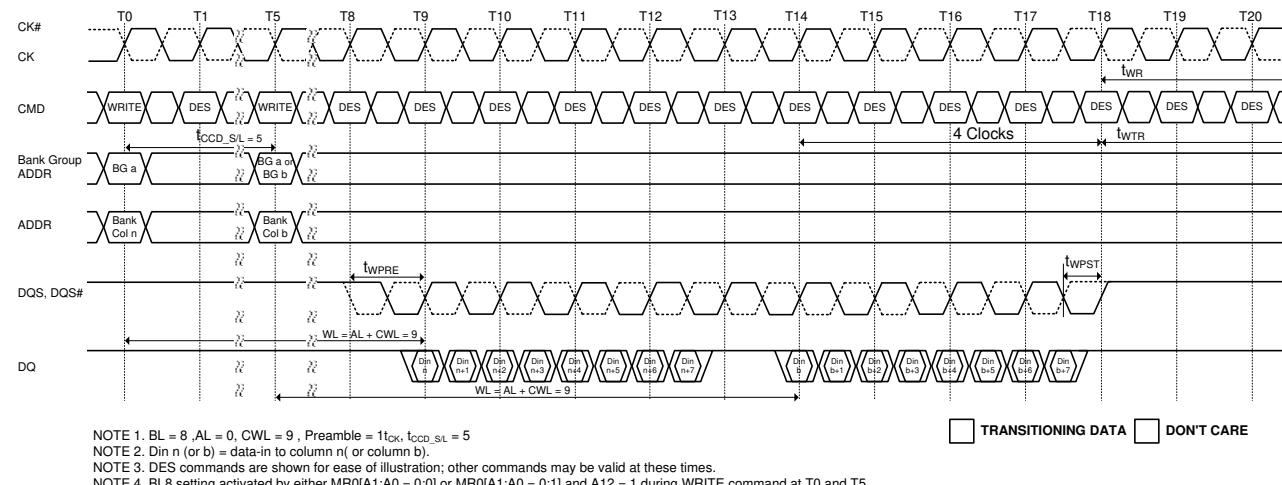


Figure 136. Nonconsecutive WRITE (BL8) with  $1t_{CK}$  Preamble in Same or Different Bank Group

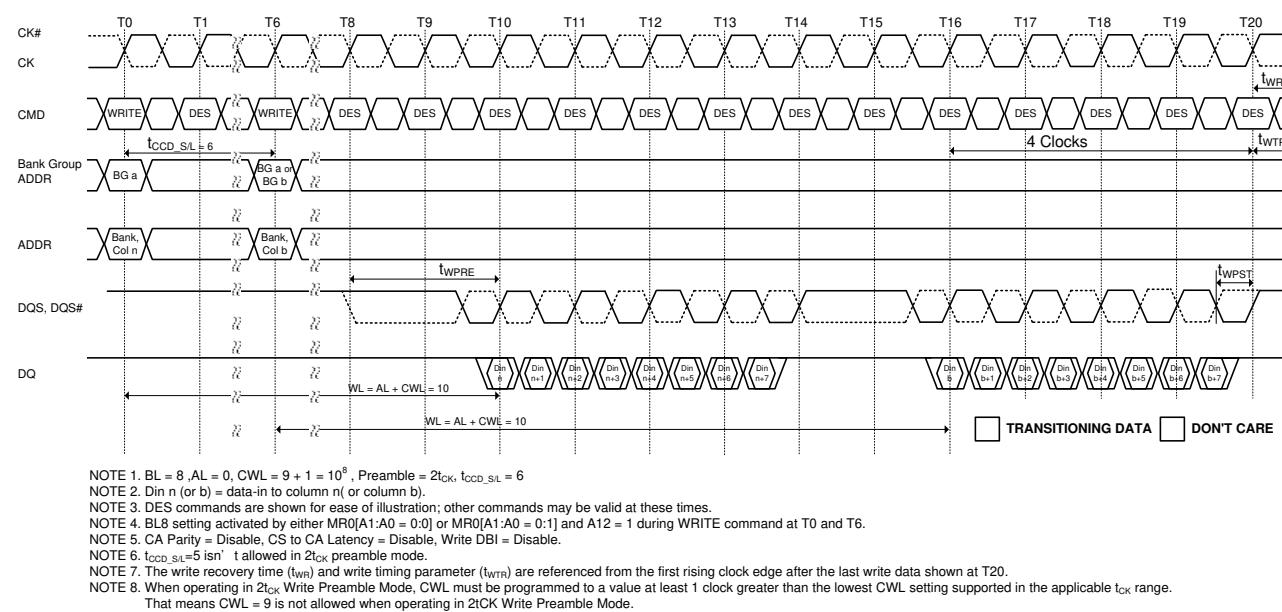


Figure 137. Nonconsecutive WRITE (BL8) with  $2t_{CK}$  Preamble in Same or Different Bank Group

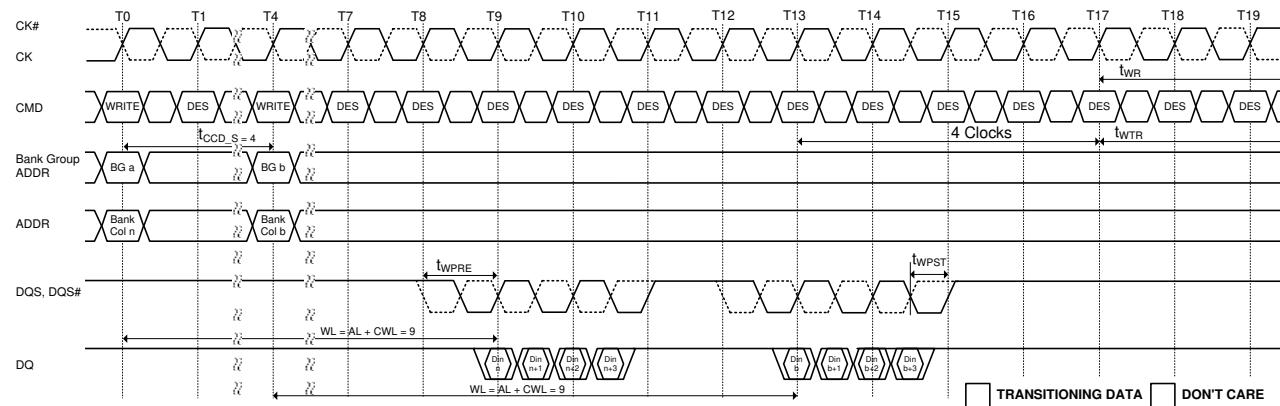


Figure 138. WRITE (BC4) OTF to WRITE (BC4) OTF with  $1t_{CK}$  Preamble in Different Bank Group

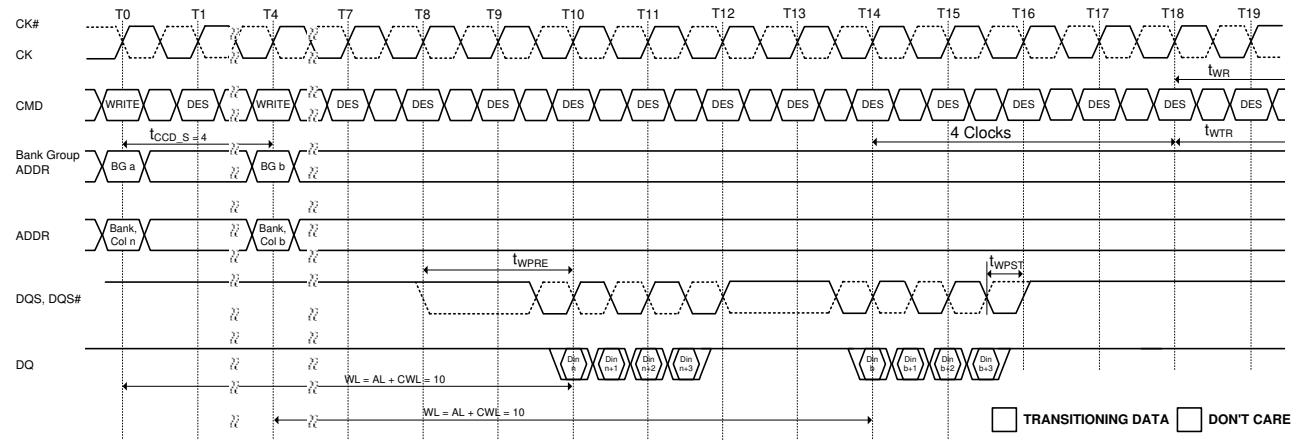
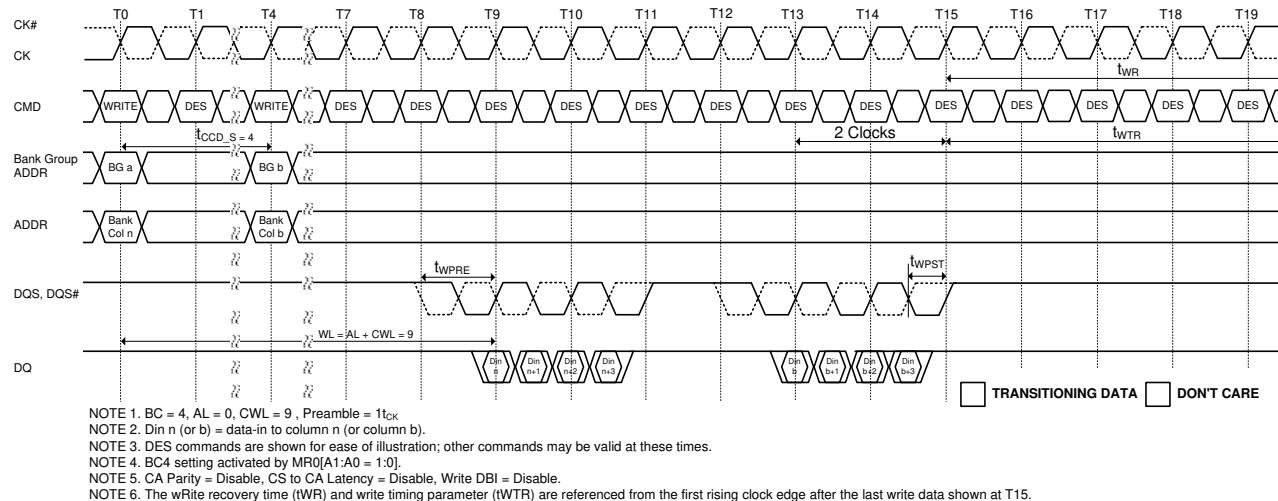
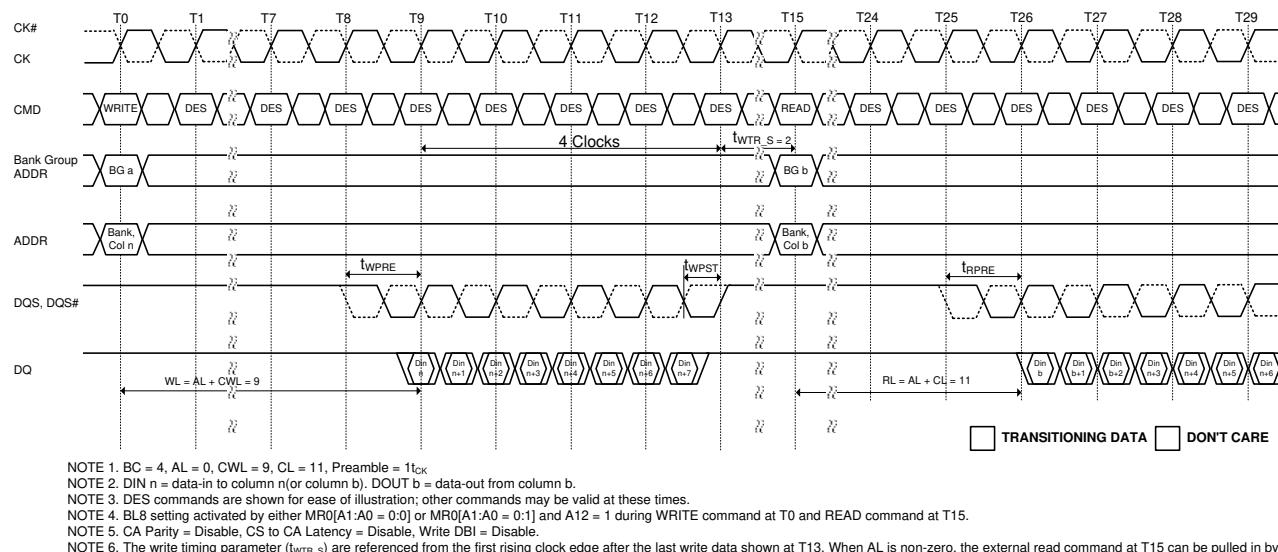


Figure 139. WRITE (BC4) OTF to WRITE (BC4) OTF with  $2t_{CK}$  Preamble in Different Bank Group



**Figure 140. WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1t<sub>CK</sub> Preamble in Different Bank Group**



**Figure 141. WRITE (BL8) to READ (BL8) with 1t<sub>CK</sub> Preamble in Different Bank Group**

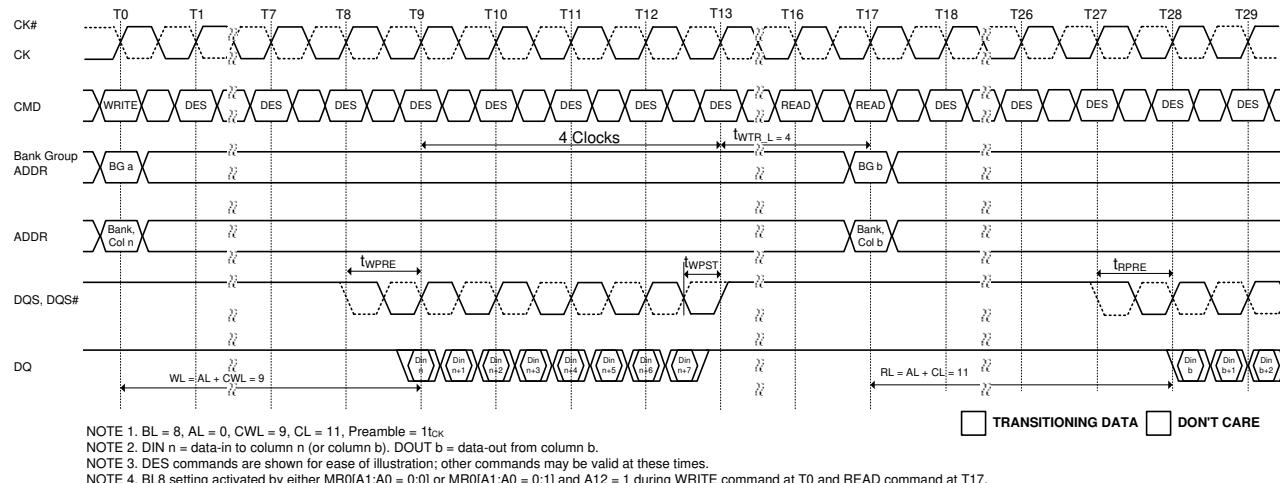
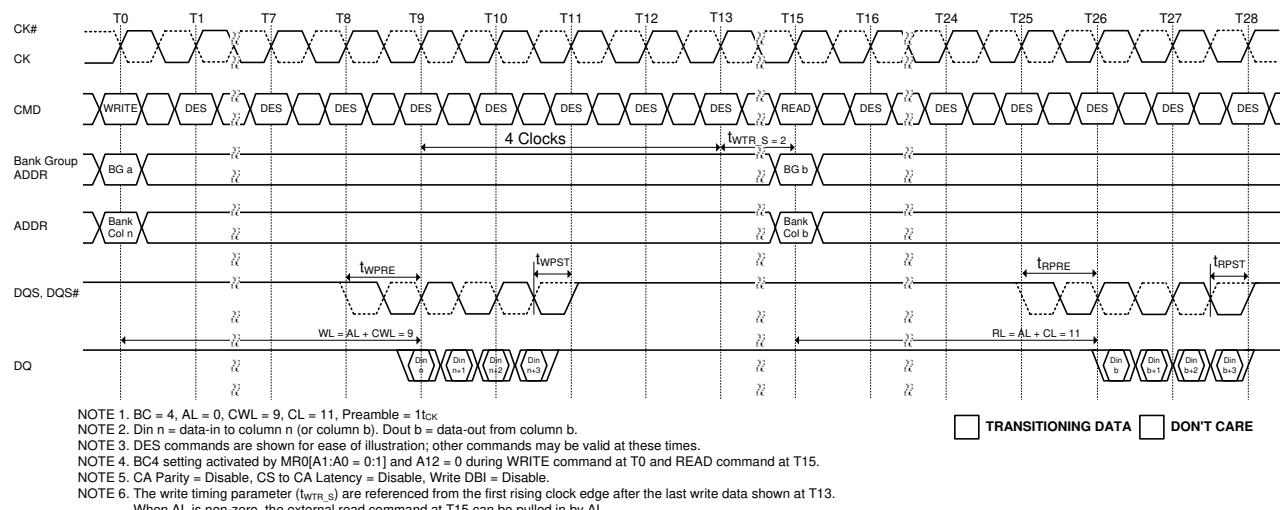
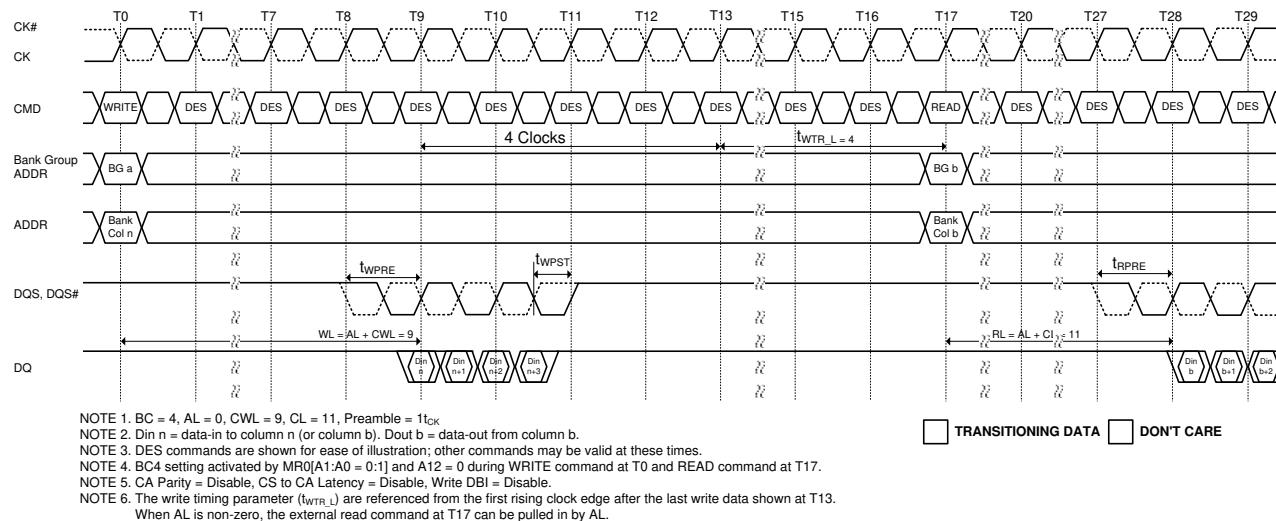


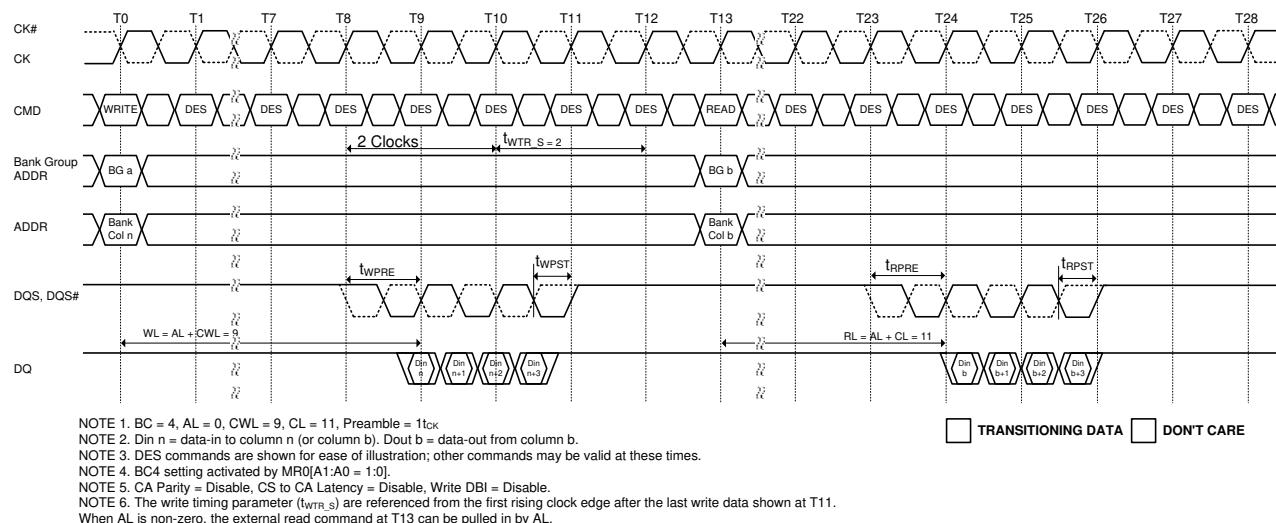
Figure 142. WRITE (BL8) to READ (BL8) with  $1t_{CK}$  Preamble in Same Bank Group



**Figure 143. WRITE (BC4)OTF to READ (BC4)OTF with 1t<sub>CK</sub> Preamble in Different Bank Group**



**Figure 144. WRITE (BC4)OTF to READ (BC4)OTF with 1t<sub>CK</sub> Preamble in Same Bank Group**



**Figure 145. WRITE (BC4)Fixed to READ (BC4)Fixed with 1t<sub>CK</sub> Preamble in Different Bank Group**

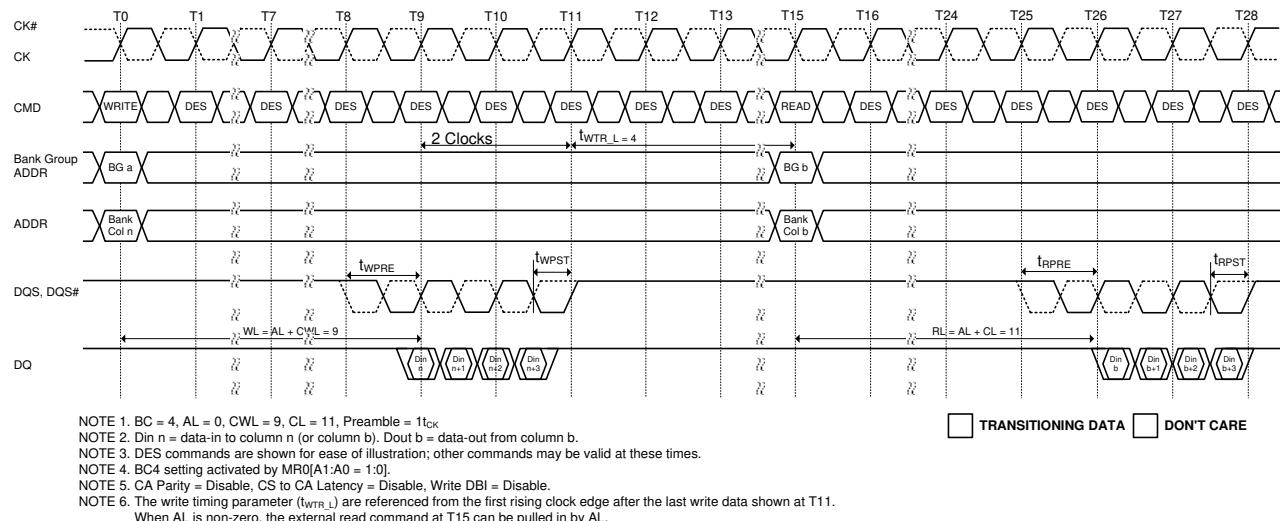


Figure 146. WRITE (BC4)Fixed to READ (BC4)Fixed with 1t<sub>CK</sub> Preamble in Same Bank Group

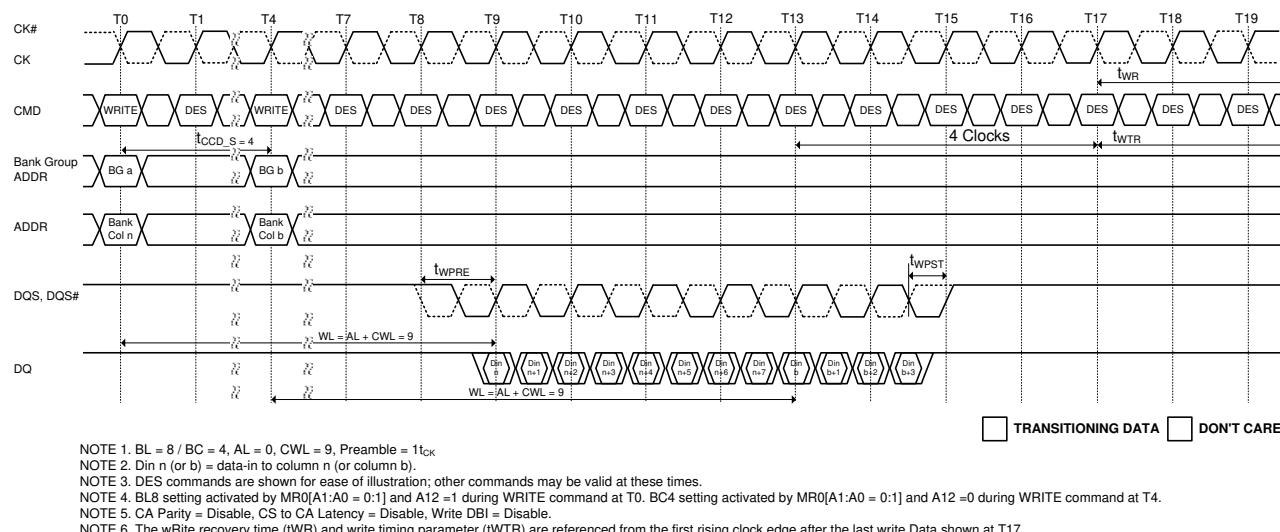


Figure 147. WRITE (BL8) to WRITE (BC4) OTF with 1t<sub>CK</sub> Preamble in Different Bank Group

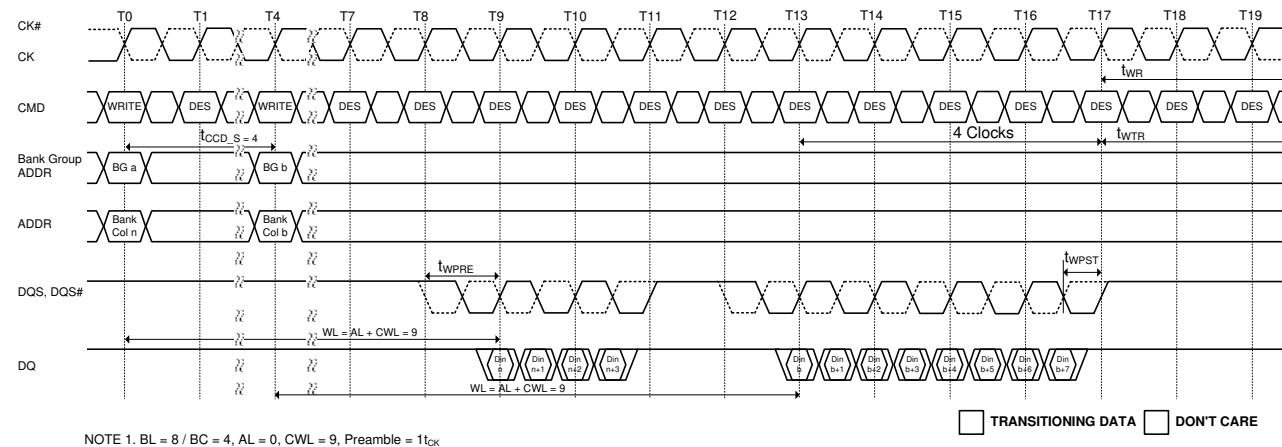


Figure 148. WRITE (BC4)OTF to WRITE (BL8) with  $1t_{CK}$  Preamble in Different Bank Group

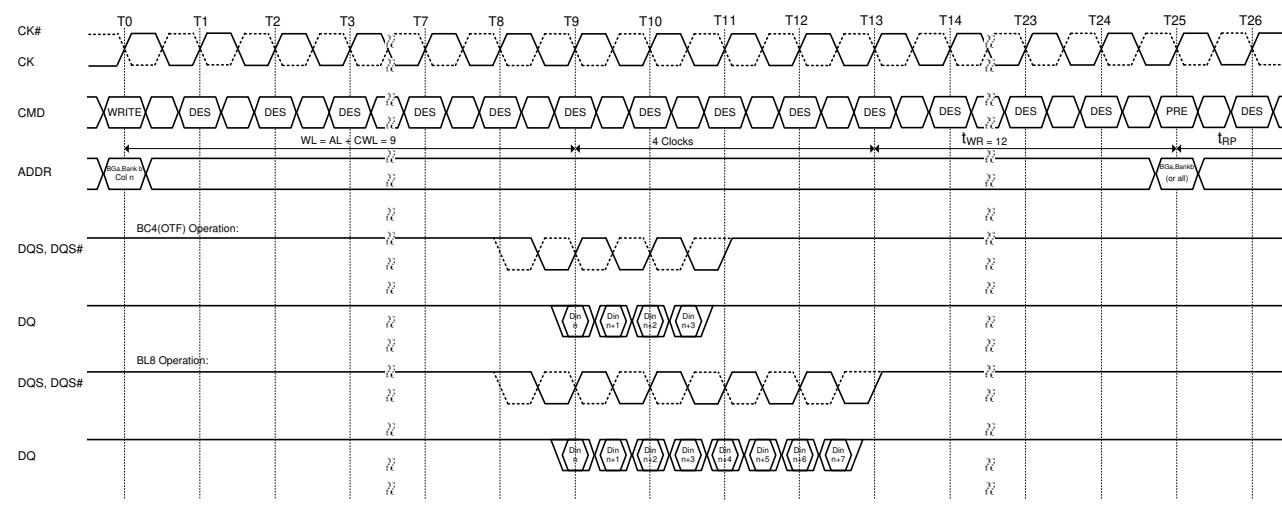
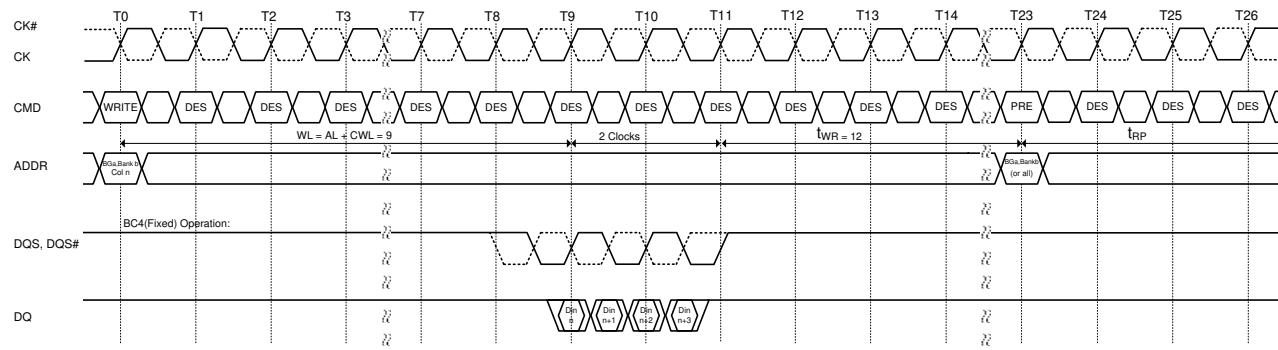


Figure 149. WRITE (BL8/BC4) OTF to PRECHARGE Operation with  $1t_{CK}$  Preamble



NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ ,  $t_{WR} = 12$

NOTE 2.  $Din\ n$  = data-in to column  $n$ .

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 1:0].

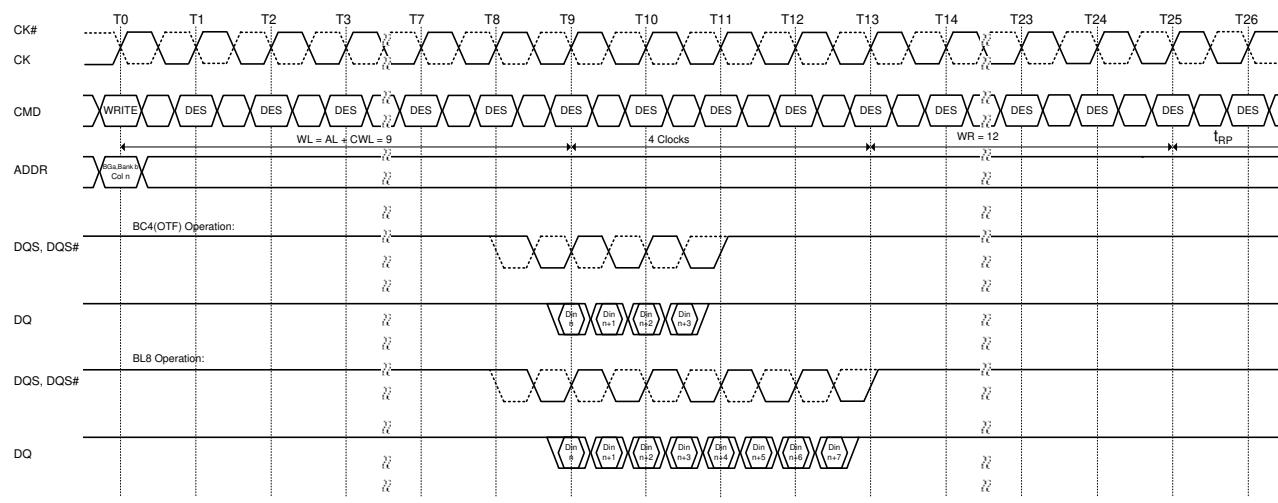
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time ( $t_{WR}$ ) is referenced from the first rising clock edge after the last write data shown at T11.

$t_{WR}$  specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA  DONT CARE

Figure 150. WRITE (BC4) Fixed to PRECHARGE Operation with  $1t_{CK}$  Preamble



NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ , WR = 12

NOTE 2.  $Din\ n$  = data-in to column  $n$ .

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0.

BL8 setting activated by either MRO[A1:0 = 00] or MRO[A1:0 = 01] and A12 = 1 during WRITE command at T0.

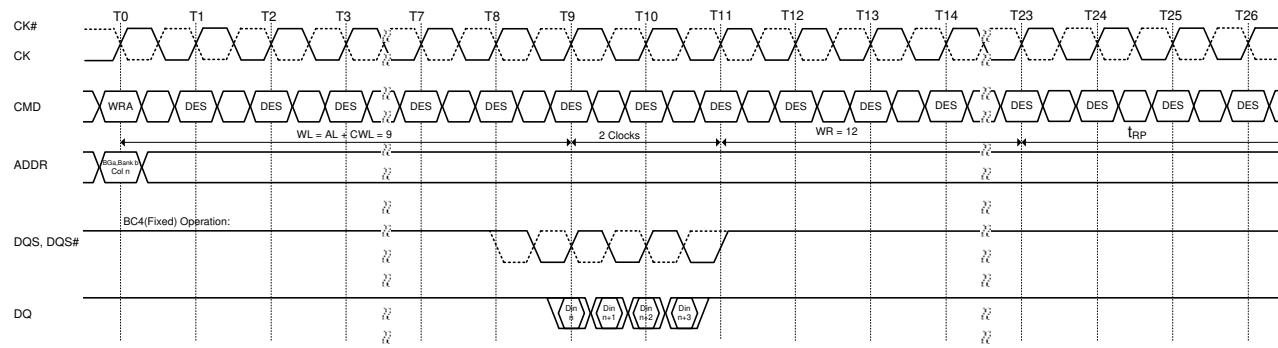
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13.

WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA  DONT CARE

Figure 151. WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and  $1t_{CK}$  Preamble



NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$ , WR = 12

NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 1:0].

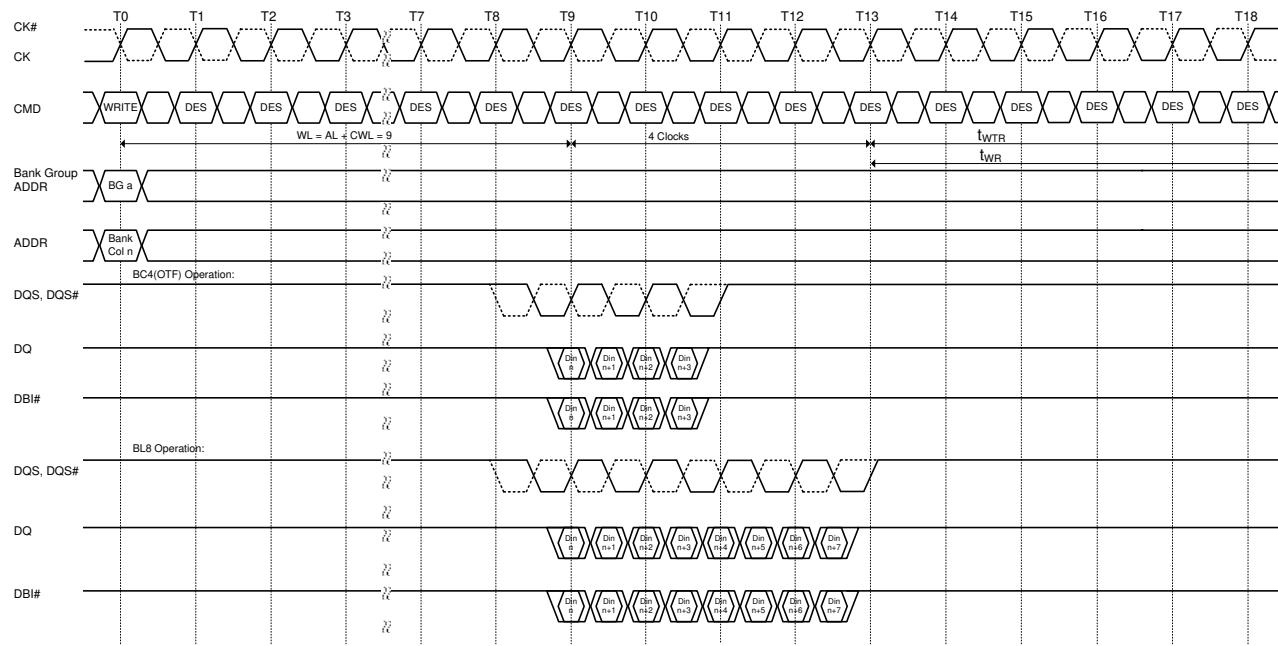
NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time ( $t_{WR}$ ) is referenced from the first rising clock edge after the last write data shown at T11.

WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

TRANSITIONING DATA DON'T CARE

**Figure 152. WRITE (BC4) Fixed with Auto PRECHARGE Operation and  $1t_{CK}$  Preamble**



NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble =  $1t_{CK}$

NOTE 2. Din n = data-in to column n.

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0.

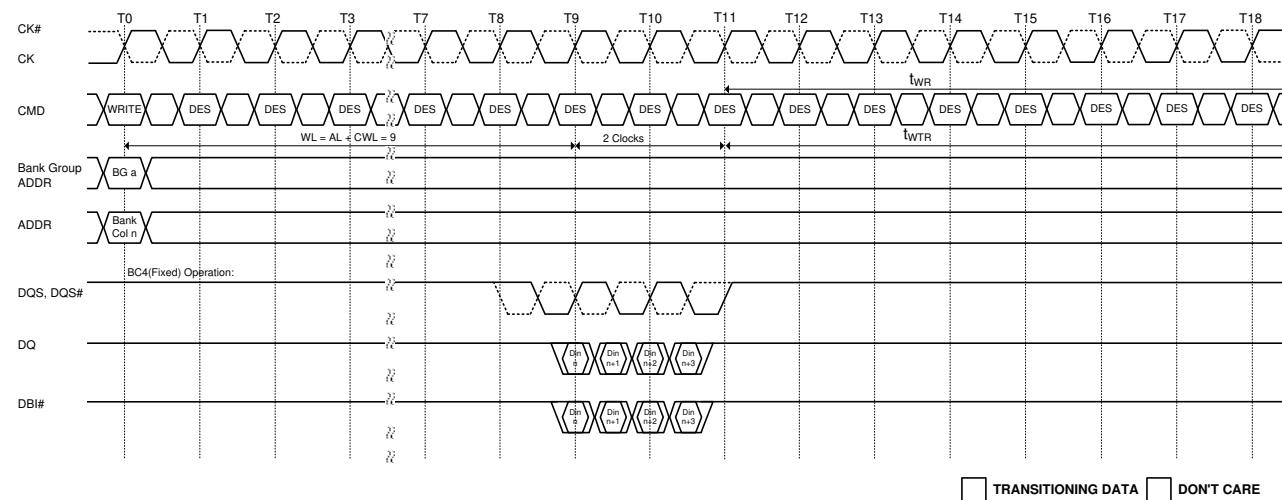
BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6. The write recovery time ( $t_{WR\_DBI}$ ) and write timing parameter ( $t_{WTR\_DBI}$ ) are referenced from the first rising clock edge after the last write data shown at T13.

TRANSITIONING DATA DON'T CARE

**Figure 153. WRITE (BL8/BC4) OTF with  $1t_{CK}$  Preamble and DBI**



NOTE 1. BC = 4, AL = 0, CWL = 9, Preamble = 1t<sub>CK</sub>

NOTE 2. Din n = data-in to column n.

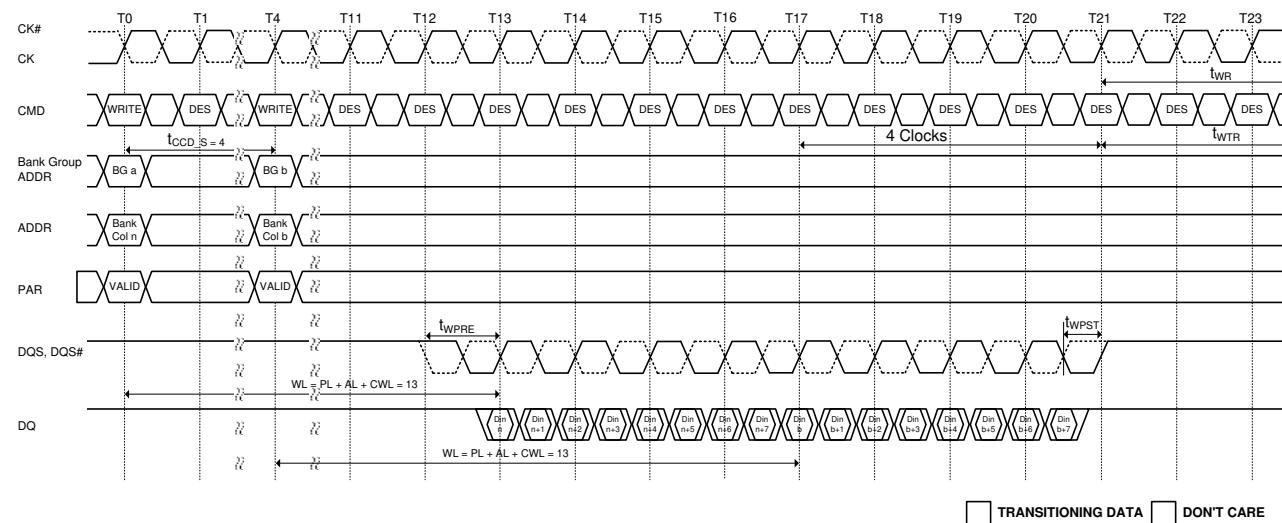
NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BC4 setting activated by MRO[A1:A0 = 1:0].

NOTE 5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 154. WRITE (BC4) Fixed with 1t<sub>CK</sub> Preamble and DBI



NOTE 1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1t<sub>CK</sub>

NOTE 2. Din n (or b) = data-in to column n (or column b).

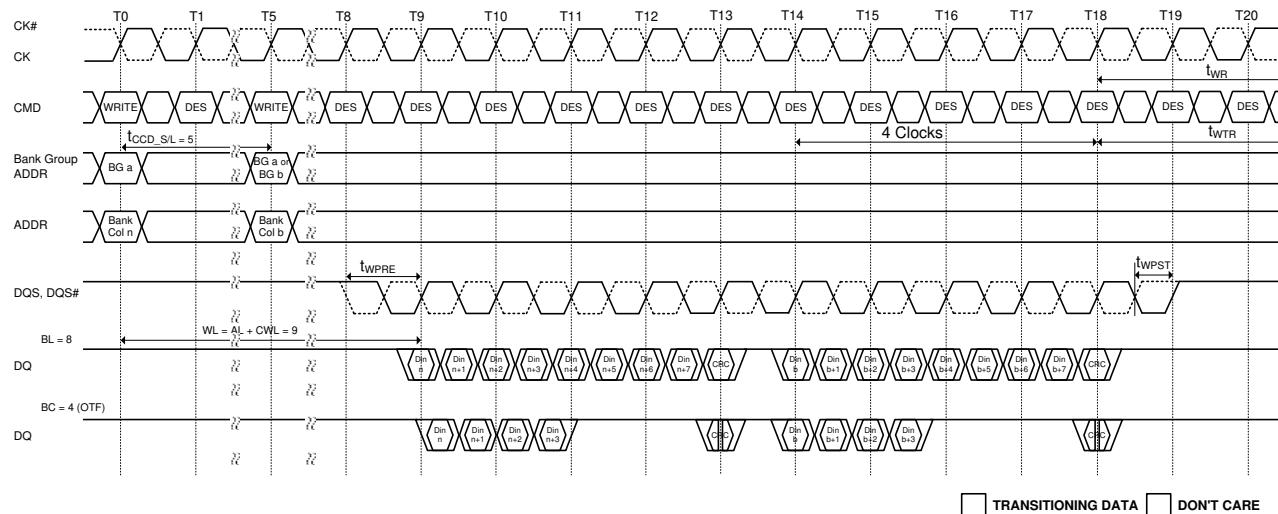
NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.

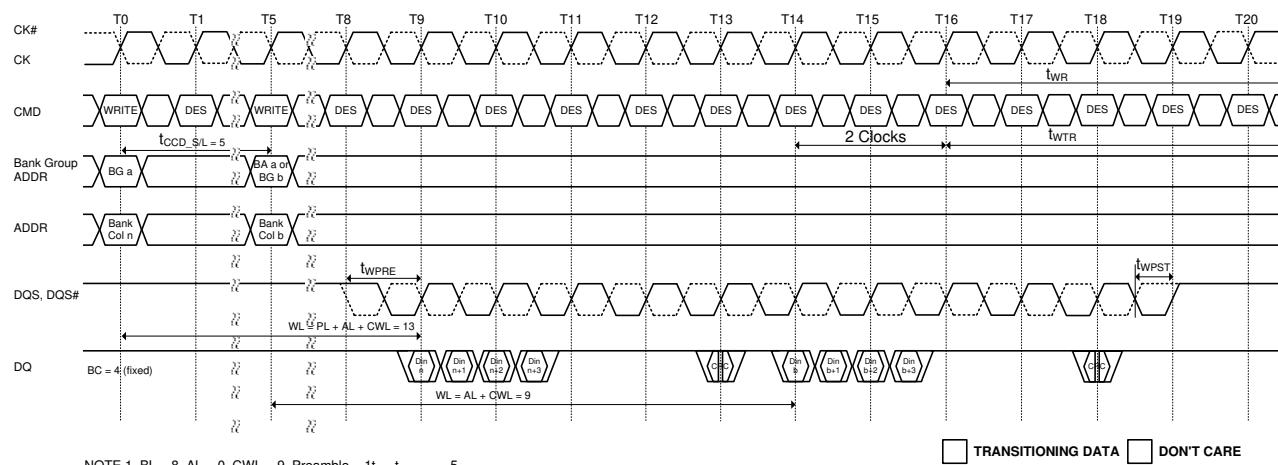
NOTE 5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6. The write recovery time ( $t_{WR}$ ) and write timing parameter ( $t_{WTR}$ ) are referenced from the first rising clock edge after the last write data shown at T21.

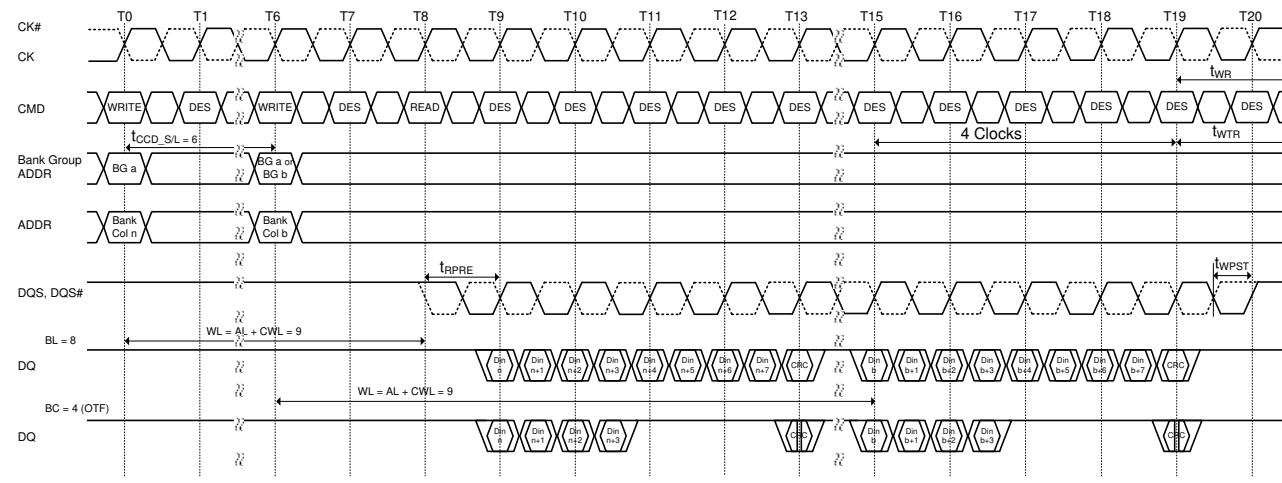
Figure 155. Consecutive WRITE (BL8) with 1t<sub>CK</sub> Preamble and CA Parity in Different Bank Group



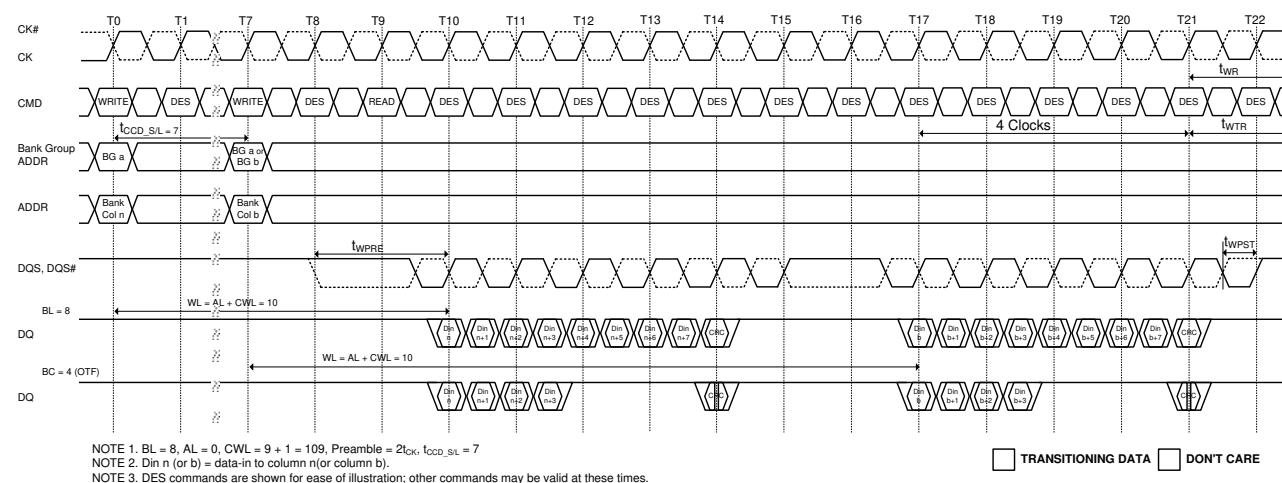
**Figure 156. Consecutive WRITE (BL8/BC4) OTF with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**



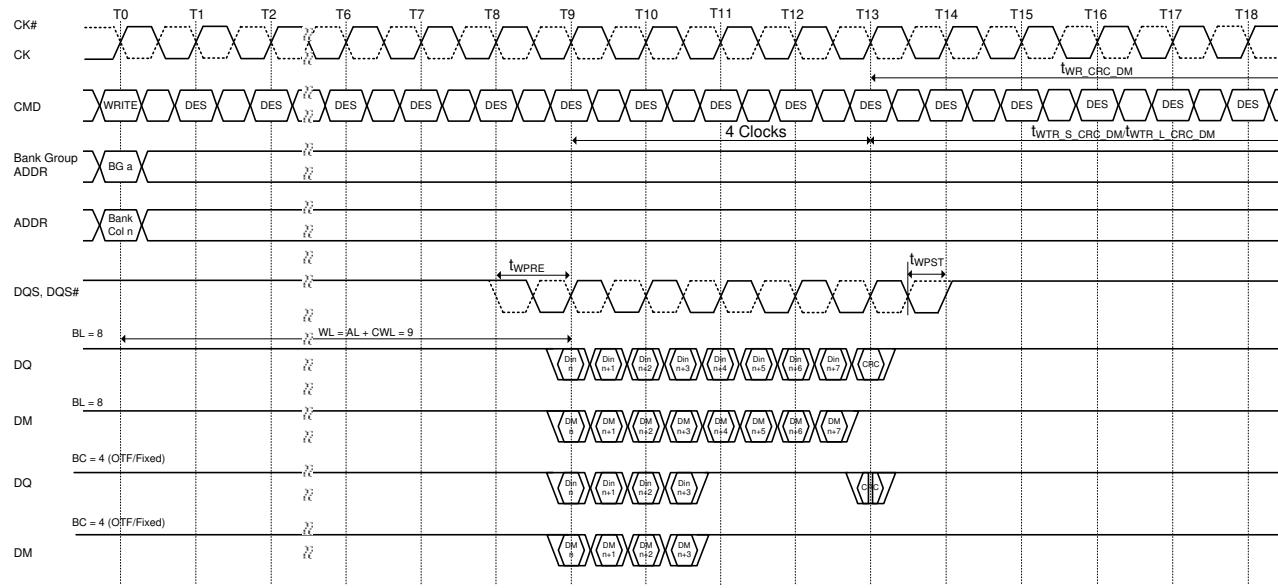
**Figure 157. Consecutive WRITE (BC4) Fixed with 1t<sub>CK</sub> Preamble and Write CRC in Same or Different Bank Group**



**Figure 158. Nonconsecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group**



**Figure 159. Nonconsecutive WRITE (BL8/BC4) OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group**



NOTE 1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tck

NOTE 2.  $Din\ n$  = data-in to column  $n$ .

NOTE 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4. BL8 setting activated by either MRO[A1:A0 = 0:0] or MRO[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5. BC4 setting activated by either MRO[A1:A0 = 1:0] or MRO[A1:A0 = 0:1] and A12 = 0 during READ command at T0.

NOTE 6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.

NOTE 7. The write recovery time ( $t_{WR\_CRC\_DM}$ ) and write timing parameter ( $t_{WR\_S\_CRC\_DM}/t_{WR\_L\_CRC\_DM}$ ) are referenced from the first rising clock edge after the last write data shown at T13.

**Figure 160. WRITE (BL8/BC4) OTF/Fixed with 1t<sub>CK</sub> Preamble and Write CRC and DM in Same or Different Bank Group**

## Read and Write Command Interval

**Table 43. Minimum Read and Write Command Timings**

Bank Group	Access type	Timing Parameter	Note
Same	Minimum Read to Write	CL - CWL + RBL / 2 + 1 t <sub>CCK</sub> + t <sub>WPRE</sub>	1,2
	Minimum Read after Write	CWL + WBL / 2 + t <sub>WTR_L</sub>	1,3
Different	Minimum Read to Write	CL - CWL + RBL / 2 + 1 t <sub>CCK</sub> + t <sub>WPRE</sub>	1,2
	Minimum Read after Write	CWL + WBL / 2 + t <sub>WTR_S</sub>	1,3

Note 1. These timings require extended calibrations times t<sub>ZQinit</sub> and t<sub>ZQcs</sub>.

Note 2. RBL: Read burst length associated with Read command

RBL = 8 for fixed 8 and on-the-fly mode 8

RBL = 4 for fixed BC4 and on-the-fly mode BC4

Note 3. WBL: Write burst length associated with Write command

WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4

WBL = 4 for fixed BC4 only

## Write Timing Violations

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

### **Motivation**

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not "hang up" and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

### **Data Setup and Hold Offset Violations**

Should the data to strobe timing requirements (t<sub>DQS\_off</sub>, t<sub>DQH\_off</sub>, t<sub>DQS\_dd\_off</sub>, t<sub>DQH\_dd\_off</sub>) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory locations addressed with this write command.

In the example (Write Burst Operation WL = 9 (AL = 0, CWL = 9, BL8), the relevant strobe edges for write burst A are associated with the clock edges: T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

### **Strobe and Strobe to Clock Timing Violations**

Should the strobe timing requirements (t<sub>DQSH</sub>, t<sub>DQSL</sub>, t<sub>WPRE</sub>, t<sub>WPST</sub>) or the strobe to clock timing requirements (t<sub>DSS</sub>, t<sub>DSH</sub>, t<sub>DQSS</sub>) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending Write command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

- 1) Both Write CRC and data burst OTF are disabled; timing specifications other than t<sub>DQSH</sub>, t<sub>DQSL</sub>, t<sub>WPRE</sub>, t<sub>WPST</sub>, t<sub>DSS</sub>, t<sub>DSH</sub>, t<sub>DQSS</sub> are not violated.
- 2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.
- 3) A Read command following an offending Write command from any open bank is allowed.
- 4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued t<sub>CCD\_L</sub> later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these Writes may provide incorrect data.
- 5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued t<sub>CCD\_S</sub> later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these Writes may provide incorrect data.
- 6) Once one or more precharge commands(PRE or PREA) are issued to DDR4 after offending write command and all banks become precharged state(idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

## Connectivity Test Mode

### Introduction

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independent of density.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. RESET# is registered to High and  $V_{REFCA}$  must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

### Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR4 memory device are classified as one of the following types:

- 1) Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent; additionally, the DRAM will set the internal  $V_{REFDQ}$  to  $V_{DDQ} \times 0.5$  during CT mode (this is the only time the DRAM takes direct control over setting the internal  $V_{REFDQ}$ ). The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
- 2) Chip Select (CS#) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be tri-stated. The CS# pin in the DDR4 memory device serves as the CS# pin when in CT mode.
- 3) Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.
- 4) Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
- 5) RESET#: Fixed high level is required during CT mode same as normal function.

**Table 44. Pin Classification of DDR4 Memory Device in Connectivity Test (CT) Mode**

CT Mode Pins	Pin Names during Normal Memory Operation	
Test Enable	TEN	
Chip Select	CS#	
Test Input	A	BA0-1, BG0, A0-A9, A10/AP, A12/BC#, A13, WE#/A14, CAS#/A15, RAS#/A16, CKE, ACT#, ODT, CK, CK#, PAR
	B	LDM#/LDBI#, UDM#/UDBI#
	C	ALERT#
	D	RESET#
Test Output	DQ0 – DQ15, LDQS, LDQS#, UDQS, UDQS#	

## Logic Equations --- Min Term Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)  
MT1 = XOR (A8, ALERT#, A9)  
MT2 = XOR (A2, A5, A13)  
MT3 = XOR (A0 A7, A11)  
MT4 = XOR (CK#, ODT, CAS#/A15)  
MT5 = XOR (CKE, RAS#/A16, A10/AP)  
MT6 = XOR (ACT#, A4, BA1)  
MT7 = XOR (x16: UDM#/UDBI#, LDM#/LDBI#, CK)  
MT8 = XOR (WE#/A14, A12/BC#, BA0)  
MT9 = XOR (BG0, A3, RESET# and TEN)

## Output equations for x16 devices

DQ0 = MT0  
DQ1 = MT1  
DQ2 = MT2  
DQ3 = MT3  
DQ4 = MT4  
DQ5 = MT5  
DQ6 = MT6  
DQ7 = MT7  
DQ8 = INV DQ0  
DQ9 = INV DQ1  
DQ10 = INV DQ2  
DQ11 = INV DQ3  
DQ12 = INV DQ4  
DQ13 = INV DQ5  
DQ14 = INV DQ6  
DQ15 = INV DQ7  
LDQS = MT8  
LDQS# = MT9  
UDQSU = INV LDQS  
UDQSU# = INV LDQS#

## Input level and Timing Requirement

During CT Mode, input levels are defined below.

TEN pin: CMOS rail-to-rail with DC high and low at 80% and 20% of  $V_{DD}$

CS#: Pseudo differential signal referring to  $V_{REFCA}$

Test Input pin A: Pseudo differential signal referring to  $V_{REFCA}$

Test Input pin B: Pseudo differential signal referring to internal  $V_{REF}$   $0.5 \times V_{DD}$

RESET#: CMOS DC high above 70 %  $V_{DD}$

ALERT#: Terminated to  $V_{DD}$ . Swing level is TBD

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK and CK# signals will be ignored and the DDR4 memory device enter into the CT mode after  $t_{CT\_Enable}$ . In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on; once the DRAM is initialized and  $V_{REFDQ}$  is calibrated, CT Mode may no longer be used.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within  $t_{CT\_Valid}$  after the test inputs have been applied to the test input pins with TEN input and CS# input maintained High and Low respectively.

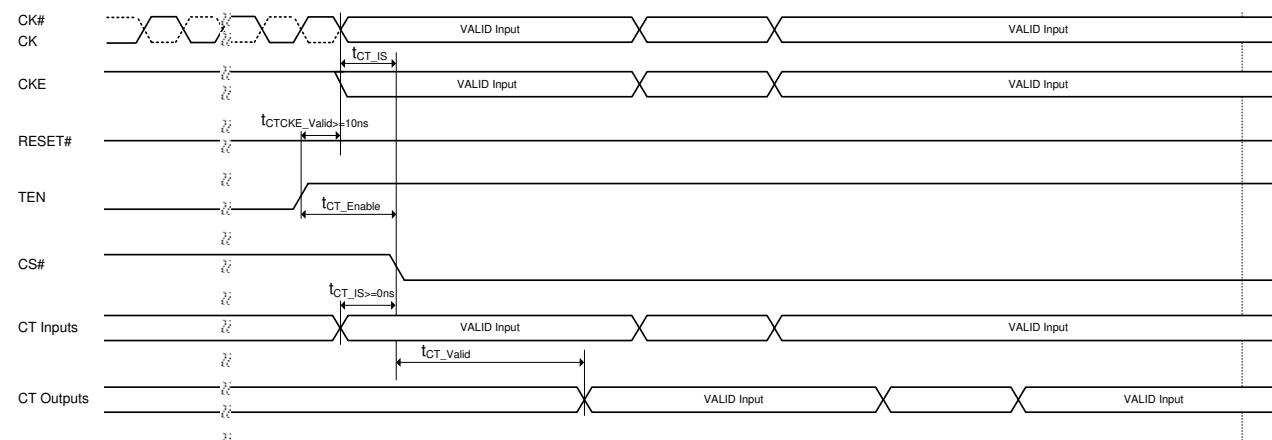


Figure 161. Timing Diagram for Connectivity Test(CT) Mode

Table 45. AC parameters for Connectivity Test (CT) Mode

Symbol	Min.	Max.	Unit
$t_{CT\_IS}$	0	-	ns
$t_{CT\_Enable}$	200	-	ns
$t_{CT\_Valid}$	-	200	ns

## Connectivity Test ( CT ) Mode Input Levels

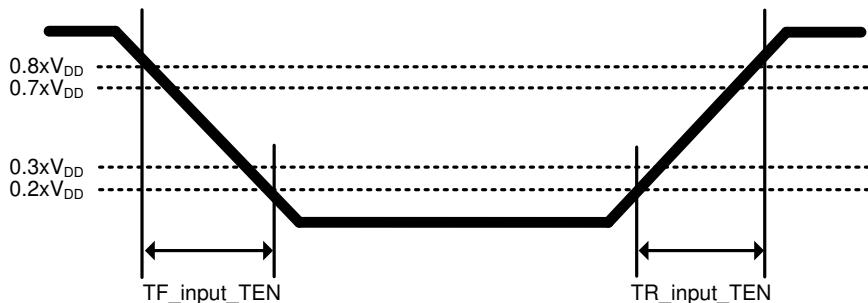
Following input parameters will be applied for DDR4 SDRAM Input Signal during Connectivity Test Mode.

**Table 46. Input Levels for TEN (CMOS)**

Parameter	Symbol	Min.	Max.	Unit	Note
TEN AC Input High Voltage	$V_{IH(AC)}\_TEN$	$0.8 \times V_{DD}$	$V_{DD}$	V	1
TEN DC Input High Voltage	$V_{IH(DC)}\_TEN$	$0.7 \times V_{DD}$	$V_{DD}$	V	
TEN DC Input Low Voltage	$V_{IL(DC)}\_TEN$	$V_{SS}$	$0.3 \times V_{DD}$	V	
TEN AC Input Low Voltage	$V_{IL(AC)}\_TEN$	$V_{SS}$	$0.2 \times V_{DD}$	V	2
TEN Input signal Falling time	$T_{F\_input\_TEN}$	-	10	ns	
TEN Input signal Rising time	$T_{R\_input\_TEN}$	-	10	ns	

Note 1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.

Note 2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.



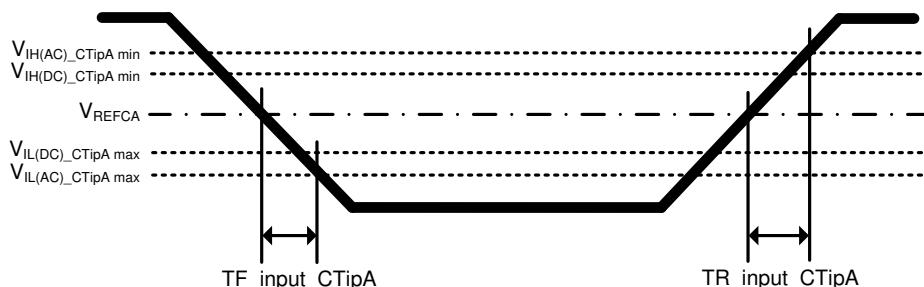
**Figure 162. TEN Input Slew Rate Definition**

**Table 47. CT Type-A Input levels for CS#, BA0-1, BG0, A0-A9, A10/AP, A12/BC#, A13, WE#/A14, CAS#/A15, RAS#/A16, CKE, ACT#, ODT, CK, CK# and PAR**

Parameter	Symbol	Min.	Max.	Unit	Note
CTipA AC Input High Voltage	$V_{IH(AC)}\_CTipA$	$V_{REFCA} + 0.2$	-	V	1
CTipA DC Input High Voltage	$V_{IH(DC)}\_CTipA$	$V_{REFCA} + 0.15$	$V_{DD}$	V	
CTipA DC Input Low Voltage	$V_{IL(DC)}\_CTipA$	$V_{SS}$	$V_{REFCA} - 0.15$	V	
CTipA AC Input Low Voltage	$V_{IL(AC)}\_CTipA$	-	$V_{REFCA} - 0.2$	V	1
CTipA Input signal Falling time	$T_{F\_input\_CTipA}$	-	5	ns	
CTipA Input signal Rising time	$T_{R\_input\_CTipA}$	-	5	ns	

Note 1. See "Overshoot and Undershoot Specifications".

Note 2.  $V_{REFCA} = 0.5 \times V_{DD}$ .



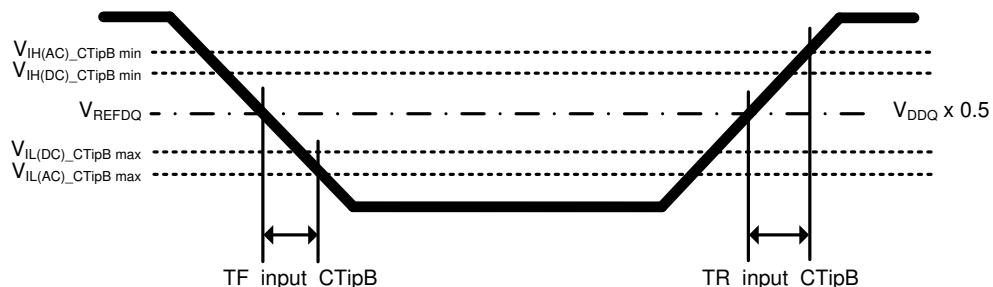
**Figure 163. Input A Slew Rate Definition**

**Table 48. CT Type-B Input levels for LDM#/LDBI#, UDM#/UDBIU#**

Parameter	Symbol	Min.	Max.	Unit	Note
CTipB AC Input High Voltage	$V_{IH(AC)}\_CTipB$	$V_{REFDQ} + 0.3$	-	V	2
CTipB DC Input High Voltage	$V_{IH(DC)}\_CTipB$	$V_{REFDQ} + 0.2$	$V_{DDQ}$	V	
CTipB DC Input Low Voltage	$V_{IL(DC)}\_CTipB$	$V_{SS}$	$V_{REFDQ} - 0.2$	V	
CTipB AC Input Low Voltage	$V_{IL(AC)}\_CTipB$	-	$V_{REFCA} - 0.3$	V	2
CTipB Input signal Falling time	$T_{F\_input\_CTipB}$	-	5	ns	
CTipB Input signal Rising time	$T_{R\_input\_CTipB}$	-	5	ns	

Note 1.  $V_{REFDQ}$  is  $V_{DDQ} \times 0.5$

Note 2. See "Overshoot and Undershoot Specifications".

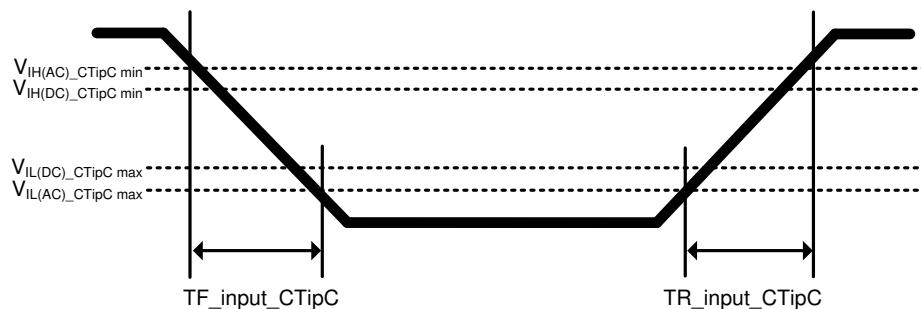


**Figure 164. Input B Slew Rate Definition**

**Table 49. CT Type-C Input levels for ALERT#**

Parameter	Symbol	Min.	Max.	Unit	Note
CTipC AC Input High Voltage	$V_{IH(AC)}\_CTipC$	$0.8 \times V_{DD}$	$V_{DD}$	V	1
CTipC DC Input High Voltage	$V_{IH(DC)}\_CTipC$	$0.7 \times V_{DD}$	$V_{DD}$	V	
CTipC DC Input Low Voltage	$V_{IL(DC)}\_CTipC$	$V_{SS}$	$0.3 \times V_{DD}$	V	
CTipC AC Input Low Voltage	$V_{IL(AC)}\_CTipC$	$V_{SS}$	$0.2 \times V_{DD}$	V	1
CTipC Input signal Falling time	$T_{F\_input\_CTipC}$	-	10	ns	
CTipC Input signal Rising time	$T_{R\_input\_CTipC}$	-	10	ns	

Note 1. See "Overshoot and Undershoot Specifications".



**Figure 165. Input C Slew Rate Definition**

**Table 50. CT Type-D Input levels for RESET#**

RESET# input condition is the same as normal operation.

Parameter	Symbol	Min.	Max.	Unit	Note
CTipD AC Input High Voltage	$V_{IH(AC)}_{CTipD}$	$0.8 \times V_{DD}$	$V_{DD}$	V	4
CTipD DC Input High Voltage	$V_{IH(DC)}_{CTipD}$	$0.7 \times V_{DD}$	$V_{DD}$	V	2
CTipD DC Input Low Voltage	$V_{IL(DC)}_{CTipD}$	$V_{SS}$	$0.3 \times V_{DD}$	V	1
CTipD AC Input Low Voltage	$V_{IL(AC)}_{CTipD}$	$V_{SS}$	$0.2 \times V_{DD}$	V	5
Rising time	$t_{R\_RESET}$	-	1	$\mu S$	3
RESET pulse width - after power-up	$t_{PW\_RESET\_S}$	1	-	$\mu S$	
RESET pulse width - during power-up	$t_{PW\_RESET\_L}$	200	-	$\mu S$	

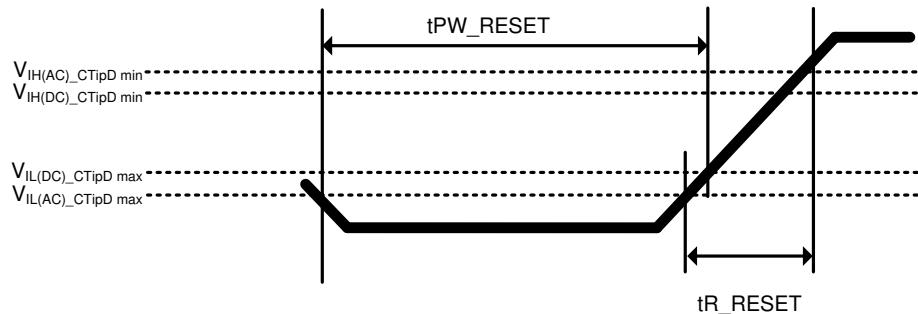
Note 1. After RESET# is registered LOW, the RESET# level must be maintained below  $V_{IL(DC)}_{RESET}$  during  $t_{PW\_RESET}$ , otherwise, the DRAM may not be reset.

Note 2. After RESET# is registered HIGH, the RESET# level must be maintained above  $V_{IH(DC)}_{RESET}$ , otherwise, operation will be uncertain until it is reset by asserting RESET# signal LOW.

Note 3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.

Note 4. Overshoot should not exceed the VIN values in the Absolute Maximum Ratings table.

Note 5. Undershoot should not exceed the VIN values in the Absolute Maximum Ratings table.



**Figure 166. Input D Slew Rate Definition**

## CRC Polynomial and logic equation

The CRC polynomial used by DDR4 is the ATM-8 HEC,  $X^8 + X^2 + X^1 + 1$ .

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

The error coverage from the DDR4 polynomial used is shown in the following table.

**Table 51. CRC Error Detection Coverage**

Error Type	Detection Capability
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

## CRC Combinatorial Logic Equations

```

module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;
NewCRC[0] =
D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0];
NewCRC[1] =
D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] =
D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] =
D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] =
D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] =
D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] =
D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] =
D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];
nextCRC8_D72 = NewCRC;

```

## Write CRC for x4, x8 and x16 devices

The Controller generates the CRC checksum and forms the write data frames as below tables.

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBI# lane if DBI function is enabled.

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the LDBI# and UDBI# lanes if DBI function is enabled.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT# signal if there is a mis-match.

A x8 device has a CRC tree with 72 input bits. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits D[71:64] are '1's.

A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits [D(143:136) and D(71:64)] are '1's.

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

**Table 52. CRC Data Mapping for x4 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

**Table 53. CRC Data Mapping for x8 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
DM#/DBI#	D64	D65	D66	D67	D68	D69	D70	D71	1	1

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].

**Table 54. CRC Data Mapping for x16 Devices, BL8**

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
LDM#/LDBI#	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
UDM#/UDBI#	D136	D137	D138	D139	D140	D141	D142	D143	1	1

## CRC Error Handling

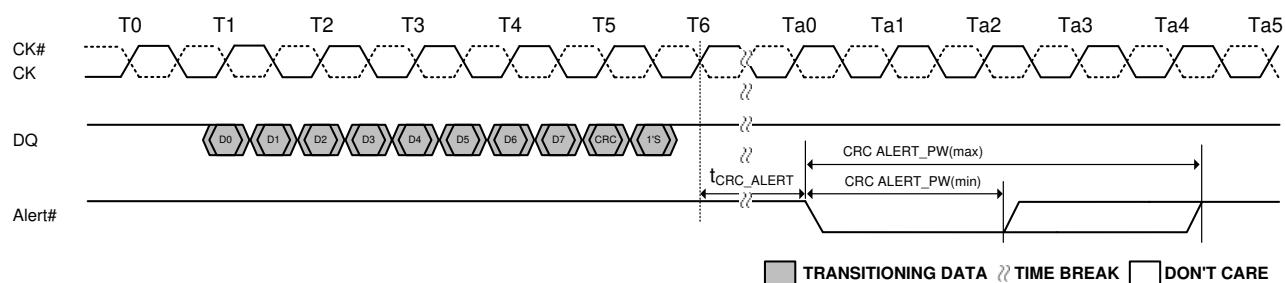
CRC Error mechanism shares the same ALERT# signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is six clocks. The latency to ALERT# signal is defined as  $t_{CRC\_ALERT}$  in the figure below.

DRAM will set CRC Error Clear bit in A3 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for ALERT# (during init) and can back up the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than six clocks at the controller if there are multiple CRC errors as the ALERT# is a daisy chain bus.



NOTE 1. CRC ALERT\_PW is specified from the point Where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.

**Figure 167. CRC Error Reporting**

**Table 55. CRC Error Timing Parameters**

Symbol	Parameter	Min.	Max.	Unit
$t_{CRC\_ALERT}$	CRC error to ALERT# Latency	3	13	ns
CRC ALERT_PW	CRC ALERT_PW	6	10	tck

## CRC Frame Format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

## CRC with BC4 Data Bit Mapping

For a x4 device, the CRC tree inputs are 16 data bits, and the inputs for the remaining bits are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree.

**Table 56. CRC Data Mapping for x4 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7

For a x8 device, the CRC tree inputs are 36 data bits in transfer's four through seven as 1's.

When A2 = 0, the input bits D[67:64]) are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[67:64]) are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree. The input bits D[71:68]) are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[71:68]) are 1.

**Table 57. CRC Data Mapping for x8 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
DM#/DBI#	D64	D65	D66	D67	1	1	1	1	1	1
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
DM#/DBI#	D68	D69	D70	D71	1	1	1	1	1	1

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

When A2 = 0, input bits D[67:64] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[139:136] are 1s.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI# or DM# functions are enabled; if DBI# and DM# are disabled, then D[143:140] are 1s.

**Table 58. CRC Data Mapping for x16 Devices, BC4**

Function	Transfer (A2 = 0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
LDM#/LDBI#	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
UDM#/UDBI#	D136	D137	D138	D139	1	1	1	1	1	1
Function	Transfer (A2 = 1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
LDM#/LDBI#	D68	D69	D70	D71	1	1	1	1	1	1
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
UDM#/UDBI#	D140	D141	D142	D143	1	1	1	1	1	1

Example shown below of CRC tree when X8 is used in BC4 mode, x4 and x16 have similar differences.

### CRC equations for x8 device in BC4 mode with A2=0 are as follows:

$\text{CRC}[0] = D[69]=1 \wedge D[68]=1 \wedge D[67] \wedge D[66] \wedge D[64] \wedge D[63]=1 \wedge D[60]=1 \wedge D[56] \wedge D[54]=1 \wedge D[53]=1 \wedge D[52]=1 \wedge D[50] \wedge D[49] \wedge D[48] \wedge D[45]=1 \wedge D[43] \wedge D[40] \wedge D[39]=1 \wedge D[35] \wedge D[34] \wedge D[31]=1 \wedge D[30]=1 \wedge D[28]=1 \wedge D[23]=1 \wedge D[21]=1 \wedge D[19] \wedge D[18] \wedge D[16] \wedge D[14]=1 \wedge D[12]=1 \wedge D[8] \wedge D[7]=1 \wedge D[6]=1 \wedge D[0];$   
 $\text{CRC}[1] = D[70]=1 \wedge D[66] \wedge D[65] \wedge D[63]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[57] \wedge D[56] \wedge D[55]=1 \wedge D[52]=1 \wedge D[51] \wedge D[48] \wedge D[46]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[43] \wedge D[41] \wedge D[39]=1 \wedge D[36]=1 \wedge D[34] \wedge D[32] \wedge D[30]=1 \wedge D[29]=1 \wedge D[28]=1 \wedge D[24] \wedge D[23]=1 \wedge D[22]=1 \wedge D[21]=1 \wedge D[20]=1 \wedge D[18] \wedge D[17] \wedge D[16] \wedge D[15]=1 \wedge D[14]=1 \wedge D[13]=1 \wedge D[12]=1 \wedge D[9] \wedge D[6]=1 \wedge D[1] \wedge D[0];$   
 $\text{CRC}[2] = D[71]=1 \wedge D[69]=1 \wedge D[68]=1 \wedge D[63]=1 \wedge D[62]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[58] \wedge D[57] \wedge D[54]=1 \wedge D[50] \wedge D[48] \wedge D[47]=1 \wedge D[46]=1 \wedge D[44]=1 \wedge D[43] \wedge D[42] \wedge D[39]=1 \wedge D[37]=1 \wedge D[34] \wedge D[33] \wedge D[29]=1 \wedge D[28]=1 \wedge D[25] \wedge D[24] \wedge D[22]=1 \wedge D[17] \wedge D[15]=1 \wedge D[13]=1 \wedge D[12]=1 \wedge D[10] \wedge D[8] \wedge D[6]=1 \wedge D[2] \wedge D[1] \wedge D[0];$   
 $\text{CRC}[3] = D[70]=1 \wedge D[69]=1 \wedge D[64] \wedge D[63]=1 \wedge D[62]=1 \wedge D[61]=1 \wedge D[59] \wedge D[58] \wedge D[55]=1 \wedge D[51] \wedge D[49] \wedge D[48] \wedge D[47]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[43] \wedge D[40] \wedge D[38]=1 \wedge D[35] \wedge D[34] \wedge D[30]=1 \wedge D[29]=1 \wedge D[26] \wedge D[25] \wedge D[23]=1 \wedge D[18] \wedge D[16] \wedge D[14]=1 \wedge D[13]=1 \wedge D[11] \wedge D[9] \wedge D[7]=1 \wedge D[3] \wedge D[2] \wedge D[1];$   
 $\text{CRC}[4] = D[71]=1 \wedge D[70]=1 \wedge D[65] \wedge D[64] \wedge D[63]=1 \wedge D[62]=1 \wedge D[60]=1 \wedge D[59] \wedge D[56] \wedge D[52]=1 \wedge D[50] \wedge D[49] \wedge D[48] \wedge D[46]=1 \wedge D[45]=1 \wedge D[44]=1 \wedge D[41] \wedge D[39]=1 \wedge D[36]=1 \wedge D[35] \wedge D[31]=1 \wedge D[30]=1 \wedge D[27] \wedge D[26] \wedge D[24] \wedge D[19] \wedge D[17] \wedge D[15]=1 \wedge D[14]=1 \wedge D[12]=1 \wedge D[10] \wedge D[8] \wedge D[4]=1 \wedge D[3] \wedge D[2];$   
 $\text{CRC}[5] = D[71]=1 \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[63]=1 \wedge D[61]=1 \wedge D[60]=1 \wedge D[57] \wedge D[53]=1 \wedge D[51] \wedge D[49] \wedge D[47]=1 \wedge D[46]=1 \wedge D[45]=1 \wedge D[42] \wedge D[40] \wedge D[37]=1 \wedge D[36]=1 \wedge D[32] \wedge D[31]=1 \wedge D[28]=1 \wedge D[27] \wedge D[25] \wedge D[20]=1 \wedge D[18] \wedge D[16] \wedge D[15]=1 \wedge D[13]=1 \wedge D[11] \wedge D[9] \wedge D[5]=1 \wedge D[4]=1 \wedge D[3];$   
 $\text{CRC}[6] = D[67] \wedge D[66] \wedge D[65] \wedge D[64] \wedge D[62]=1 \wedge D[61]=1 \wedge D[58] \wedge D[54]=1 \wedge D[52]=1 \wedge D[51] \wedge D[50] \wedge D[48] \wedge D[47]=1 \wedge D[46]=1 \wedge D[43] \wedge D[41] \wedge D[38]=1 \wedge D[37]=1 \wedge D[33] \wedge D[32] \wedge D[29]=1 \wedge D[28]=1 \wedge D[26] \wedge D[21]=1 \wedge D[19] \wedge D[17] \wedge D[16] \wedge D[14]=1 \wedge D[12]=1 \wedge D[10] \wedge D[6]=1 \wedge D[5]=1 \wedge D[4]=1;$   
 $\text{CRC}[7] = D[68]=1 \wedge D[67] \wedge D[66] \wedge D[65] \wedge D[63]=1 \wedge D[62]=1 \wedge D[59] \wedge D[55]=1 \wedge D[53]=1 \wedge D[52]=1 \wedge D[51] \wedge D[49] \wedge D[48] \wedge D[47]=1 \wedge D[44]=1 \wedge D[42] \wedge D[39]=1 \wedge D[38]=1 \wedge D[34] \wedge D[33] \wedge D[30]=1 \wedge D[29]=1 \wedge D[27] \wedge D[22]=1 \wedge D[20]=1 \wedge D[18] \wedge D[17] \wedge D[15]=1 \wedge D[13]=1 \wedge D[11] \wedge D[7]=1 \wedge D[6]=1 \wedge D[5]=1;$

### CRC equations for x8 device in BC4 mode with A2=1 are as follows:

$\text{CRC}[0] = 1 \wedge 1 \wedge D[71] \wedge D[70] \wedge D[68] \wedge 1 \wedge 1 \wedge D[60] \wedge 1 \wedge 1 \wedge D[54] \wedge D[53] \wedge D[52] \wedge 1 \wedge D[47] \wedge D[44] \wedge 1 \wedge D[39] \wedge D[38] \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[23] \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge D[12] \wedge 1 \wedge 1 \wedge D[4];$   
 $\text{CRC}[1] = 1 \wedge D[70] \wedge D[69] \wedge 1 \wedge 1 \wedge 1 \wedge D[61] \wedge D[60] \wedge 1 \wedge 1 \wedge D[55] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[45] \wedge 1 \wedge 1 \wedge D[38] \wedge D[36] \wedge 1 \wedge 1 \wedge 1 \wedge D[28] \wedge 1 \wedge 1 \wedge 1 \wedge D[22] \wedge D[21] \wedge D[20] \wedge 1 \wedge 1 \wedge 1 \wedge D[13] \wedge 1 \wedge D[5] \wedge D[4];$   
 $\text{CRC}[2] = 1 \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge 1 \wedge D[62] \wedge D[61] \wedge 1 \wedge 1 \wedge D[54] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[46] \wedge 1 \wedge 1 \wedge D[38] \wedge D[37] \wedge 1 \wedge 1 \wedge D[29] \wedge D[28] \wedge 1 \wedge D[21] \wedge 1 \wedge 1 \wedge 1 \wedge D[14] \wedge D[12] \wedge 1 \wedge D[6] \wedge D[5] \wedge D[4];$   
 $\text{CRC}[3] = 1 \wedge 1 \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[63] \wedge D[62] \wedge 1 \wedge D[55] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[47] \wedge D[44] \wedge 1 \wedge D[39] \wedge D[38] \wedge 1 \wedge 1 \wedge D[30] \wedge D[29] \wedge 1 \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge D[15] \wedge D[13] \wedge 1 \wedge D[7] \wedge D[6] \wedge D[5];$   
 $\text{CRC}[4] = 1 \wedge 1 \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[63] \wedge D[60] \wedge 1 \wedge D[54] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[45] \wedge 1 \wedge 1 \wedge D[39] \wedge 1 \wedge 1 \wedge D[31] \wedge D[30] \wedge D[28] \wedge D[23] \wedge D[21] \wedge 1 \wedge 1 \wedge D[14] \wedge D[12] \wedge 1 \wedge D[7] \wedge D[6];$   
 $\text{CRC}[5] = 1 \wedge D[70] \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge 1 \wedge D[61] \wedge 1 \wedge D[55] \wedge D[54] \wedge D[53] \wedge 1 \wedge 1 \wedge 1 \wedge D[46] \wedge D[44] \wedge 1 \wedge 1 \wedge D[36] \wedge 1 \wedge 1 \wedge D[31] \wedge D[29] \wedge 1 \wedge D[22] \wedge D[20] \wedge 1 \wedge 1 \wedge D[15] \wedge D[13] \wedge 1 \wedge 1 \wedge D[7];$   
 $\text{CRC}[6] = D[71] \wedge D[70] \wedge D[69] \wedge D[68] \wedge 1 \wedge 1 \wedge D[62] \wedge 1 \wedge 1 \wedge D[55] \wedge D[54] \wedge D[52] \wedge 1 \wedge 1 \wedge D[47] \wedge D[45] \wedge 1 \wedge 1 \wedge D[37] \wedge D[36] \wedge 1 \wedge 1 \wedge D[30] \wedge D[23] \wedge D[21] \wedge D[20] \wedge 1 \wedge 1 \wedge D[14] \wedge 1 \wedge 1 \wedge 1;$   
 $\text{CRC}[7] = 1 \wedge D[71] \wedge D[70] \wedge D[69] \wedge 1 \wedge 1 \wedge D[63] \wedge 1 \wedge 1 \wedge 1 \wedge D[55] \wedge D[53] \wedge D[52] \wedge 1 \wedge 1 \wedge 1 \wedge D[46] \wedge 1 \wedge 1 \wedge D[38] \wedge D[37] \wedge 1 \wedge 1 \wedge D[31] \wedge 1 \wedge 1 \wedge D[22] \wedge D[21] \wedge 1 \wedge 1 \wedge D[15] \wedge 1 \wedge 1 \wedge 1;$

### Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data. For a x16, when the DRAM detects an error in CRC tree, DDR4 DRAMs may mask all DQs or half the DQs depending upon the specific vendor implementation behavior. Both implementations are valid. For the DDR4 DRAMs that masking half the DQs, DQ0 through DQ7 will be masked if the lower byte. CRC tree had the error and DQ8 through DQ15 will be masked if the upper byte CRC tree had the error.

### Simultaneous MPR Write, Per DRAM Addressability and CRC Functionality

The following combination of DDR4 features are prohibited for simultaneous operation:

- 1) MPR Write and Write CRC (Note: MPR Write is via Address pins)
- 2) Per DRAM Addressability and Write CRC (Note: Only MRS are allowed during PDA and also DQ0 is used for PDA detection)

## Post Package Repair

JEDEC defines two modes of Post Package Repair (PPR): soft Post Package Repair (sPPR) and hard Post Package Repair (hPPR). sPPR is non-persistent so the repair row maybe altered; that is, sPPR is NOT a permanent repair and even though it will repair a row, the repair can be reversed, reassigned via another sPPR, or made permanent via hPPR. Hard Post Package Repair is persistent so once the repair row is assigned for a hPPR address, further PPR commands to a previous hPPR section should not be performed, that is, hPPR is a permanent repair; once repaired, it cannot be reversed. The controller provides the failing row address in the hPPR/sPPR sequence to the device to perform the row repair. hPPR Mode and sPPR Mode may not be enabled at the same time.

The hPPR support is identified via an MPR read from MPR Page 2, MPR0[7] and sPPR support is identified via an MPR read from MPR Page 2, MPR0[6].

The PPR support exceeds the JEDEC minimum requirements; DDR4 DRAMs have at least one row of repair for each bank which is essentially 4 row repairs per BG for a total of 8 repair rows for x16; a 4x increase in repair rows.

JEDEC requires the user to have all sPPR row repair addresses reset and cleared prior to enabling hPPR Mode. This DDR4 PPR does not have this restriction, the existing sPPR row repair addresses are not required to be cleared prior to entering hPPR mode.

Each bank in a BG is PPR independent: sPPR or hPPR issued to a bank will not alter a sPPR row repair existing in a different bank.

### sPPR followed by sPPR to same bank

When PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR. When a subsequent sPPR is issued to the same bank, the previous sPPR repair row will be cleared and used for the subsequent sPPR address as the sPPR operation is non-persistent.

### sPPR followed by hPPR to same bank

When a PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR. When a subsequent hPPR is issued to the same bank, the initial sPPR repair row will be cleared and used for the hPPR address. If a further subsequent PPR (hPPR or sPPR) is issued to the same bank, the further subsequent PPR (hPPR or sPPR) repair row will not clear or overwrite the previous hPPR address as the hPPR operation is persistent.

### hPPR followed by hPPR or sPPR to same bank

When a PPR is issued to a bank for the first time and is a hPPR command, the repair row will be a hPPR. When a subsequent PPR (hPPR or sPPR) is issued to the same bank, the subsequent PPR ( hPPR or sPPR) repair row will not clear or overwrite the initial hPPR address as the initial hPPR is persistent.

## Hard Post Package Repair

All banks must be precharged and idle. DBI and CRC modes must be disabled. Both sPPR and hPPR must be disabled. sPPR is disabled with MR4[5] = 0. hPPR is disabled with MR4[13] = 0, which is the normal state, and hPPR is enabled with MR4[13] = 1, which is the hPPR enabled state. There are two forms of hPPR mode. Both forms of hPPR have the same entry requirement as defined in the sections below. The first command sequence uses a WRA command and supports data retention with a refresh operation except for the bank containing the row that is being repaired; JEDEC has relaxed this requirement and allows BA[0] to be a don't care regarding the banks which are not required to maintain data a refresh operation during hPPR. The second command sequence uses a WR command (a refresh operation can't be performed in this command sequence). The second command sequence doesn't support data retention for the target DRAM.

### hPPR Row Repair - Entry

As stated above, all banks must be precharged and idle. DBI and CRC modes must be disabled, and all timings must be followed as shown in the timing diagram that follows.

All other commands except those listed in the following sequences are illegal.

1. Issue MR4[13] 1 to enter hPPR mode enable.
  - a. All DQ are driven HIGH.
2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by tMOD. The PPR guard key settings are the same whether performing sPPR or hPPR mode.
  - a. Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ, and NOP, are not allowed.
  - b. If the guard key bits are not entered in the required order or interrupted with other MR commands, hPPR will not be enabled, and the programming cycle will result in a NOP.
  - c. When the hPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
  - d. JEDEC allows A6:0 to be "Don't Care" on 4Gb and 8Gb devices from a supplier perspective and the user should rely on vendor datasheet.

**Table 59. PPR MR0 Guard Key Sequences**

Guard Keys	BG1:0 <sup>(1)</sup>	BA1:0	A16:A12	A11	A10	A9	A8	A7	A6:A0
1 <sup>st</sup> MR0	00	00	xxxxxx	1	1	0	0	1	1111111
2 <sup>nd</sup> MR0	00	00	xxxxxx	0	1	1	1	1	1111111
3 <sup>rd</sup> MR0	00	00	xxxxxx	1	0	1	1	1	1111111
4 <sup>th</sup> MR0	00	00	xxxxxx	0	0	1	1	1	1111111

Note 1. BG1 is 'Don't Care' in x16

### hPPR Row Repair – WRA Initiated (REF Commands Allowed)

1. Issue an ACT command with failing BG and BA with the row address to be repaired.
2. Issue a WRA command with BG and BA of failing row address.
  - a. The address must be at valid levels, but the address is "Don't Care."
3. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL PL) in order for hPPR to initiate repair.
  - a. Repair will be initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW. The bank under repair does not get the REFRESH command applied to it.
  - b. Repair will not be initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.  
\* JEDEC states: All DQs of target DRAM should be LOW for 4tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than 2tCK, then hPPR mode execution is unknown.
  - c. DQS should function normally.
4. REF command may be issued anytime after the WRA command followed by WL + 4nCK + tWR + tRP.
  - a. Multiple REF commands are issued at a rate of tREFI or tREFI/2, however back-to-back REF commands must be separated by at least tREFI/4 when the DRAM is in hPPR mode.
  - b. All banks except the bank under repair will perform refresh.

5. Issue PRE after tPGM time so that the device can repair the target row during tPGM time.
  - a. Wait tPGM\_Exit after PRE to allow the device to recognize the repaired target row address.
6. Issue MR4[13] 0 command to hPPR mode disable.
  - a. Wait tPGMPST for hPPR mode exit to complete.
  - b. After tPGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

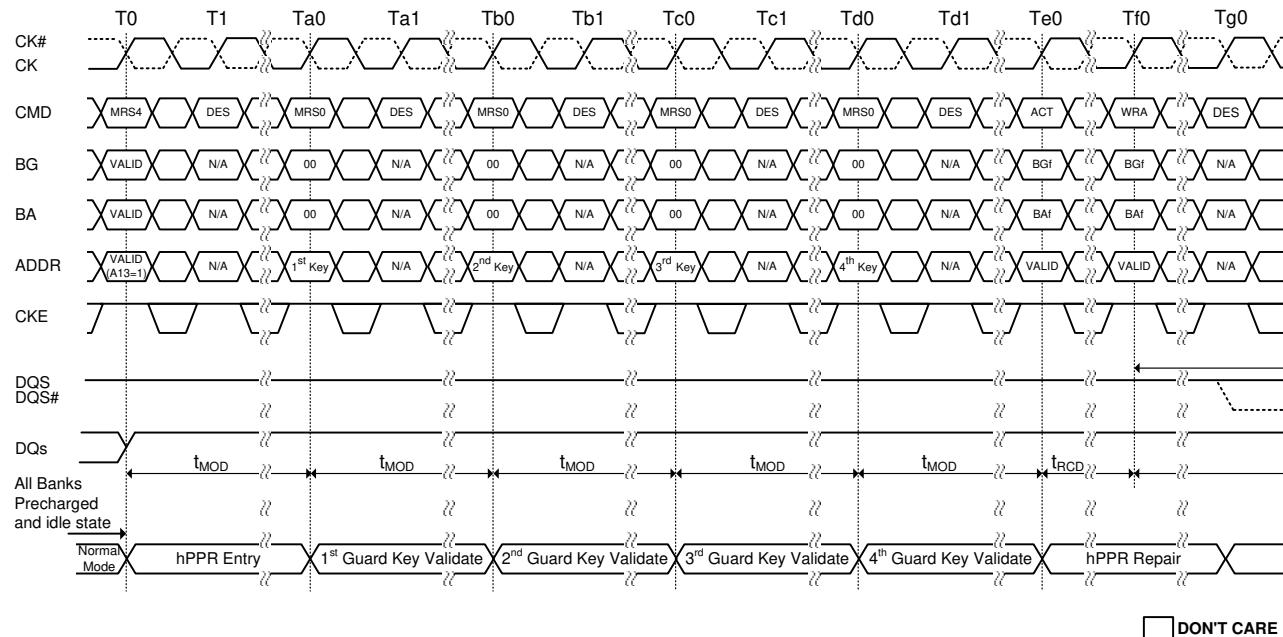


Figure 168. hPPR WRA – Entry

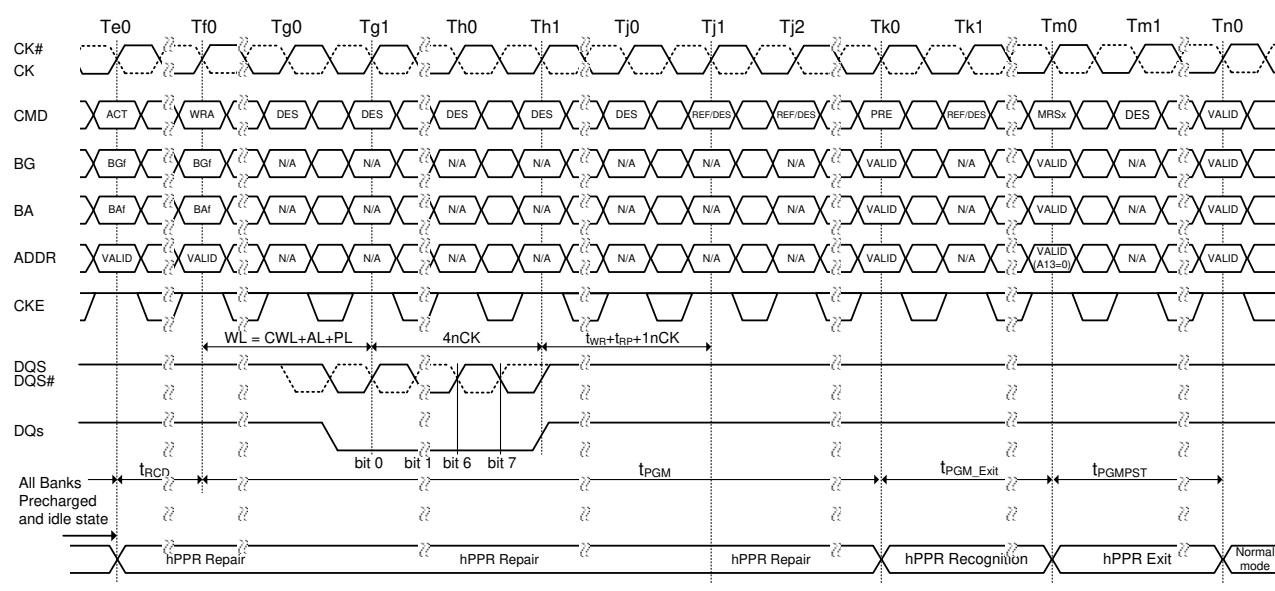


Figure 169. hPPR WRA – Repair and Exit

## hPPR Row Repair – WR Initiated (REF Commands NOT Allowed)

1. Issue an ACT command with failing BG and BA with the row address to be repaired.
2. Issue a WR command with BG and BA of failing row address.
  - a. The address must be at valid levels, but the address is "Don't Care."
3. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for hPPR to initiate repair.
  - a. Repair will be initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
  - b. Repair will not be initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.

\* JEDEC states: All DQs of target DRAM should be LOW for 4tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than 2tCK, then hPPR mode execution is unknown.
- c. DQS should function normally.
4. REF commands may NOT be issued at anytime while in PPT mode.
5. Issue PRE after tPGM time so that the device can repair the target row during tPGM time.
  - a. Wait tPGM\_Exit after PRE to allow the device to recognize the repaired target row address.
6. Issue MR4[13] 0 command to hPPR mode disable.
  - a. Wait tPGMPST for hPPR mode exit to complete.
  - b. After tPGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

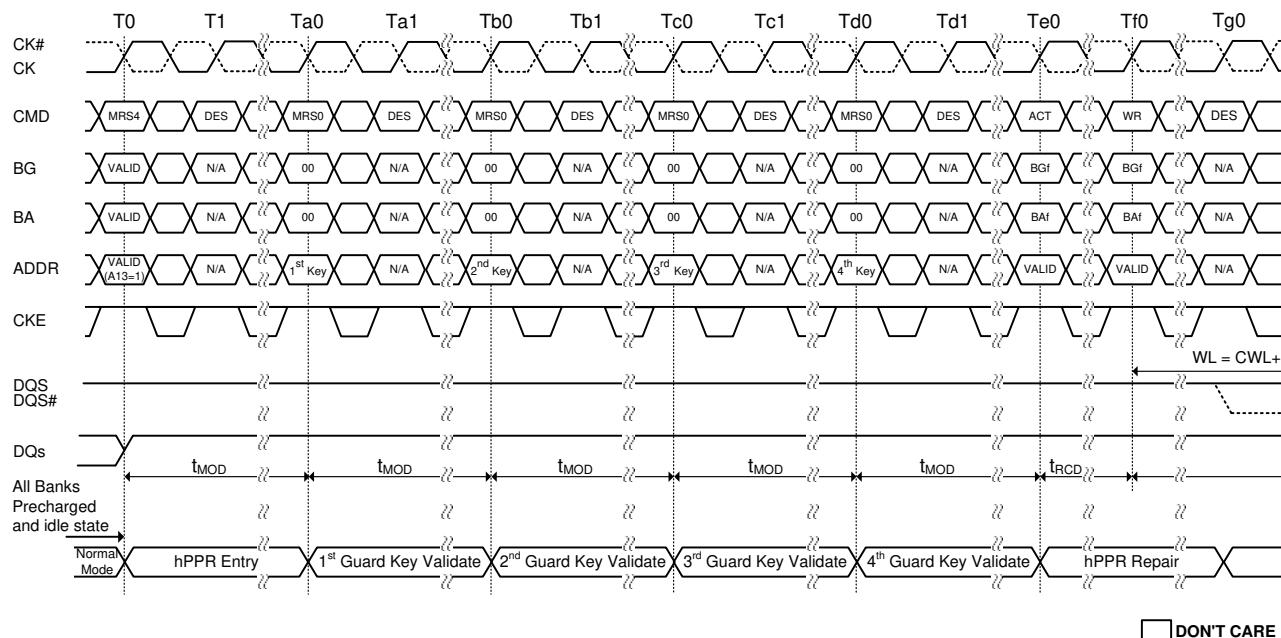


Figure 170. hPPR WR – Entry

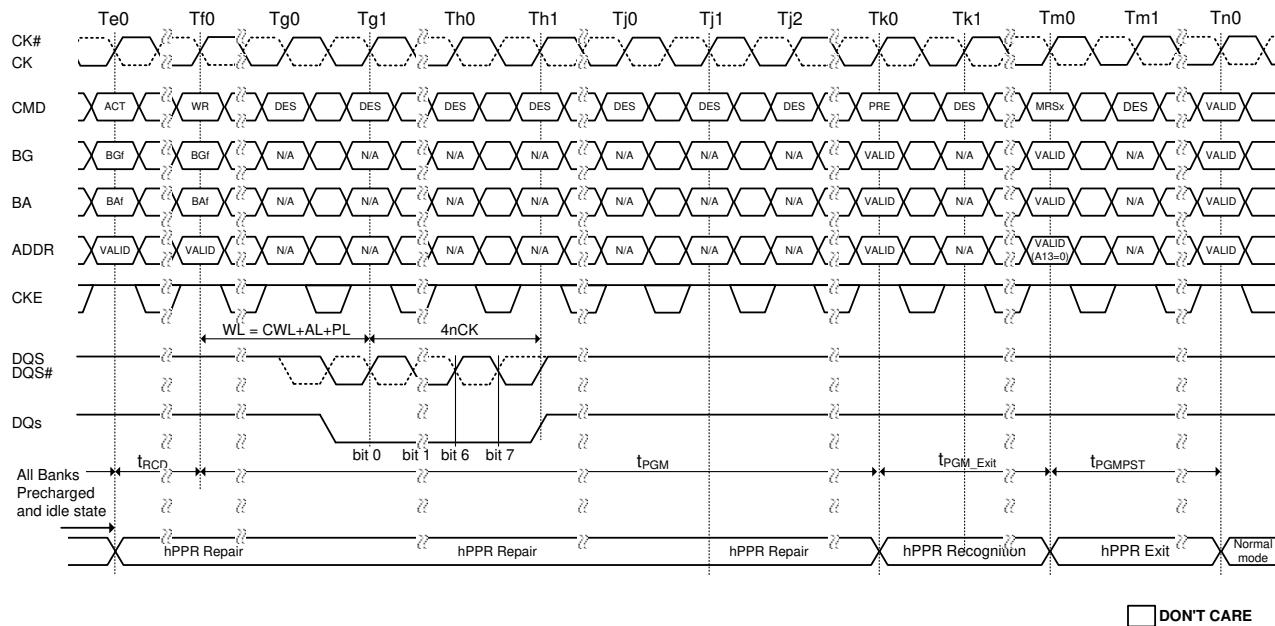


Figure 171. hPPR WR – Repair and Exit

Table 60. hPPR Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
$t_{PPGM}$	hPPR Programming Time	2000	-	ms
$t_{PPGM\_Exit}$	hPPR Precharge Exit Time	15	-	ns
$t_{PPGM\_PST}$	hPPR Exit Time	50	-	μs

## sPPR Row Repair

Soft post package repair (sPPR) is a way to quickly, but temporarily, repair a row element in a bank on a DRAM device, where hPPR takes longer but permanently repairs a row element. sPPR mode is entered in a similar fashion as hPPR, sPPR uses MR4[5] while hPPR uses MR4[13]. sPPR is disabled with MR4[5] = 0, which is the normal state, and sPPR is enabled with MR4[5] = 1, which is the sPPR enabled state.

sPPR requires the same guard key sequence as hPPR to qualify the MR4 PPR entry. After sPPR entry, an ACT command will capture the target bank and target row, herein seed row, where the row repair will be made. After tRCD time, a WR command is used to select the individual DRAM, through the DQ bits, to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE command, the sPPR mode can be exited and normal operation can resume.

The DRAM will retain the soft repair information as long as VDD remains within the operating region unless rewritten by a subsequent sPPR entry to the same bank. If DRAM power is removed or the DRAM is reset, the soft repair will revert to the unrepairs state. hPPR and sPPR should not be enabled at the same time; sPPR does not have to be disabled and cleared prior to entering hPPR mode.

With sPPR, DDR4 can repair one row per bank. When a subsequent sPPR request is made to the same bank, the subsequently issued sPPR address will replace the previous sPPR address. When the hPPR resource for a bank is used up, the bank should be assumed to not have available resources for sPPR. If a repair sequence is issued to a bank with no repair resource available, the DRAM will ignore the programming sequence.

The bank receiving sPPR change is expected to retain memory array data in all rows except for the seed row and its associated row addresses. If the data in the memory array in the bank under sPPR repair is not required to be retained, then the handling of the seed row's associated row addresses is not of interest and can be ignored. If the data in the memory array is required to be retained in the bank under sPPR mode, then prior to executing the sPPR mode, the seed row and its associated row addresses should be backed up and subsequently restored after sPPR has been completed. sPPR associated seed row addresses are specified in the Table below.

**Table 61. sPPR Associated Row**

sPPR Associated Row Addresses						
BA0	A16	A15	A14	A13	A1	A0

All banks must be precharged and idle. DBI and CRC modes must be disabled, and all sPPR timings must be followed as shown in the timing diagram that follows.

All other commands except those listed in the following sequences are illegal.

1. Issue MR4[5] 1 to enter sPPR mode enable.
  - a. All DQ are driven HIGH.
2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by tMOD. Please note that JEDEC recently added the four guard key entry used for hPPR to sPPR entry; early DRAMs may not require four guard key entry code. A prudent controller design should accommodate either option in case an earlier DRAM is used.
  - a. Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ, and NOP, are not allowed.
  - b. If the guard key bits are not entered in the required order or interrupted with other MR commands, sPPR will not be enabled, and the programming cycle will result in a NOP.
  - c. When the sPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
3. After tMOD, issue an ACT command with failing BG and BA with the row address to be repaired.
4. After tRCD, issue a WR command with BG and BA of failing row address.
  - a. The address must be at valid levels, but the address is a "Don't Care."

5. All DQ of the target DRAM should be driven LOW for 4nCK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for sPPR to initiate repair.
  - a. Repair will be initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
  - b. Repair will not be initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.

\* JEDEC states: All DQs of target DRAM should be LOW for 4tCK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than the first 2tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than the first 2tCK, then hPPR mode execution is unknown.

  - c. DQS should function normally.
6. REF command may NOT be issued at anytime while in sPPR mode.
7. Issue PRE after tWR time so that the device can repair the target row during tWR time.
  - a. Wait tPGM\_Exit\_s after PRE to allow the device to recognize the repaired target row address.
8. Issue MR4[5] 0 command to sPPR mode disable.
  - a. Wait tPGMPST\_s for sPPR mode exit to complete.
  - b. After tPGMPST\_s has expired, any valid command may be issued.

The entire sequence from sPPR mode enable through sPPR mode disable may be repeated if more than one repair is to be done.

After sPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

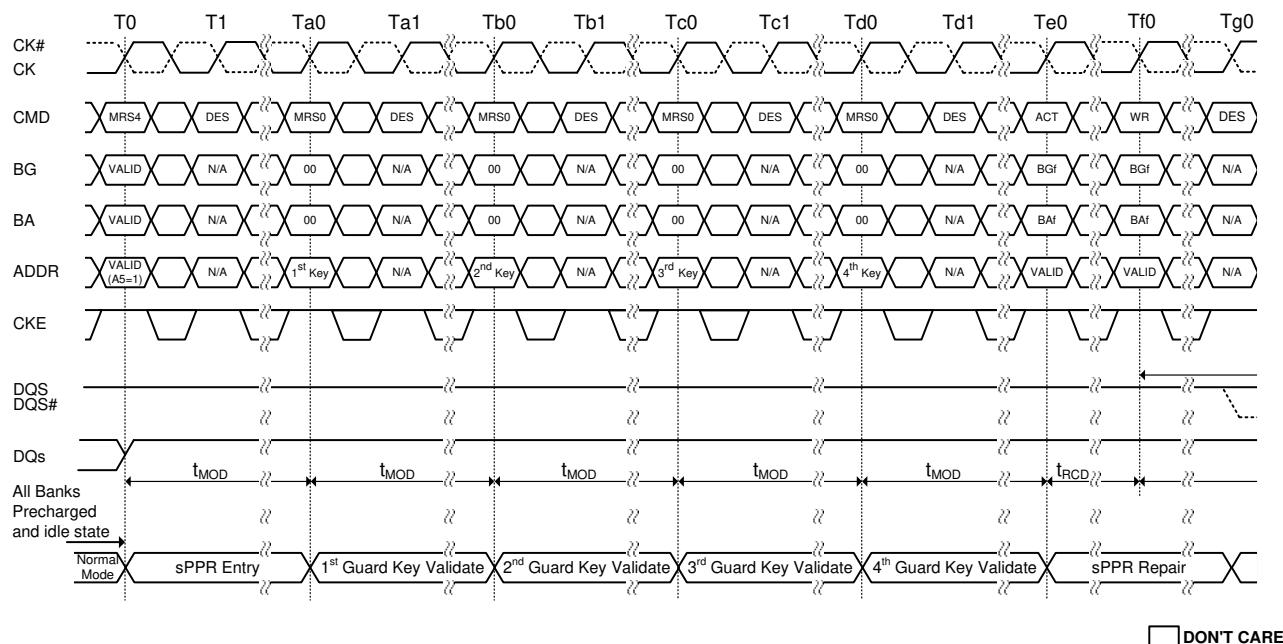


Figure 172. sPPR – Entry

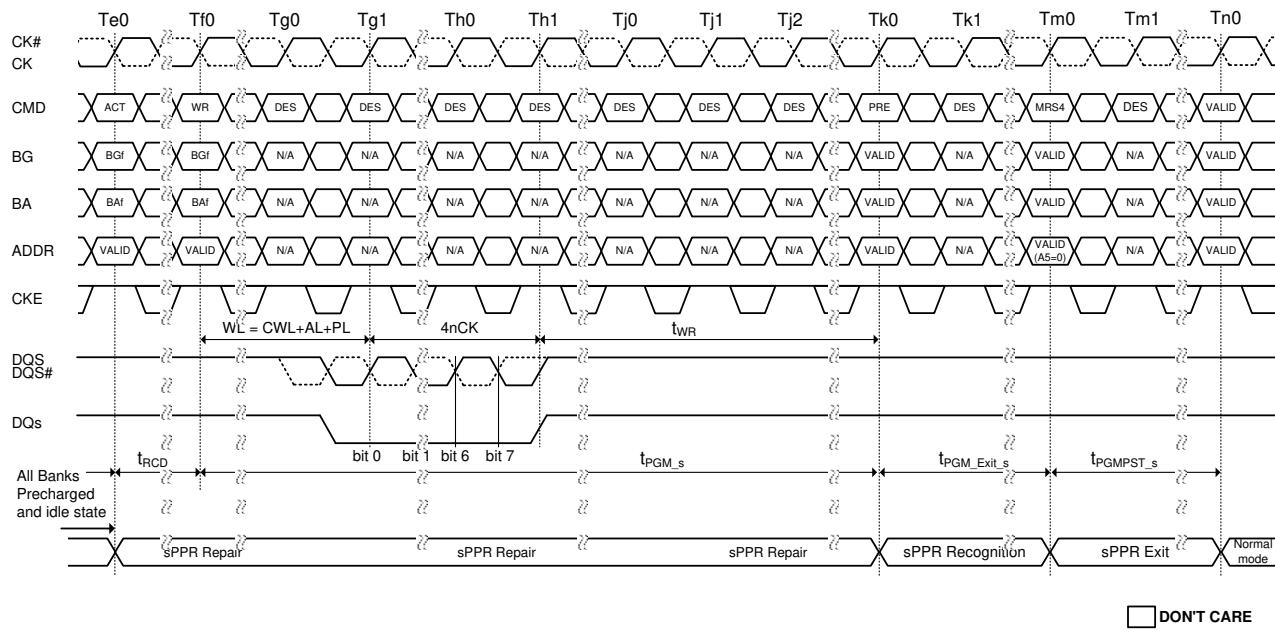


Figure 173. sPPR – Repair, and Exit

Table 62. hPPR Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
$t_{PGM\_S}$	sPPR Programming Time	$t_{RCD}(\text{MIN}) + WL + 4nCK + t_{WR}(\text{MIN})$	-	ns
$t_{PGM\_Exit\_S}$	sPPR Precharge Exit Time	20	-	ns
$t_{PGMPST\_S}$	sPPR Exit Time	$t_{MOD}$	-	us

## hPPR/sPPR Support Identifier

Table 63. DDR4 Repair Mode Support Identifier

MPR Page 2	A7	A6	A5	A4	A3	A2	A1	A0
	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
MPR0	hPPR <sup>1</sup>	sPPR <sup>2</sup>	RTT_WR	Temp sensor		CRC	RTT_WR	

Note 1. 0 = hPPR mode is not available, 1 = hPPR mode is available.

Note 2. 0 = sPPR mode is not available, 1 = sPPR mode is available.

Note 3. Gray shaded areas are for reference only.

## On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for x16 configuration. ODT is applied to each DQ0-15, UDQS, UDQS#, LDQS, LDQS#, UDM# and LDM# signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown below.

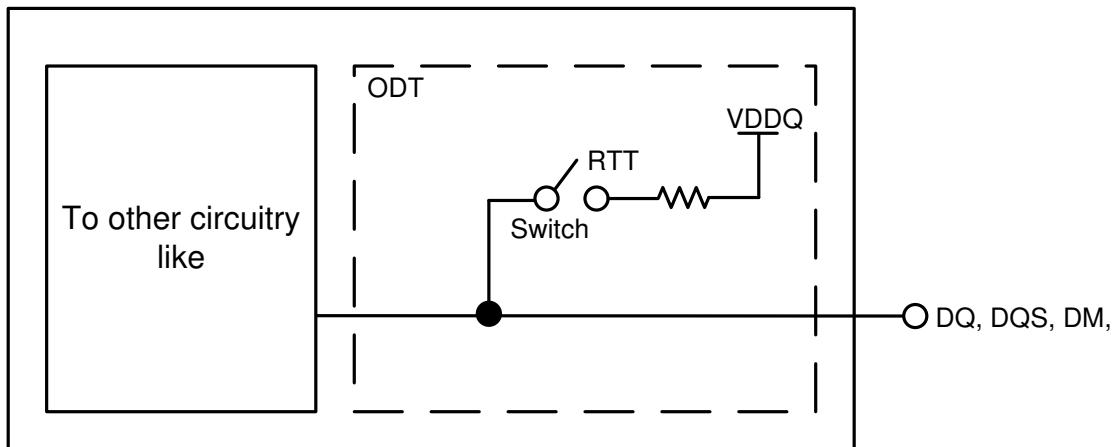


Figure 174. Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of  $R_{TT}$  is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable  $R_{TT\_NOM}$  (MR1 A [10:8] = 000) and in self refresh mode.

## ODT Mode Register and ODT State Table

The ODT Mode of DDR4 device has 4 states, Data Termination Disable,  $R_{TT\_WR}$ ,  $R_{TT\_NOM}$  and  $R_{TT\_PARK}$ . And the ODT Mode is enabled if any of MR1 A[10:8] or MR2 A[10:9] or MR5 A[8:6] are non zero. When enabled, the value of  $R_{TT}$  is determined by the settings of these bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Controller can control each  $R_{TT}$  condition with WR/RD command and ODT pin.

- $R_{TT\_WR}$ : The rank that is being written to provide termination regardless of ODT pin status (either high or low)
- $R_{TT\_NOM}$ : DRAM turns ON  $R_{TT\_NOM}$  if it sees ODT asserted (except ODT is disabled by MR1).
- $R_{TT\_PARK}$ : Default parked value set via MR5 to be enabled and ODT pin is driven low.
- Data Termination Disable: DRAM driving data upon receiving Read command disables the termination after RL-X and stays off for a duration of BL/2 + X clock cycles. (X is 2 for  $1t_{CK}$  and 3 for  $2t_{CK}$  preamble mode).

The  $R_{TT}$  values have the following priority:

which means if there is Write command along with ODT pin high, then DRAM turns on  $R_{TT\_WR}$  not  $R_{TT\_NOM}$ , and also if there is Read command, then DRAM disables data termination regardless of ODT pin and goes into driving mode.

- Data termination disable
- $R_{TT\_WR}$
- $R_{TT\_NOM}$
- $R_{TT\_PARK}$

**Table 64. Termination State Table**

Case	$R_{TT\_PARK}$ MR5[8:6]	$R_{TT\_NOM}$ MR1[10:8] <sup>1</sup>	$R_{TT\_WR}$ MR2[11:9] <sup>2</sup>	ODT pin	ODT Read <sup>3</sup>	ODT termination state <sup>7</sup>	ODT Write
A <sup>4</sup>	Disabled	Disabled	Disabled	Don't care	Off (Hi-Z)	Off (Hi-Z)	Off (Hi-Z)
			Enabled	Don't care	Off (Hi-Z)	Off (Hi-Z)	$R_{TT\_WR}$
B <sup>5</sup>	Enabled	Disabled	Disabled	Don't care	Off (Hi-Z)	$R_{TT\_PARK}$	$R_{TT\_PARK}$
			Enabled	Don't care	Off (Hi-Z)	$R_{TT\_PARK}$	$R_{TT\_WR}$
C <sup>6</sup>	Disabled	Enabled	Disabled	Low	Off (Hi-Z)	Off (Hi-Z)	Off (Hi-Z)
				High	Off (Hi-Z)	$R_{TT\_NOM}$	$R_{TT\_NOM}$
			Enabled	Low	Off (Hi-Z)	Off (Hi-Z)	$R_{TT\_WR}$
				High	Off (Hi-Z)	$R_{TT\_NOM}$	$R_{TT\_WR}$
D <sup>6</sup>	Enabled	Enabled	Disabled	Low	Off (Hi-Z)	$R_{TT\_PARK}$	$R_{TT\_PARK}$
				High	Off (Hi-Z)	$R_{TT\_NOM}$	$R_{TT\_NOM}$
			Enabled	Low	Off (Hi-Z)	$R_{TT\_PARK}$	$R_{TT\_WR}$
				High	Off (Hi-Z)	$R_{TT\_NOM}$	$R_{TT\_WR}$

Note 1. If  $R_{TT\_NOM}$  MR is disabled, ODT receiver power will be turned off to save power.

Note 2. If  $R_{TT\_WR}$  is enabled,  $R_{TT\_WR}$  will be activated by write command for defined period time independent of ODT pin and MR setting of  $R_{TT\_PARK}$  /  $R_{TT\_NOM}$ . This is described in the Dynamic ODT section.

Note 3. When a read command is executed, DRAM termination state will be High-Z for defined period independent of ODT pin and MR setting of  $R_{TT\_PARK}$  /  $R_{TT\_NOM}$ . This is described in the ODT during Read section.

Note 4. Case A is generally best for single-rank memories.

Note 5. Case B is generally best for dual-rank, single-slotted memories.

Note 6. Case C and Case D are generally best for multi-slotted memories.

Note 7. The ODT feature is turned off and not supported in self refresh mode.

## ODT Read Disable State Table

Upon receiving a READ command, the DRAM driving data disables ODT after RL - (2 or 3) clock cycles, where 2 = 1tCK preamble mode and 3 = 2tCK preamble mode. ODT stays off for a duration of BL/2 + (2 or 3) + (0 or 1) clock cycles, where 2 = 1tCK preamble mode, 3 = 2tCK preamble mode, 0 = CRC disabled, and 1 = CRC enabled.

**Table 65. Read Termination Disable Window**

Preamble	CRC	Start ODT Disable After Read	Duration of ODT Disable
1 tCK	Disabled	RL - 2	BL/2 + 2
	Enabled	RL - 2	BL/2 + 3
2 tCK	Disabled	RL - 3	BL/2 + 3
	Enabled	RL - 3	BL/2 + 4

On-die termination effective resistances are defined and can be selected by any or all of the following options:

- MR1 A[10:8] ( $R_{TT\_NOM}$ ) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.
- MR2 A[11:9] ( $R_{TT\_WR}$ ) - Disable, 240Ω, 120Ω, and 80Ω.
- MR5 A[8:6] ( $R_{TT\_PARK}$ ) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.

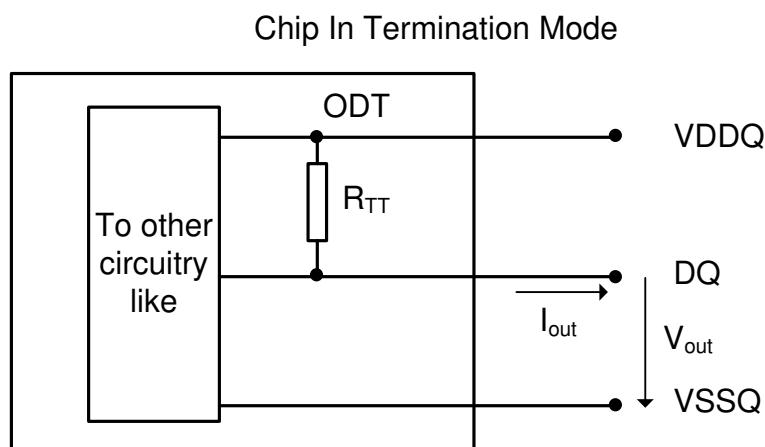
ODT is applied to the following inputs:

- x16: DQs, LDM#, UDM#, LDQS, LDQS#, UDQS, and UDQS# inputs.

## ODT Definition of Voltages and Currents

On die termination effective R<sub>tt</sub> values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

$$R_{TT} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$



**Figure 175. On Die Termination**

**Table 66. ODT Electrical Characteristics RZQ=240Ω ±1% entire temperature operation range; after proper ZQ calibration**

R <sub>TT</sub>	V <sub>out</sub>	Min.	Nom.	Max.	Unit	Note
240Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ	1,2,3
120Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/2	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/2	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/2	1,2,3
80Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/3	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/3	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/3	1,2,3
60Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/4	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/4	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/4	1,2,3
48Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/5	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/5	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/5	1,2,3
40Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/6	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/6	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/6	1,2,3
34Ω	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/7	1,2,3
	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/7	1,2,3
	V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0	-	10	%	1,2,4,5,6

Note 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

Note 2. Pull-up ODT resistors are recommended to be calibrated at 0.8 x V<sub>DDQ</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 x V<sub>DDQ</sub> and 1.1 x V<sub>DDQ</sub>.

Note 3. The tolerance limits are specified under the condition that V<sub>DDQ</sub>=V<sub>DD</sub> and V<sub>SSQ</sub>=V<sub>SS</sub>.

Note 4. DQ to DQ mismatch within byte variation for a given component including DQS and DQS#. (characterized)

Note 5. R<sub>TT</sub> variance range ratio to R<sub>TT</sub> Nominal value in a given component, including DQS and DQS#.

$$\text{DQ-DQ Mismatch in a Device} = \frac{R_{TT\text{Max}} - R_{TT\text{Min}}}{R_{TT\text{NOM}}} \times 100$$

Note 6. This parameter of x16 device is specified for Upper byte and Lower byte.

## Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power-down mode (regardless of MR1 bit A10)
- Precharge power-down mode

In synchronous ODT mode,  $R_{TT\_NOM}$  will be turned on DODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off DODTLoft clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoft = WL - 2. When operating in  $2t_{CK}$  Preamble Mode, The ODT latency must be 1 clock smaller than in  $1t_{CK}$  Preamble Mode; DODTLon = WL - 3; DODTLoft = WL - 3. (WL = CWL+AL+PL)

## ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register MR1 applies to ODT Latencies as shown below:

**Table 67. ODT Latency**

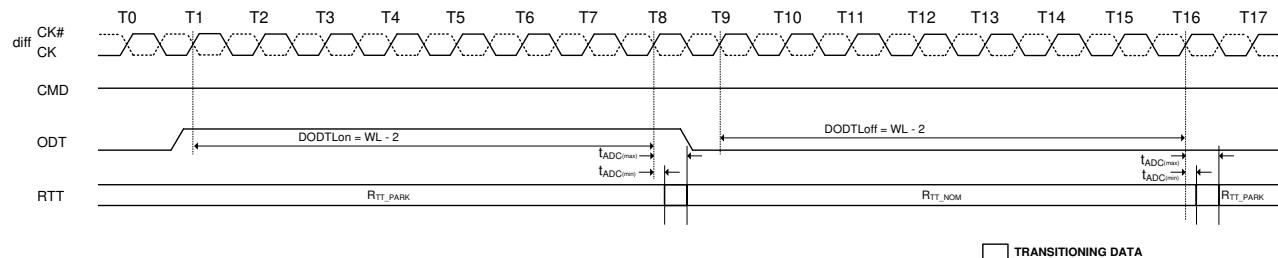
Symbol	Parameter	1 $t_{CK}$ Preamble	2 $t_{CK}$ Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL - 2	CWL + AL + PL - 3	$t_{CK}$
DODTLoft	Direct ODT turn off Latency	CWL + AL + PL - 2	CWL + AL + PL - 3	$t_{CK}$
RODTLoft	Read command to internal ODT turn off Latency	CL + AL + PL - 2	CL + AL + PL - 3	$t_{CK}$
RODTLon4	Read command to $R_{TT\_PARK}$ turn on Latency in BC4	RODTLoft + 4	RODTLoft + 5	$t_{CK}$
RODTLon8	Read command to $R_{TT\_PARK}$ turn on Latency in BC8/BL8	RODTLoft + 6	RODTLoft + 7	$t_{CK}$
ODTH4	ODT Assertion time, BC4 mode	4	5	$t_{CK}$
ODTH8	ODT Assertion time, BL8 mode	6	7	$t_{CK}$

## Timing Parameter

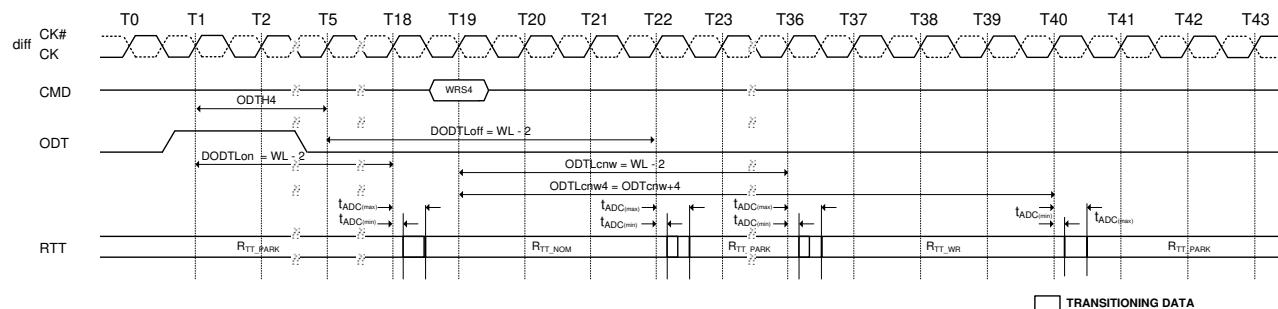
In synchronous ODT mode, the following parameters apply:

- DODTLon, DODTloff, RODTloff, RODTLon4, RODTLon8,  $t_{ADC}$  (MIN) (MAX).
- $t_{ADC}$  (MIN) and  $t_{ADC}$  (MAX) are minimum and maximum  $R_{TT}$  change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

When ODT is asserted, it must remain high until minimum ODTH4 (BL = 4) or ODTH8 (BL = 8) is satisfied. Additionally, depending on CRC or  $2t_{CK}$  preamble setting in MRS, ODTH should be adjusted.



**Figure 176. Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODTloff=WL-2=7**



**Figure 177. Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17**

ODT must be held high for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or  $2t_{CK}$  preamble setting.

## ODT During Reads

Because the DDR4 DRAM cannot terminate with  $R_{TT}$  and drive with  $R_{ON}$  at the same time;  $R_{TT}$  may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25, the device turns on the termination when it stops driving, which is determined by  $t_{HZ}$ . If the DRAM stops driving early (that is,  $t_{HZ}$  is early), then  $t_{ADC (MIN)}$  timing may apply. If the DRAM stops driving late (that is,  $t_{HZ}$  is late), then the DRAM complies with  $t_{ADC (MAX)}$  timing.

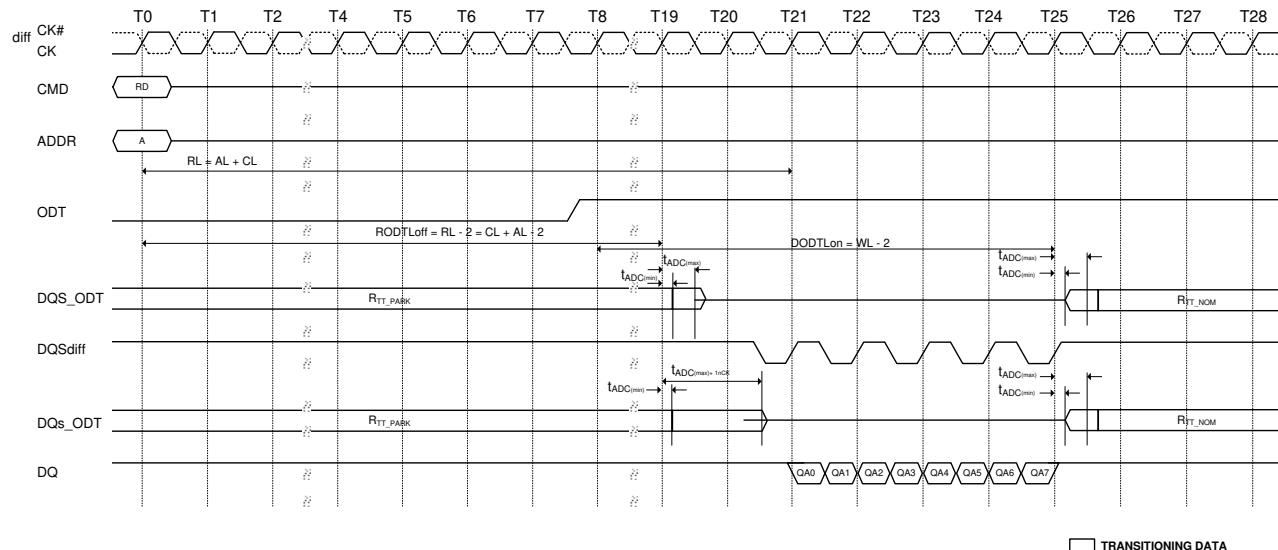


Figure 178. Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLooff=AL+CWL-2=17; 1tCK preamble)

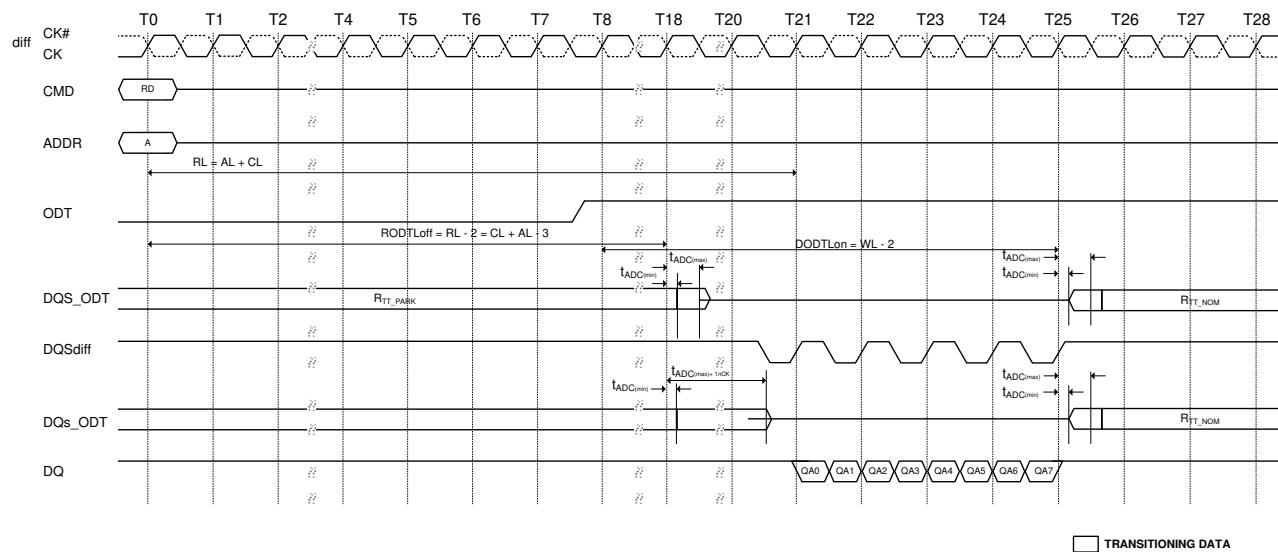


Figure 179. Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLooff=AL+CWL-2=17; 2tCK preamble)

## Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature, described below.

### Functional Description

The dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three  $R_{TT}$  values are available:  $R_{TT\_NOM}$ ,  $R_{TT\_WR}$ , and  $R_{TT\_PARK}$ .
  - The value for  $R_{TT\_NOM}$  is preselected via bits MR1 A[10:8].
  - The value for  $R_{TT\_WR}$  is preselected via bits MR2 A[11:9].
  - The value for  $R_{TT\_PARK}$  is preselected via bits MR5 A[8:6].
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength  $R_{TT\_NOM}$  or  $R_{TT\_PARK}$  is selected.
  - $R_{TT\_NOM}$  on/off timing is controlled via ODT pin and latencies DODTLon and DODTLooff; and  $R_{TT\_PARK}$  is on when ODT is LOW.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - Latency ODTLcnw after the write command, termination strength  $R_{TT\_WR}$  is selected.
  - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength  $R_{TT\_WR}$  is deselected.
  - One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC Mode and/or 2  $t_{CK}$  preamble enablement. The following table shows latencies and timing parameters which are relevant for the on-die termination control in dynamic ODT mode.

The dynamic ODT feature is not supported in DLL-off mode. MRS command must be used to set  $R_{TT\_WR}$ , MR2 A[11:9] = 000, to disable dynamic ODT externally.

**Table 68. Latencies and timing parameters relevant for Dynamic ODT with 1 $t_{CK}$  preamble mode and CRC disabled**

Name and Description	Abbr.	Defined from	Define to	DDR4-3200	Unit
ODT Latency for changing from $R_{TT\_PARK}/R_{TT\_NOM}$ to $R_{TT\_WR}$	ODTLcnw	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_PARK}/R_{TT\_NOM}$ to $R_{TT\_WR}$	ODTLcnw = WL - 2	$t_{CK}$
ODT Latency for change from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$ (BL = 4)	ODTLcwn4	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$	ODTLcwn4 = 4 + ODTLcnw	$t_{CK}$
ODT Latency for change from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$ (BL = 8)	ODTLcwn8	Registering external write command	Change $R_{TT}$ strength from $R_{TT\_WR}$ to $R_{TT\_PARK}/R_{TT\_NOM}$	ODTLcwn8 = 6 + ODTLcnw	$t_{CK}$
RTT change skew	$t_{ADC}$	ODTLcnw ODTLcwn	$R_{TT}$ Valid	$t_{ADC(min)} = 0.26$ $t_{ADC(max)} = 0.74$	$t_{CK}$

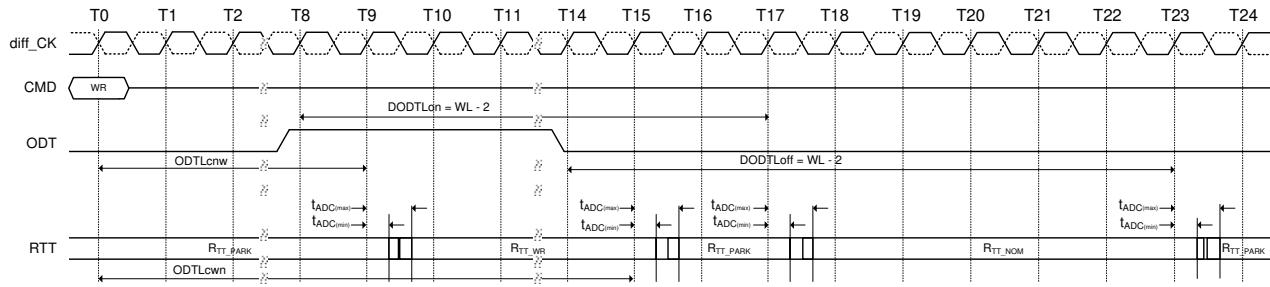
**Table 69. Latencies and timing parameters relevant for Dynamic ODT with 1 $t_{CK}$  and 2 $t_{CK}$  preamble mode and CRC enabled/disabled**

Symbol	1 $t_{CK}$ Preamble		2 $t_{CK}$ Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw <sup>1</sup>	WL - 2	WL - 2	WL - 3	WL - 3	$t_{CK}$
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	$t_{CK}$
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	$t_{CK}$

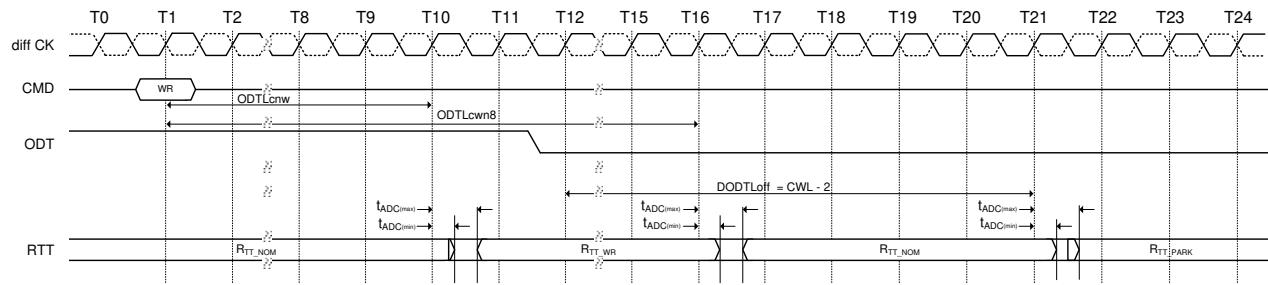
Note 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).

## ODT Timing Diagrams

The following pages provide example timing diagrams



**Figure 180. ODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)**



**Figure 181. Dynamic ODT overlapped with Rtt\_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)**

## Asynchronous ODT Mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.

In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal ( $R_{TT\_NOM}$ ). In asynchronous ODT mode, the following timing parameters apply  $t_{AONAS,min,max}$ ,  $t_{AOFAS,min,max}$ .

Minimum  $R_{TT\_NOM}$  turn-on time ( $t_{AONAS,min}$ ) is the point in time when the device termination circuit leaves  $R_{TT\_PARK}$  and ODT resistance begins to change. Maximum  $R_{TT\_NOM}$  turn on time ( $t_{AONAS,max}$ ) is the point in time when the ODT resistance is reached  $R_{TT\_NOM}$ .

$t_{AONAS,min}$  and  $t_{AONAS,max}$  are measured from ODT being sampled high.

Minimum  $R_{TT\_NOM}$  turn-off time ( $t_{AOFAS,min}$ ) is the point in time when the devices termination circuit starts to leave  $R_{TT\_NOM}$ .

Maximum  $R_{TT\_NOM}$  turn-off time ( $t_{AOFAS,max}$ ) is the point in time when the on-die termination has reached  $R_{TT\_PARK}$ .  $t_{AOFAS,min}$  and  $t_{AOFAS,max}$  are measured from ODT being sampled low.

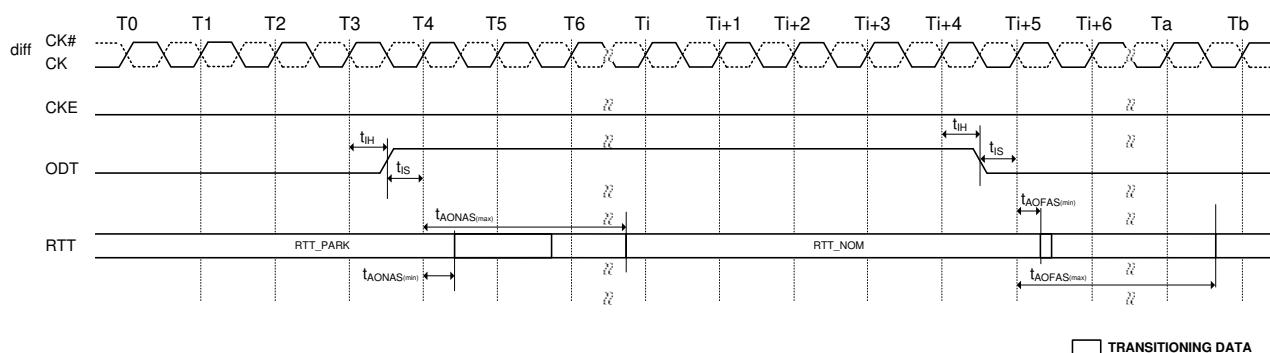


Figure 182. Asynchronous ODT Timing on DDR4 SDRAM with DLL-off

## ODT buffer disabled mode for Power down

DRAM does not provide  $R_{TT\_NOM}$  termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down (from  $t_{DODT\text{off}+1}$  prior to CKE low till  $t_{CPDED}$  after CKE low). The ODT signal may be floating after  $t_{CPDED\text{min}}$  has expired. In this mode,  $R_{TT\_NOM}$  termination corresponding to sampled ODT at the input after CKE is first registered low (and  $t_{ANPD}$  before that) may be either  $R_{TT\_NOM}$  or  $R_{TT\_PARK}$ .  $t_{ANPD}$  is equal to  $(WL-1)$  and is counted backwards from PDE.

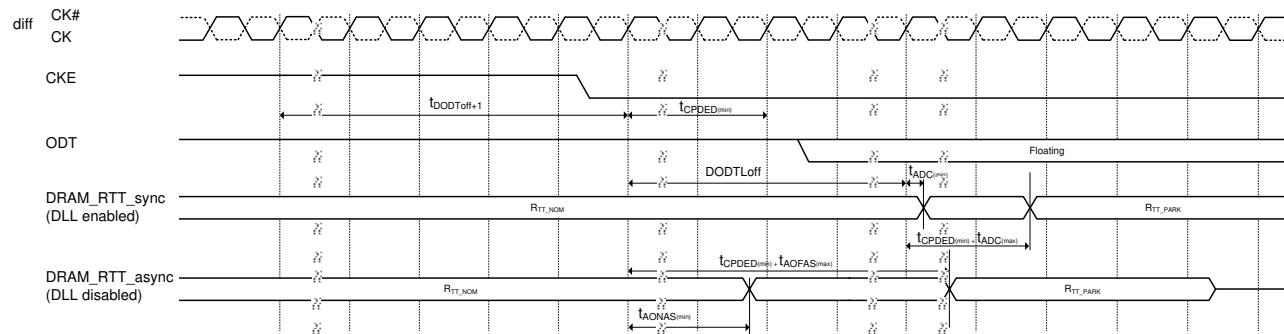


Figure 183. ODT timing for power down entry with ODT buffer disable mode

When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until  $t_{XP}$  is met.

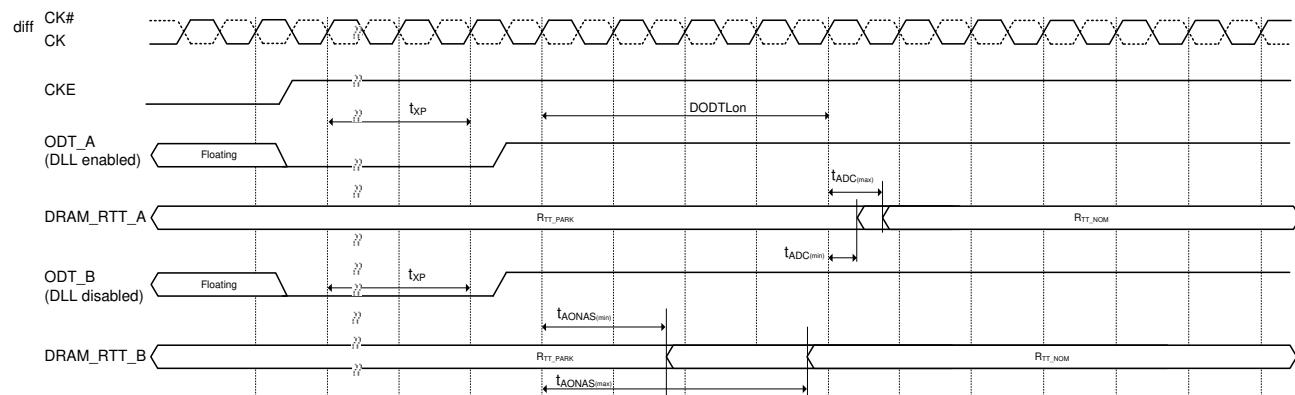
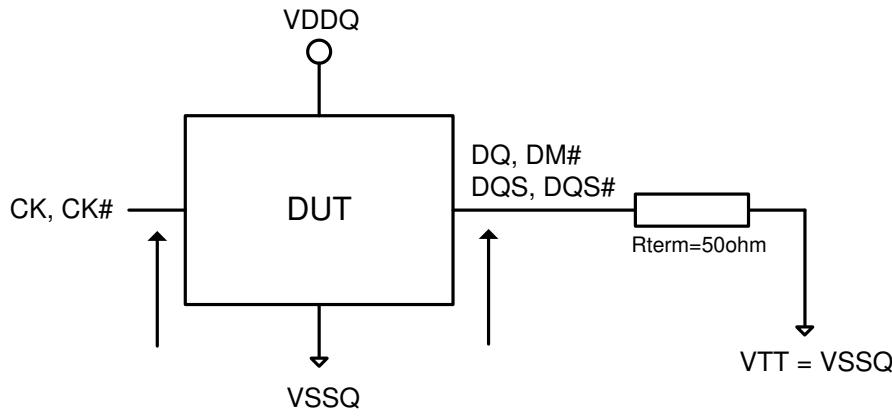


Figure 184. ODT timing for power down exit with ODT buffer disable mode

## ODT Timing Definitions

### Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined below



**Figure 185. ODT Timing Reference Load**

### ODT Timing Definitions

Definitions for  $t_{ADC}$ ,  $t_{AONAS}$  and  $t_{AOFAS}$  are provided in the table and measurement reference settings are provided in the subsequent. The  $t_{ADC}$  for the Dynamic ODT case and Read Disable ODT cases are represented by  $t_{ADC}$  of Direct ODT Control case.

**Table 70. ODT Timing Definitions**

Symbol	Begin Point Definition	End Point Definition
$t_{ADC}$	Rising edge of CK,CK# defined by the end point of DODTLooff	Extrapolated point at $V_{RTT\_NOM}$
	Rising edge of CK,CK# defined by the end point of DODTLon	Extrapolated point at $V_{SSQ}$
	Rising edge of CK,CK# defined by the end point of ODTLcnw	Extrapolated point at $V_{RTT\_NOM}$
	Rising edge of CK,CK# defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at $V_{SSQ}$
$t_{AONAS}$	Rising edge of CK,CK# with ODT being first registered high	Extrapolated point at $V_{SSQ}$
$t_{AOFAS}$	Rising edge of CK,CK# with ODT being first registered low	Extrapolated point at $V_{RTT\_NOM}$

**Table 71. Reference Settings for ODT Timing Measurements**

Measured Parameter	$R_{TT\_PARK}$	$R_{TT\_NOM}$	$R_{TT\_WR}$	$V_{sw1}$	$V_{sw2}$	Note
$t_{ADC}$	Disable	RZQ/7	-	0.20V	0.40V	1,2
	-	RZQ/7	Hi-Z	0.20V	0.40V	1,3
$t_{AONAS}$	Disable	RZQ/7	-	0.20V	0.40V	1,2
$t_{AOFAS}$	Disable	RZQ/7	-	0.20V	0.40V	1,2

Note 1. MR setting is as follows.

- MR1 A10=1, A9=1, A8=1 ( $R_{TT\_NOM}$  Setting)
- MR5 A8=0, A7=0, A6=0 ( $R_{TT\_PARK}$  Setting)
- MR2 A11=0, A10=1, A9=1 ( $R_{TT\_WR}$  Setting)

Note 2. ODT state change is controlled by ODT pin.

Note 3. ODT state change is controlled by Write Command.

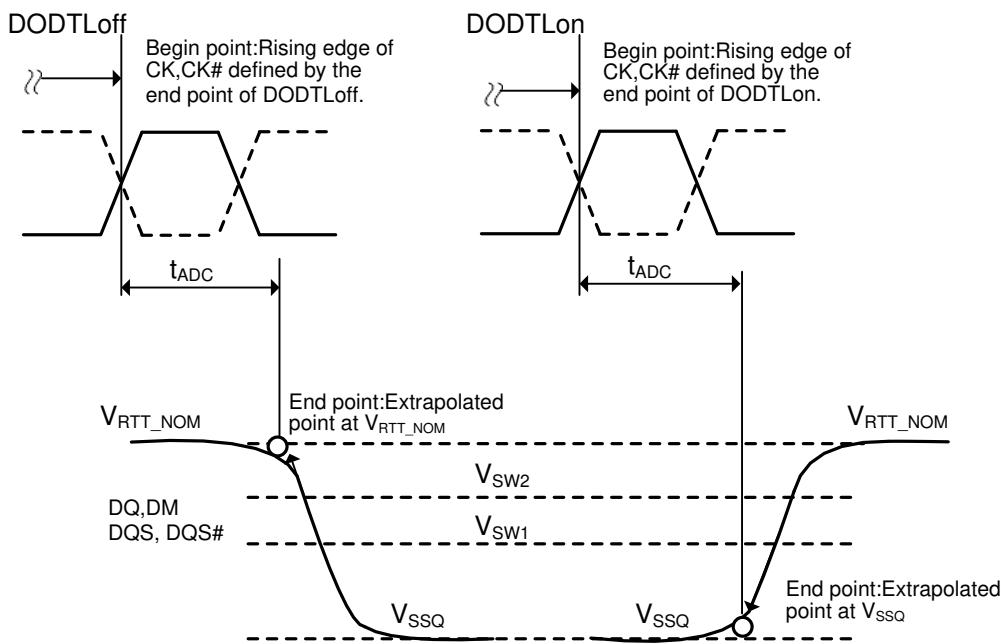


Figure 186. Definition of tADC at Direct ODT Control

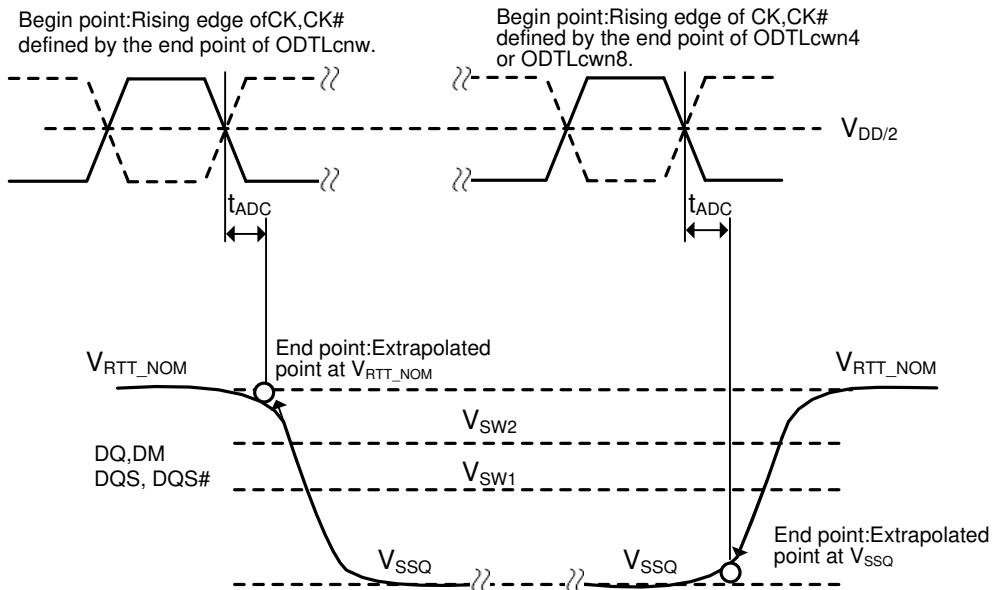


Figure 187. Definition of tADC at Dynamic ODT Control

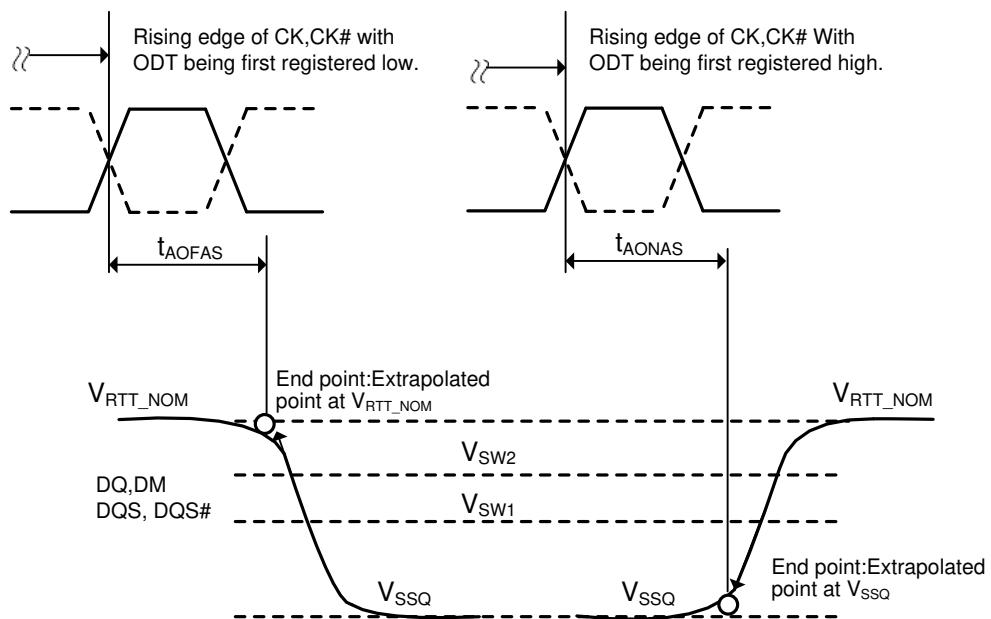


Figure 188. Definition of  $t_{AOFAS}$  and  $t_{AONAS}$

**Table 72. Absolute Maximum DC Ratings**

Symbol	Parameter	Values	Unit	Note
$V_{DD}$	Voltage on $V_{DD}$ pin relative to $V_{SS}$	-0.3 ~ 1.5	V	1,3
$V_{DDQ}$	Voltage on $V_{DDQ}$ pin relative to $V_{SS}$	-0.3 ~ 1.5	V	1,3
$V_{PP}$	Voltage on $V_{PP}$ pin relative to $V_{SS}$	-0.3 ~ 3.0	V	4
$V_{IN}, V_{OUT}$	Voltage on any pin except $V_{REFCA}$ relative to $V_{SS}$	-0.3 ~ 1.5	V	1,3,5
$T_{STG}$	Storage Temperature	-55 ~ 100	°C	1,2

Note 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Note 3.  $V_{DD}$  and  $V_{DDQ}$  must be within 300 mV of each other at all times; and  $V_{REFCA}$  must be not greater than  $0.6 \times V_{DDQ}$ . When  $V_{DD}$  and  $V_{DDQ}$  are less than 500 mV;  $V_{REFCA}$  may be equal to or less than 300 mV.

Note 4.  $V_{PP}$  must be equal or greater than  $V_{DD}/V_{DDQ}$  at all times.

Note 5. Refer to overshoot area above 1.5 V.

**Table 73. Temperature Range**

Symbol	Parameter	Values	Unit	Note
$T_{OPER}$	Normal Operating Temperature Range	0 ~ 85	°C	1
	Extended Temperature Range	85 ~ 95	°C	1,2

Note 1. Operating temperature is the case surface temperature on center/top of the DRAM.

Note 2. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are guaranteed in this range, but the following additional apply.

a. Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

**Table 74. Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$V_{DD}$	Supply Voltage	1.14	1.2	1.26	V	1,2,3
$V_{DDQ}$	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
$V_{PP}$	DRAM Activating Power Supply	2.375	2.5	2.75	V	3

Note 1. Under all conditions  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .

Note 2.  $V_{DDQ}$  tracks with  $V_{DD}$ . AC parameters are measured with  $V_{DD}$  and  $V_{DDQ}$  tied together.

Note 3. DC bandwidth is limited to 20MHz.

## AC and DC Input Measurement Levels

**Table 75. Single-Ended AC and DC Input Levels for Command and Address**

<b>Symbol</b>	<b>Parameter</b>	<b>DDR4-3200</b>		<b>Unit</b>	<b>Note</b>
		<b>Min.</b>	<b>Max.</b>		
$V_{IH,CA(DC65)}$	DC input logic high	$V_{REF} + 0.065$	$V_{DD}$	V	1,2
$V_{IL,CA(DC65)}$	DC input logic low	$V_{SS}$	$V_{REF} - 0.065$	V	1,2
$V_{IH,CA(AC90)}$	AC input logic high	$V_{REF} + 0.09$	$V_{DD}^5$	V	1,2,3
$V_{IL,CA(AC90)}$	AC input logic low	$V_{SS}^5$	$V_{REF} - 0.09$	V	1,2,3
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	$0.49 \times V_{DD}$	$0.51 \times V_{DD}$	V	4

Note 1. For input except RESET#.  $V_{REF} = V_{REFCA(DC)}$ .

Note 2.  $V_{REF} = V_{REFCA(DC)}$ .

Note 3. Input signal must meet  $V_{IL}/V_{IH(AC)}$  to meet  $t_{IS}$  timings and  $V_{IL}/V_{IH(DC)}$  to meet  $t_{IH}$  timings.

Note 4. The AC peak noise on  $V_{REF}$  may not allow  $V_{REF}$  to deviate from  $V_{REFCA(DC)}$  by more than  $\pm 1\% V_{DD}$  (for reference: approx.  $\pm 12mV$ )

Note 5. See "Overshoot and Undershoot Specifications".

## AC and DC Input Measurement Levels: $V_{REF}$ Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages  $V_{REFCA}$  is illustrated in the following figure. It shows a valid reference voltage  $V_{REF}(t)$  as a function of time. ( $V_{REF}$  stands for  $V_{REFCA}$ ).

$V_{REF}(DC)$  is the linear average of  $V_{REF}(t)$  over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in previous page. Furthermore  $V_{REF}(t)$  may temporarily deviate from  $V_{REF}(DC)$  by no more than  $\pm 1\% V_{DD}$ .

The voltage levels for setup and hold time measurements  $V_{IH}(AC)$ ,  $V_{IH}(DC)$ ,  $V_{IL}(AC)$ , and  $V_{IL}(DC)$  are dependent on  $V_{REF}$ .

“ $V_{REF}$ ” shall be understood as  $V_{REF}(DC)$ .

This clarifies that dc-variations of  $V_{REF}$  affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for  $V_{REF}(DC)$  deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with  $V_{REF}$  ac-noise. Timing and voltage effects due to ac-noise on  $V_{REF}$  up to the specified limit ( $\pm 1\% V_{DD}$ ) are included in DRAM timings and their associated deratings.

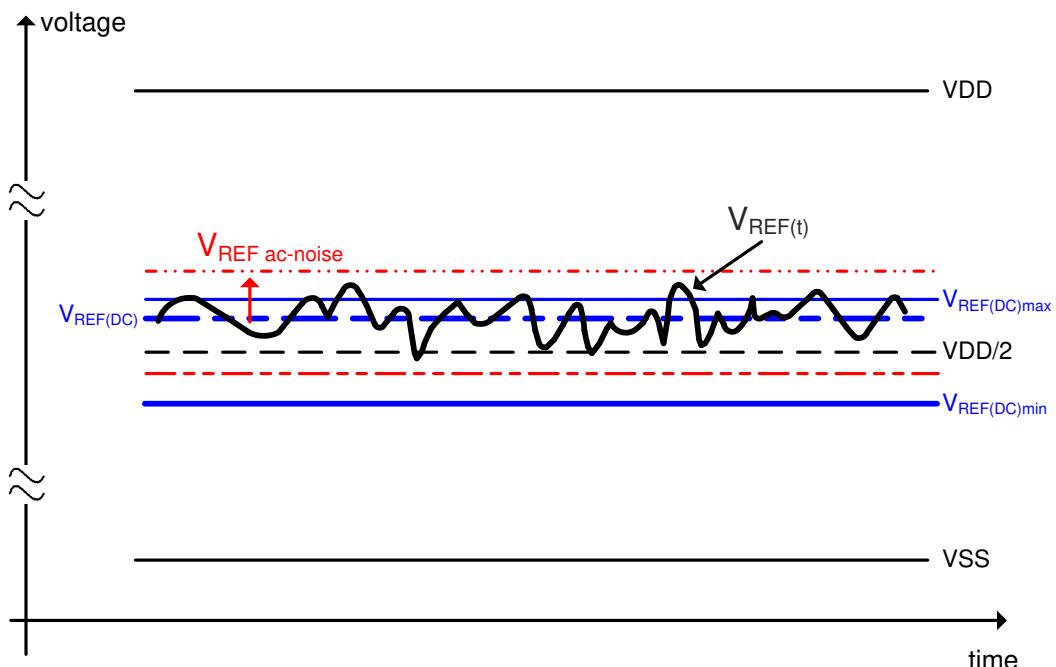
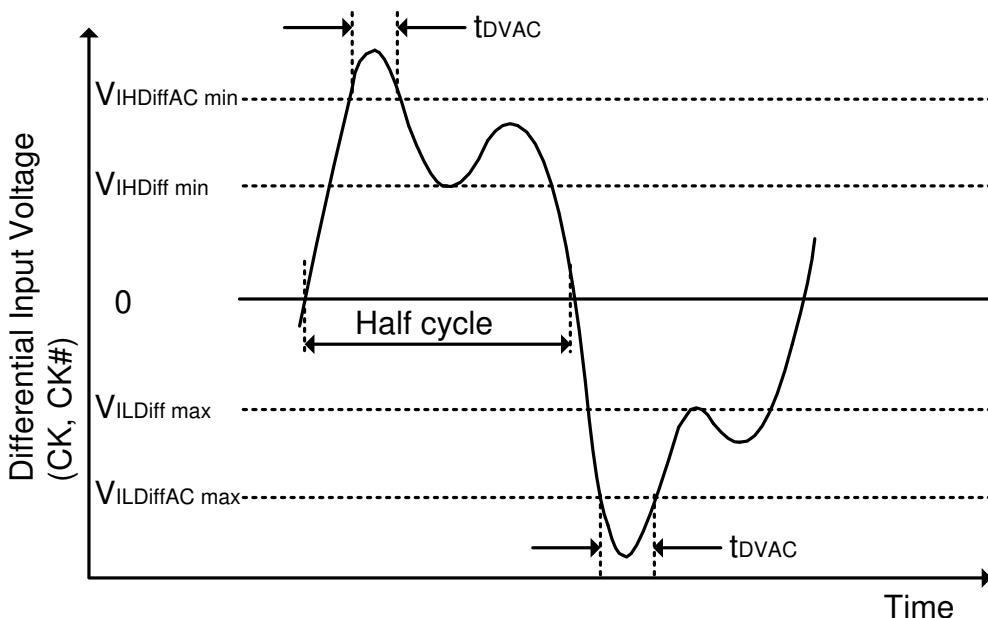


Figure 189. Illustration of  $V_{REF}(DC)$  tolerance and  $V_{REF}$  AC-noise limits

## Differential signal definition



NOTE 1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.  
 NOTE 2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

Figure 190. Definition of differential ac-swing and “time above ac-level” tDVAC

## Differential swing requirements for clock (CK – CK#)

Table 76. Differential AC and DC Input Levels

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$V_{IHdiff}$	Differential input high	110	-	mV	1,3
$V_{ILdiff}$	Differential input low	-	-110	mV	1,3
$V_{IHdiff(AC)}$	Differential input high ac	$2 \times (V_{IH(AC)} - V_{REF})$	-	V	2,3
$V_{ILdiff(AC)}$	Differential input low ac	-	$2 \times (V_{IL(AC)} - V_{REF})$	V	2,3

Note 1. Used to define a differential signal slew-rate.

Note 2. For CK - CK# use  $V_{IH,CA}/V_{IL,CA(AC)}$  of ADD/CMD and  $V_{REFCA}$ ;

Note 3. These values are not defined; however, the differential signals CK - CK#, need to be within the respective limits ( $V_{IH,CA(DC)} \text{ max}$ ,  $V_{IL,CA(DC)} \text{ min}$ ) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 77. Allowed time before ringback (tDVAC) for CK – CK#

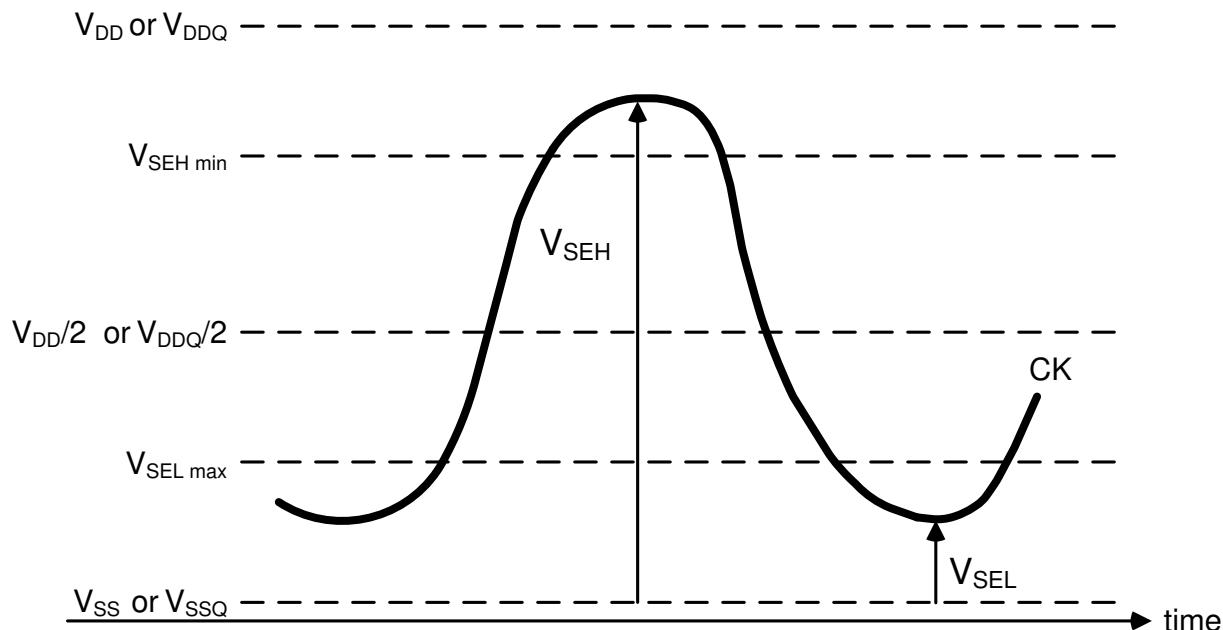
Slew Rate [V/ns]	tDVAC [ps] @ $ VIH/Ldiff(AC)  = 200$ mV		tDVAC [ps] @ $ VIH/Ldiff(AC)  = TBD$ mV	
	Min.	Max.	Min.	Max.
>4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.9	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
<1.0	80	-	TBD	-

## Single-ended requirements for differential signals

Each individual component of a differential signal (CK, CK#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach  $V_{SEHmin}$  /  $V_{SELmax}$  (approximately equal to the ac-levels ( $V_{IH,CA}(AC)$  /  $V_{IL,CA}(AC)$ ) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than  $V_{IH,CA}(AC100)/V_{IL,CA}(AC100)$  is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and CK#.



**Figure 191. Single-ended requirement for differential signals**

Note that, while ADD/CMD signal requirements are with respect to  $V_{REFCA}$ , the single-ended components of differential signals have a requirement with respect to  $V_{DD}/2$ ; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach  $V_{SELmax}$ ,  $V_{SEHmin}$  has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

**Table 78. Single-ended levels for CK, CK#**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$V_{SEH}$	Single-ended high-level for CK, CK#	$(V_{DD}/2) + 0.085$	-	V	1-3
$V_{SEL}$	Single-ended low-level for CK, CK#	-	$(V_{DD}/2) - 0.085$	V	1-3

Note 1. For CK – CK# use  $V_{IH,CA}/V_{IL,CA}(AC)$  of ADD/CMD

Note 2.  $V_{IH,CA}/V_{IL,CA}(AC)$  for ADD/CMD is based on  $V_{REFCA}$

Note 3. These values are not defined; however, the differential signals CK – CK#, need to be within the respective limits ( $V_{IH,CA}(DC)_{max}$ ,  $V_{IL,CA}(DC)_{min}$ ) for single-ended signals as well as the limitations for overshoot and undershoot.

## Address, Command and Control Overshoot and Undershoot specifications

Table 79. AC overshoot/undershoot for Address, Command and Control pins

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{AOSP}$	Maximum peak amplitude above $V_{AOS}$	0.06	V	
$V_{AOS}$	Upper boundary of overshoot area $A_{AOS1}$	$V_{DD} + 0.24$	V	1
$V_{AUS}$	Maximum peak amplitude allowed for undershoot	0.30	V	
$A_{AOS2}$	Maximum overshoot area per 1 $t_{CK}$ above $V_{AOS}$	0.0055	V-ns	
$A_{AOS1}$	Maximum overshoot area per 1 $t_{CK}$ between $V_{DD}$ and $V_{AOS}$	0.1699	V-ns	
$A_{AUS}$	Maximum undershoot area per 1 $t_{CK}$ below $V_{SS}$	0.1762	V-ns	

(A0-A13, BG0, BA0-BA1, ACT#, RAS#/A16, CAS#/A15, WE#/A14, CS#, CKE, ODT)

Note 1. The value of  $V_{AOS}$  matches  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DD}$  equals  $V_{DD}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DD}$  is above the recommended operating conditions,  $V_{AOS}$  remains at  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings"

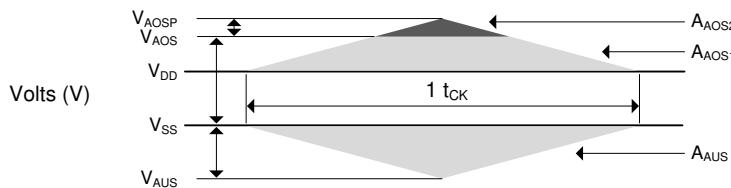


Figure 192. Address, Command and Control Overshoot and Undershoot Definition

## Clock Overshoot and Undershoot Specifications

Table 80. AC overshoot/undershoot specification for Clock

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{COSP}$	Maximum peak amplitude above $V_{COS}$	0.06	V	
$V_{COS}$	Upper boundary of overshoot area $A_{COS1}$	$V_{DD} + 0.24$	V	1
$V_{CUS}$	Maximum peak amplitude allowed for undershoot	0.30	V	
$A_{COS2}$	Maximum overshoot area per 1 UI above $V_{COS}$	0.0025	V-ns	
$A_{COS1}$	Maximum overshoot area per 1 UI between $V_{DD}$ and $V_{COS}$	0.0750	V-ns	
$A_{CUS}$	Maximum undershoot area per 1 UI below $V_{SS}$	0.0762	V-ns	

(CK, CK#)

Note 1. The value of  $V_{COS}$  matches  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DD}$  equals  $V_{DD}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DD}$  is above the recommended operating conditions,  $V_{COS}$  remains at  $V_{DD}$  absolute max as defined in "Absolute Maximum DC Ratings"

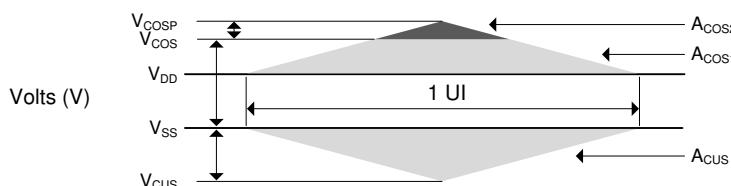


Figure 193. Clock Overshoot and Undershoot Definition

## Data, Strobe and Mask Overshoot and Undershoot Specifications

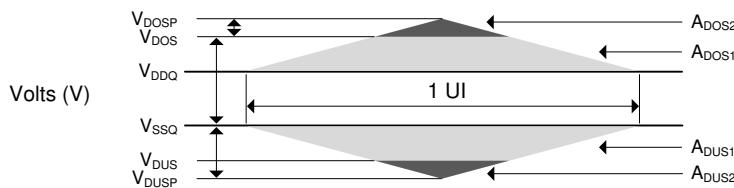
**Table 81. AC overshoot/undershoot specification for Data, Strobe and Mask**

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{DOSP}$	Maximum peak amplitude above $V_{DOS}$	0.16	V	
$V_{DOS}$	Upper boundary of overshoot area $A_{DOS1}$	$V_{DDQ} + 0.24$	V	1
$V_{DUS}$	Lower boundary of undershoot area $A_{DUS1}$	0.30	V	2
$V_{DUSP}$	Maximum peak amplitude below $V_{DUS}$	0.10	V	
$A_{DOS2}$	Maximum overshoot area per 1 UI above $V_{DOS}$	0.0100	V-ns	
$A_{DOS1}$	Maximum overshoot area per 1 UI between $V_{DDQ}$ and $V_{DOS}$	0.0700	V-ns	
$A_{CUS1}$	Maximum undershoot area per 1 UI between $V_{SSQ}$ and $V_{DUS}$	0.0700	V-ns	
$A_{CUS2}$	Maximum undershoot area per 1 UI below $V_{DUS}$	0.0100	V-ns	

(DQ, DQS, DQS#, DM#, DBI#)

Note 1. The value of  $V_{DOS}$  matches  $(V_{IN}, V_{OUT})$  max as defined in "Absolute Maximum DC Ratings". Absolute Maximum DC Ratings if  $V_{DDQ}$  equals  $V_{DDQ}$  max as defined in "Recommended DC Operating Conditions". If  $V_{DDQ}$  is above the recommended operating conditions,  $V_{DOS}$  remains at  $(V_{IN}, V_{OUT})$  max as defined in "Absolute Maximum DC Ratings"

Note 2. The value of  $V_{DUS}$  matches  $(V_{IN}, V_{OUT})$  min as defined in "Absolute Maximum DC Ratings".



**Figure 194. Data, Strobe and Mask Overshoot and Undershoot Definition**

Table 82. Capacitance

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$C_{IO}$	Input/output capacitance	0.55	1	pF	1,2,3
$C_{DIO}$	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
$C_{DDQS}$	Input/output capacitance delta DQS and DQS#	-	0.05	pF	1,2,3,5
$C_{CK}$	Input capacitance, CK and CK#	0.15	0.7	pF	1,3
$C_{DCK}$	Input capacitance delta CK and CK#	-	0.05	pF	1,3,4
$C_I$	Input capacitance(CTRL, ADD, CMD pins only)	0.15	0.55	pF	1,3,6
$C_{DI\_CTRL}$	Input capacitance delta (All CTRL pins only)	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	pF	1,2,9,10
$C_{ALERT}$	Input/output capacitance of ALERT	0.5	1.5	pF	1,3
$C_{ZQ}$	Input/output capacitance of ZQ	-	2.3	pF	1,3,12
$C_{TEN}$	Input capacitance of TEN	0.15	2.3	pF	1,3,13

Note 1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L and C parasitic. The capacitance is measured with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  applied with all other signal pins floating. Measurement procedure TBD. Used to define a differential signal slew-rate.

Note 2. DQ, DM#, DQS, DQS#. Although the DM pins have different functions, the loading matches DQ and DQS.

Note 3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

Note 4. Absolute value CK-CK#.

Note 5. Absolute value of  $C_{IO}(DQS) - C_{IO}(DQS\#)$ .

Note 6.  $C_I$  applies to ODT, CS#, CKE, A0-A16, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14, ACT# and PAR.

Note 7.  $C_{DI\_CTRL}$  applies to ODT, CS# and CKE.

Note 8.  $C_{DI\_CTRL} = C_I(CLOCK) - 0.5 \times (C_I(CLK) + C_I(CLK\#))$ .

Note 9.  $C_{DI\_ADD\_CMD}$  applies to, A0-A16, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14, ACT# and PAR.

Note 10.  $C_{DI\_ADD\_CMD} = C_I(ADD\_CMD) - 0.5 \times (C_I(CLK) + C_I(CLK\#))$ .

Note 11.  $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS) + C_{IO}(DQS\#))$ .

Note 12. Maximum external load capacitance on ZQ pin: TBD pF.

Note 13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to  $V_{SS}$ . In this case  $C_{TEN}$  might not be valid and system shall verify TEN signal with vendor specific information.

**Table 83. DRAM package electrical specifications**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$Z_{IO}$	Input/output Zpkg	45	85	$\Omega$	1,2,4,5,10
$T_{dIO}$	Input/output Pkg Delay	14	45	ps	1,3,4,5,10
$L_{io}$	Input/Output Lpkg	-	3.4	nH	10,11
$C_{io}$	Input/Output Cpkg	-	0.82	pF	10,12
$Z_{IO\ DQS}$	DQS, DQS# Zpkg	45	85	$\Omega$	1,2,5,10
$T_{dIO\ DQS}$	DQS, DQS# Pkg Delay	14	45	ps	1,3,5,10
$L_{IO\ DQS}$	DQS Lpkg	-	3.4	nH	10,11
$C_{IO\ DQS}$	DQS Cpkg	-	0.82	pF	10,12
$DZ_{DIO\ DQS}$	Delta Zpkg UDQS, UDQS#	-	10.5	$\Omega$	1,2,5,7
	Delta Zpkg LDQS, LDQS#	-	10.5	$\Omega$	1,3,5,7
$D_{TdDIO\ DQS}$	Delta Delay UDQS, UDQS#	-	5	ps	1,2,5,9,10
	Delta Delay LDQS, LDQS#	-	5	ps	1,3,5,9,10
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	50	90	$\Omega$	10,11
$T_{dI\ CTRL}$	Input CTRL pins Pkg Delay	14	42	ps	10,12
$L_{I\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1,2,5,8,10
$C_{I\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1,3,5,8,10
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	$\Omega$	10,11
$T_{dIADD\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	10,12
$L_{I\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1,2,5,10
$C_{I\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1,3,5,10
$Z_{CK}$	CLK# Zpkg	50	90	$\Omega$	10,11
$Td_{CK}$	CLK# Pkg Delay	14	42	ps	10,12
$L_{I\ CLK}$	Input CLK Lpkg	-	3.4	nH	1,2,5,6
$C_{I\ CLK}$	Input CLK Cpkg	-	0.7	pF	1,3,5,6
$DZ_{DCK}$	Delta Zpkg CLK#	-	10.5	$\Omega$	1,2,5,10
$D_{TdCK}$	Delta Delay CLK#	-	5	ps	1,3,5,10
$Z_{OZQ}$	ZQ Zpkg	-	100	$\Omega$	1,2,5,10
$Td_{OZQ}$	ZQ Delay	20	90	ps	1,3,5,10
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	$\Omega$	1,2,4,5,10
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	1,3,4,5,10

Note 1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  shorted with all other signal pins floating. The inductance is measured with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  shorted and all other signal pins shorted at the die side (not pin). Measurement procedure TBD.

Note 2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Z_{pkg} (\text{total per pin}) = \sqrt{L_{pkg} \times C_{pkg}}$$

Note 3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$T_{pkg} (\text{total per pin}) = \sqrt{L_{pkg} \times C_{pkg}}$$

Note 4.  $Z_{IO}$  and  $T_{dIO}$  applies to DQ, DM.

Note 5. This parameter applies to monolithic devices only.

Note 6. Absolute value of  $Z_{CK}$ - $Z_{CK\#}$  for impedance(Z) or absolute value of  $T_{dCK}$ - $T_{dCK\#}$  for delay(Td).

Note 7. Absolute value of  $Z_{IO\ (DQS)}$ - $Z_{IO\ (DQS\#)}$  for impedance(Z) or absolute value of  $T_{dIO\ (DQS)}$ - $T_{dIO\ (DQS\#)}$  for delay(Td).

Note 8.  $Z_{IADD\ CMD}$  &  $T_{dIADD\ CMD}$  applies to A0-A13, ACT#, BA0-BA1, BG0, RAS#/A16, CAS#/A15, WE#/A14 and PAR.

Note 9.  $Z_{I\ CTRL}$  &  $T_{dI\ CTRL}$  applies to ODT, CS# and CKE.

Note 10. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.

Note 11. It is assumed that Lpkg can be approximated as  $L_{pkg} = Z_{OZQ} \times Td$ .

Note 12. It is assumed that Cpkg can be approximated as  $C_{pkg} = Td/Z_{OZQ}$ .

## I<sub>DD</sub> and I<sub>DDQ</sub> Specification Parameters and Test conditions

In this chapter, I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurement conditions such as test load and patterns are defined and setup and test load for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurements are also described here.

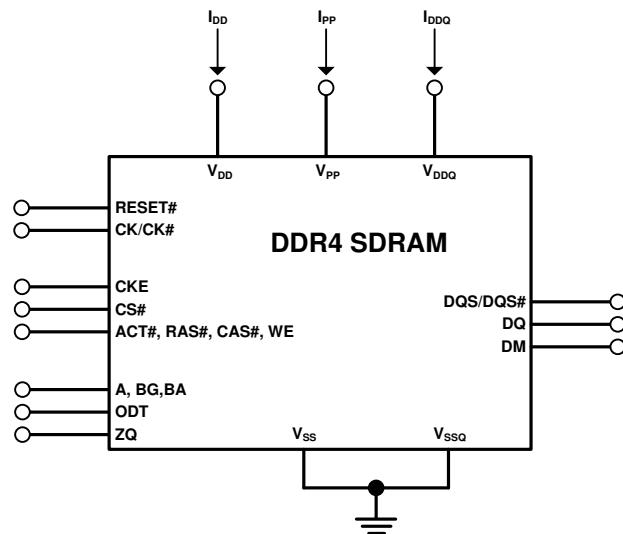
- I<sub>DD</sub> currents (I<sub>DD0</sub>, I<sub>DD1</sub>, I<sub>DD2N</sub>, I<sub>DD2NT</sub>, I<sub>DD2P</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3P</sub>, I<sub>DD4R</sub>, I<sub>DD4W</sub>, I<sub>DD5B</sub>, I<sub>DD6N</sub>, I<sub>DD6E</sub>, I<sub>DD6R</sub>, I<sub>DD6A</sub>, I<sub>DD7</sub>, and I<sub>DD8</sub>) are measured as time-averaged currents with all V<sub>DD</sub> balls of the device under test grouped together.
- I<sub>PP</sub> currents are I<sub>PP3N</sub> for standby cases (I<sub>DD2N</sub>, I<sub>DD2NT</sub>, I<sub>DD2P</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3P</sub>, I<sub>DD8</sub>), I<sub>PP0</sub> for active cases (I<sub>DD0</sub>, I<sub>DD1</sub>, I<sub>DD4R</sub>, I<sub>DD4W</sub>), I<sub>PP5B</sub> for the distributed refresh case (I<sub>DD5B</sub>), I<sub>PP6x</sub> for self refresh cases (I<sub>DD6N</sub>, I<sub>DD6E</sub>, I<sub>DD6R</sub>, I<sub>DD6A</sub>) and I<sub>PP7</sub> for the operating bank interleave read case (I<sub>DD7</sub>). These have the same definitions as the I<sub>DD</sub> currents referenced but are measured on the V<sub>PP</sub> supply.
- I<sub>DDQ</sub> currents are measured as time-averaged currents with V<sub>DDQ</sub> balls of the device under test grouped together. The device does not specify IDDQ currents.
- I<sub>PP</sub> and I<sub>DDQ</sub> currents are not included in I<sub>DD</sub> currents, I<sub>DD</sub> and I<sub>DDQ</sub> currents are not included in I<sub>PP</sub> currents, and I<sub>DD</sub> and I<sub>PP</sub> currents are not included in I<sub>DDQ</sub> currents.

Note: I<sub>DDQ</sub> values cannot be directly used to calculate the I/O power of the device. They can be used to support correlation of simulated I/O power to actual I/O power. In DRAM module application, I<sub>DDQ</sub> cannot be measured separately because V<sub>DD</sub> and V<sub>DDQ</sub> are using a merged-power layer in the module PCB.

The following definitions apply for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurements.

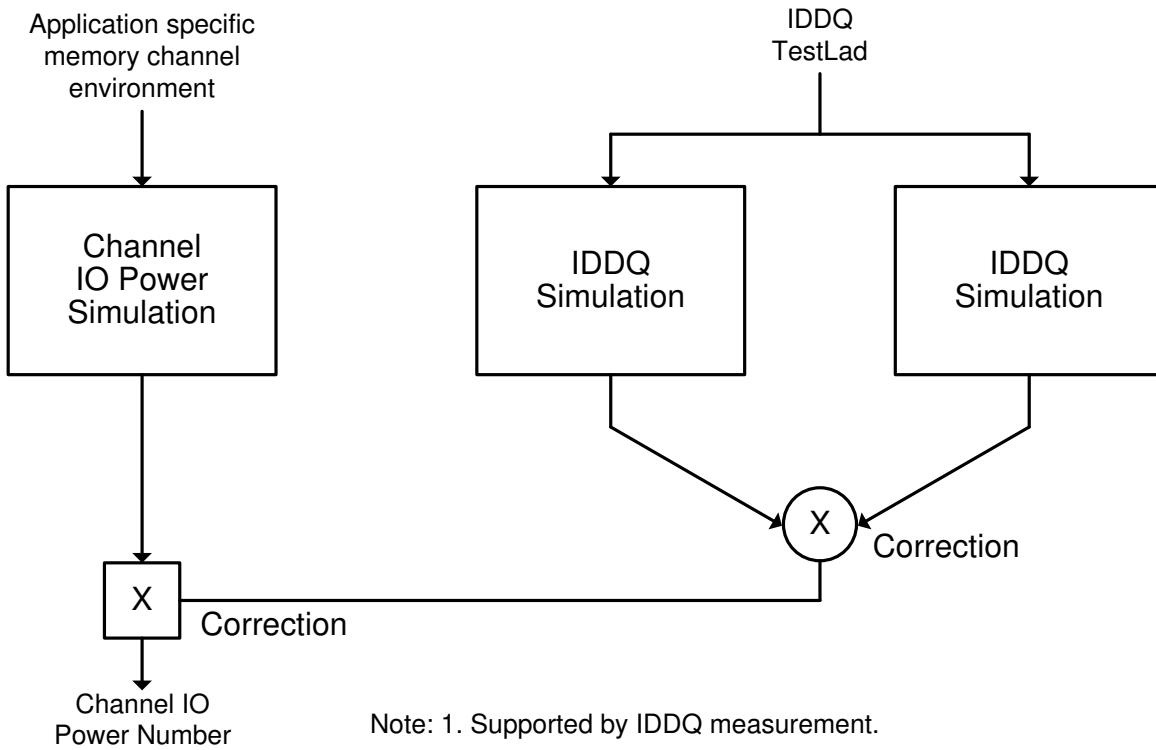
- “0” and “LOW” is defined as V<sub>IN</sub> ≤ V<sub>ILAC(max)</sub>.
- “1” and “HIGH” is defined as V<sub>IN</sub> ≥ V<sub>IHAC(min)</sub>.
- “MID-LEVEL” is defined as inputs are V<sub>REF</sub> = V<sub>DD</sub> / 2.
- Timings used for I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurement-loop patterns are provided in the Current Test Definition and Patterns section.
- Basic I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurement conditions are described in the Current Test Definition and Patterns section.
- Detailed I<sub>DD</sub>, I<sub>PP</sub> and I<sub>DDQ</sub> measurement-loop patterns are described in the Current Test Definition and Patterns section.
- Current measurements are done after properly initializing the device. This includes, but is not limited to, setting:
  - R<sub>ON</sub> = RZQ/7 (34 Ohm in MR1);
  - R<sub>TT\_NOM</sub> = RZQ/6 (40 Ohm in MR1);
  - R<sub>TT\_WR</sub> = RZQ/2 (120 Ohm in MR2);
  - R<sub>TT\_PARK</sub> = Disable;
  - Qoff = 0B (Output Buffer enabled) in MR1
  - CRC disabled in MR2;
  - CA parity feature disabled in MR5;
  - Gear down mode disabled in MR3
  - Read/Write DBI disabled in MR5;
  - DM disabled in MR5
- Define D = {CS#, RAS#, CAS#, WE#} := {HIGH, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D# = {CS#, RAS#, CAS#, WE#} := {HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

Note: The measurement-loop patterns must be executed at least once before actual current measurements can be taken.



NOTE 1. DIMM level Output test load condition may be different from above.

**Figure 195. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements**



**Figure 196. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement**

**Table 84. Timings used for IDD, IPP and IDDQ Measurement**

Symbol	DDR4-3200	Unit	
tCK	0.625	ns	
CL	22	nCK	
CWL	20	nCK	
nRCD	22	nCK	
nRC	74	nCK	
nRAS	52	nCK	
nRP	22	nCK	
nFAW	x4	16	nCK
	x8	34	nCK
	x16	48	nCK
nRRDS	x4	4	nCK
	x8	4	nCK
	x16	9	nCK
nRRDL	x4	8	nCK
	x8	8	nCK
	x16	11	nCK
tCCD_S	4	nCK	
tCCD_L	8	nCK	
tWTR_S	4	nCK	
tWTR_L	12	nCK	
nREFI	12,480	nCK	
nRFC 16Gb	560	nCK	

**Table 85. Basic IDD, IPP and IDDQ Measurement Conditions**

Symbol	Description
IDD0	<p><b>Operating One Bank Active-Precharge Current (AL=0)</b>            CKE: High; External clock: On; tCK, nRC, nRAS, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see IDD Loop table</p>
IPP0	<p><b>Operating One Bank Active-Precharge IPP Current</b>            Same condition with IDD0</p>
IDD1	<p><b>Operating One Bank Active-Read-Precharge Current (AL=0)</b>            CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to IDD Loop table; DM#: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see IDD Loop table</p>
IPP1	<p><b>Operating One Bank Active-Read-Precharge IPP Current</b>            Same condition with IDD1</p>
IDD2N	<p><b>Precharge Standby Current (AL=0)</b>            CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see IDD Loop table</p>
IPP2N	<p><b>Precharge Standby IPP Current</b>            Same condition with IDD2N</p>
IDD2NT	<p><b>Precharge Standby ODT Current</b>            CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VSSQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: toggling according to IDD Loop table; Pattern Details: see to IDD Loop table</p>
IDD2P	<p><b>Precharge Power-Down Current</b>            CKE: Low; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0</p>
IPP2P	<p><b>Precharge Power-Down IPP Current</b>            Same condition with IDD2P</p>
IDD2Q	<p><b>Precharge Quiet Standby Current</b>            CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0</p>
IDD3N	<p><b>Active Standby Current</b>            CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see IDD Loop table</p>
IPP3N	<p><b>Active Standby IPP Current</b>            Same condition with IDD3N</p>
IDD3P	<p><b>Active Power-Down Current</b>            CKE: Low; External clock: On; tCK, CL: see IDD timing Table; BL: 8<sup>1</sup>; AL: 0; CS#: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM#: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0</p>
IPP3P	<p><b>Active Power-Down IPP Current</b>            Same condition with IDD3P</p>
IDD4R	<p><b>Operating Burst Read Current</b>            CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8<sup>1</sup>; AL: 0; CS#: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: seamless read data burst with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers<sup>2</sup>; ODT Signal: stable at 0; Pattern Details: see IDD Loop table</p>
IPP4R	<p><b>Operating Burst Read IPP Current</b>            Same condition with IDD4R</p>

IDD4W	<b>Operating Burst Write Current</b> CKE: High; External clock: On; tCK, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: seamless write data burst with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at HIGH; Pattern Details: see IDD Loop table
IDD4WA	<b>Operating Burst Write Current (AL=CL-1)</b> AL = CL-1, Other conditions: see IDD4W
IPP4W	<b>Operating Burst Write IPP Current</b> Same condition with IDD4W
IDD5B	<b>Burst Refresh Current (1X REF)</b> CKE: High; External clock: On; tCK, CL, nRFC: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: VDDQ; DM#: stable at 1; Bank Activity: REF command every nRFC (see IDD Loop table); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IPP5B	<b>Burst Refresh Write IPP Current (1X REF)</b> Same condition with IDD5B
IDD6N	<b>Self Refresh Current: Normal Temperature Range</b> T <sub>CASE</sub> : 0 - 85°C; Auto Self Refresh (ASR) : disabled <sup>3</sup> ; Self refresh temperature range (SRT): normal <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: VDDQ; DM#: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6N	<b>Self Refresh IPP Current: Normal Temperature Range</b> Same condition with IDD6N
IDD6E	<b>Self-Refresh Current: Extended Temperature Range<sup>4</sup></b> T <sub>CASE</sub> : 0 - 95°C; Auto Self Refresh (ASR): disabled <sup>4</sup> ; Self refresh temperature range (SRT): Extended <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: VDDQ; DM#:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6E	<b>Self Refresh IPP Current: Extended Temperature Range</b> Same condition with IDD6E
IDD6R	<b>Self-Refresh Current: Reduced Temperature Range</b> T <sub>CASE</sub> : 0 - 45°C; Auto Self Refresh (ASR): disabled; Self refresh temperature range (SRT): Reduced <sup>4</sup> ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: 0; CS#, Command, Address, Bank Group Address, Bank Address, Data IO: VDDQ; DM#:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL
IPP6R	<b>Self Refresh IPP Current: Reduced Temperature Range</b> Same condition with IDD6R
IDD7	<b>Operating Bank Interleave Read Current</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see IDD timing table; BL: 8 <sup>1</sup> ; AL: CL-1; CS#: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD Loop table; Data IO: read data bursts with different data between one burst and the next one according to IDD Loop table; DM#: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD Loop table; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: see IDD Loop table
IPP7	<b>Operating Bank Interleave Read IPP Current</b> Same condition with IDD7

Note 1. Burst Length: BL8 fixed by MRS: set MR0 A[1:0] =00.

Note 2. Output Buffer Enable: set MR1 A12 = 0: Qoff = Output buffer enabled; set MR1 A[2:1] = 00: Output Driver Impedance Control = RZQ/7; R<sub>TT\_NOM</sub> enable: set MR1 A[10:8] = 011: R<sub>TT\_NOM</sub> = RZQ/6; R<sub>TT\_WR</sub> enable: set MR2 A[11:9] = 001: R<sub>TT\_WR</sub> = RZQ/2, and R<sub>TT\_PARK</sub> disable: set MR5 A[8:6] = 000.

Note 3. Auto self refresh (ASR): set MR2 A[6] 0 to disable or MR2 A[6] 1 to enable feature.

Note 4. Self refresh temperature range (SRT): set MR2 A[7] = 0 for normal or MR2 A[7] = 1 for extended temperature range.

Note 5. READ burst type: Nibble sequential, set MR0[3] 0.

**Table 86. IDD0 and IPP0 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	1-2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	3-4	D#,D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
	0	...	Repeat pattern 1...4 until nRAS - 1; truncate if necessary																
	0	nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	-	
	0	...	Repeat pattern 1...4 until nRC - 1; truncate if necessary																
	1	1×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=1 instead																
	2	2×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																
	3	3×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=3 instead																
	4	4×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																
	5	5×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=2 instead																
	6	6×nRC	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																
	7	7×nRC	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=0 instead																
	8	8×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																
	9	9×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=1 instead																
	10	10×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																
	11	11×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=3 instead																
	12	12×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																
	13	13×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=2 instead																
	14	14×nRC	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																
	15	15×nRC	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=0 instead																

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

For x4  
and  
x8 only

**Table 87. IDD1 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	1-2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	3-4	D#,D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	
		0	...																
		0	nRCD-AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00	
		0	...															D4=FF, D5=00	
		0	nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	D6=00, D7=FF	
		0	...																
		1	1×nRC+0	ACT	0	0	0	1	1	0	1	1	0	0	0	0	0	-	
		1	1×nRC+1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1×nRC+3,4	D#,D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	
		1	...																
		1	1×nRC +nRCD-AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
		1	...																
		1	1×nRAS+nRAS	PRE	0	1	0	1	0	0	1	1	0	0	0	0	0		
		1	...																
		2	2×nRC																
		3	3×nRC																
		4	4×nRC																
		5	5×nRC																
		6	6×nRC																
		7	7×nRC																
		8	9×nRC																
		9	10×nRC																
		10	11×nRC																
		11	12×nRC																
		12	13×nRC																
		13	14×nRC																
		14	15×nRC																
		15	16×nRC																

Note 1. DQS, DQS# are VDDQ when not toggling.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V<sub>DDQ</sub>.

For x4  
and  
x8 only

**Table 88. IDD2N, IDD3N, and IDD3P Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	2	D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
	0	3	D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
	1	4-7	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=1 instead																
	2	8-11	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																
	3	12-15	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=3 instead																
	4	16-19	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead																
	5	20-23	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead																
	6	24-27	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead																
	7	28-31	Repeat sub-loop 0, use BG[1:0]=1, BA[1:0]=0 instead																
	8	32-35	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead																
	9	36-39	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=1 instead																
	10	40-43	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead																
	11	44-47	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=3 instead																
	12	48-51	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead																
	13	52-55	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=2 instead																
	14	56-59	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead																
	15	60-63	Repeat sub-loop 0, use BG[1:0]=3, BA[1:0]=0 instead																

Note 1. DQS, DQS# are  $V_{DDQ}$ .

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are  $V_{DDQ}$ .

**Table 89. IDD2NT Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 [2]	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	0	2	D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
	0	3	D#	1	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-
	1	4-7	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 1 instead																
	2	8-11	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 2 instead																
	3	12-15	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 3 instead																
	4	16-19	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 1 instead																
	5	20-23	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 2 instead																
	6	24-27	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 3 instead																
	7	28-31	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 0 instead																
	8	32-35	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 0 instead															For x4 and x8 only	
	9	36-39	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 1 instead																
	10	40-43	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 2 instead																
	11	44-47	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 3 instead																
	12	48-51	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 1 instead																
	13	52-55	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 2 instead																
	14	56-59	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 3 instead																
	15	60-63	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 0 instead																

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

**Table 90. IDD4R Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
	0	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
	0	2-3	D#,D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
	1	4	RD	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
	1	5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
	1	6-7	D#,D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
	2	8-11																Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead	
	3	12-15																Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=3 instead	
	4	16-19																Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead	
	5	20-23																Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=2 instead	
	6	24-27																Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead	
	7	28-31																Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=0 instead	
	8	32-35																Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead	
	9	36-39																Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=1 instead	
	10	40-43																Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead	
	11	44-47																Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=3 instead	
	12	48-51																Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead	
	13	52-55																Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=2 instead	
	14	56-59																Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead	
	15	60-63																Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=0 instead	

Note 1. DQS, DQS# are V<sub>DQ</sub> when not toggling.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command.

For x4  
and  
x8 only

**Table 91. IDD4W Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
		0	1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
		0	2-3	D#,D#	1	1	1	1	0	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	
		1	4	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
		1	5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
		1	6-7	D#,D#	1	1	1	1	0	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	For x4 and x8 only
		2	8-11																
		3	12-15																
		4	16-19																
		5	20-23																
		6	24-27																
		7	28-31																
		8	32-35																
		9	36-39																
		10	40-43																
		11	44-47																
		12	48-51																
		13	52-55																
		14	56-59																
		15	60-63																

Note 1. DQS, DQS# are VDDQ when not toggling.

Note 2. BG1 is don't care and AL is not supported for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Write Command.

**Table 92. IDD4WC Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggling Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF, D8=CRC
	0	1-2	D,D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	D3=00 D4=FF, D5=00
	0	3-4	D#,D#	1	1	1	1	0	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	D6=00, D7=FF, D8=CRC	
	0	5	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF	
	0	6-7	D,D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	D4=00, D5=FF D6=FF, D7=00	
	0	8-9	D#,D#	1	1	1	1	0	1	3 <sup>[2]</sup>	3	0	0	0	7	F	0	D8=CRC	
	2	10-14																	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=2 instead
	3	15-19																	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=3 instead
	4	20-24																	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=1 instead
	5	25-29																	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=2 instead
	6	30-34																	Repeat sub-loop 0, use BG[1:0]=0, BA[1:0]=3 instead
	7	35-39																	Repeat sub-loop 1, use BG[1:0]=1, BA[1:0]=0 instead
	8	40-44																	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=0 instead
	9	45-49																	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=1 instead
	10	50-54																	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=2 instead
	11	55-59																	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=3 instead
	12	60-64																	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=1 instead
	13	65-69																	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=2 instead
	14	70-74																	Repeat sub-loop 0, use BG[1:0]=2, BA[1:0]=3 instead
	15	75-79																	Repeat sub-loop 1, use BG[1:0]=3, BA[1:0]=0 instead

Note 1. DQS, DQS# are V<sub>DDQ</sub> when not toggling.

Note 2. BG1 is don't care for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Write Command.

Note 4. Pattern provided for reference only.

For x4  
and  
x8 only

**Table 93. IDD5B Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>		
Toggling Static High		0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	-			
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	-			
		1	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	-			
		1	3	D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-		
		1	4	D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	7	F	0	-		
		1	5-8	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=1 instead																	
		1	9-12	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=2 instead																	
		1	13-16	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=3 instead																	
		1	17-20	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=1 instead																	
		1	21-24	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=2 instead																	
		1	25-28	Repeat pattern 1...4, use BG[1:0]=0, BA[1:0]=3 instead																	
		1	29-32	Repeat pattern 1...4, use BG[1:0]=1, BA[1:0]=0 instead																	
		1	33-36	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=0 instead												For x4 and x8 only					
		1	37-40	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=1 instead																	
		1	41-44	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=2 instead																	
		1	45-48	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=3 instead																	
		1	49-52	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=1 instead																	
		1	53-56	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=2 instead																	
		1	57-60	Repeat pattern 1...4, use BG[1:0]=2, BA[1:0]=3 instead																	
		1	61-64	Repeat pattern 1...4, use BG[1:0]=3, BA[1:0]=0 instead																	
		2	65...nRFC-1	Repeat sub-loop 1, Truncate, if necessary																	

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care for x16 device.

Note 3. DQ signals are V<sub>DDQ</sub>.

**Table 94. IDD7 Measurement - Loop Pattern<sup>[1]</sup>**

CK/ CK#	CKE	Sub- Loop	Cycle Number	CMD	CS#	ACT#	RAS#/A16	CAS#/A15	WE#/A14	ODT	BG0-1 <sup>[2]</sup>	BA0-1	A12/ BC#	A13, A11	A10	A9-A7	A6-A3	A2-A0	Data <sup>[3]</sup>
Toggle Static High	nRRD	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	1	RDA	0	1	1	0	1	0	0	0	0	0	1	0	0	-	
		0	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	-	
		0	3	D#	1	1	1	1	1	0	3 <sup>[2]</sup>	3	0	0	0	0	7	F	0
		0	...	Repeat pattern 2...3, until nRRD - 1, if nRRD > 4. Truncate if necessary															
		1	nRRD	ACT	0	0	0	0	0	0	1	1	0	0	0	0	0	-	
		1	nRRD+1	RDA	0	1	1	0	1	0	1	1	0	0	1	0	0	-	
		1	...	Repeat pattern 2...3, until 2×nRRD - 1, if nRRD > 4. Truncate if necessary															
		2	2×nRRD	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead															
		3	3×nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead															
		4	4×nRRD	Repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4 × nRRD. Truncate if necessary															
		5	nFAW	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead															
		6	nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead															
		7	nFAW+ 2×nRRD	Repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead															
		8	nFAW+ 3×nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead															
		9	nFAW+ 4×nRRD	Repeat Sub-Loop 4															
		10	2×nFAW	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead															
		11	2×nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead															
		12	2×nFAW+ 2×nRRD	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead															
		13	2×nFAW+ 3×nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead															
		14	2×nFAW+ 4×nRRD	Repeat Sub-Loop 4															
		15	3×nFAW	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead															
		16	3×nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead															
		17	3×nFAW+ 2×nRRD	Repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead															
		18	3×nFAW+ 3×nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead															
		19	3×nFAW+ 4×nRRD	Repeat Sub-Loop 4															
		20	4×nFAW	Repeat pattern 2 ... 3 until nRC - 1, if nRC > 4 × nFAW. Truncate if necessary															

Note 1. DQS, DQS# are V<sub>DDQ</sub>.

Note 2. BG1 is don't care for x16 device.

Note 3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V<sub>DDQ</sub>.

For x4  
and  
x8 only

Table 95. IDD and IDDQ Specification Parameters and Test conditions

Parameter	Symbol	DDR4-3200	Unit	
		Max.		
Operating One Bank Active-Precharge Current (AL=0)	$I_{DD0}$	70	mA	
Operating One Bank Active-Precharge IPP Current	$I_{PP0}$	4	mA	
Operating One Bank Active-Read-Precharge Current (AL=0)	$I_{DD1}$	84	mA	
Precharge Standby Current (AL=0)	$I_{DD2N}$	45	mA	
Precharge Standby ODT Current	$I_{DD2NT}$	58	mA	
Precharge Power-Down Current CKE	$I_{DD2P}$	38	mA	
Precharge Quiet Standby Current	$I_{DD2Q}$	42	mA	
Active Standby Current	$I_{DD3N}$	62	mA	
Active Standby IPP Current	$I_{PP3N}$	2	mA	
Active Power-Down Current	$I_{DD3P}$	51	mA	
Operating Burst Read Current	$I_{DD4R}$	193	mA	
Operating Burst Write Current	$I_{DD4W}$	141	mA	
Burst Refresh Current (1X REF)	$I_{DD5B}$	68	mA	
Burst Refresh Write IPP Current (1X REF)	$I_{PP5B}$	4	mA	
Self Refresh Current: Normal Temperature Range	$T_C = 0\text{~}85^\circ\text{C}^{*1}$	$I_{DD6N}$	53	mA
Self-Refresh Current: Extended Temperature Range)	$T_C = 0\text{~}95^\circ\text{C}^{*2,4}$	$I_{DD6E}$	90	mA
Self-Refresh Current: Reduced Temperature Range	$T_C = 0\text{~}45^\circ\text{C}^{*3,4}$	$I_{DD6R}$	20	mA
Auto Self-Refresh Current	$T_C = 25^\circ\text{C}^{*4}$	$I_{DD6A}$	11	mA
	$T_C = 45^\circ\text{C}^{*4}$		20	mA
	$T_C = 75^\circ\text{C}^{*4}$		51	mA
	$T_C = 95^\circ\text{C}^{*4}$		90	mA
Auto Self-Refresh IPP Current	$T_C = 0\text{~}95^\circ\text{C}^{*26}$	$I_{PP6A}$	6	mA
Operating Bank Interleave Read Current	$I_{DD7}$	200	mA	
Operating Bank Interleave Read IPP Current	$I_{PP7}$	13	mA	

Note 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0 ~ 85°C).

Note 2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0 ~ 95°C).

Note 3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0 ~ 45°C).

Note 4. IDD6R, IDD6A, and IDD6E values are verified by design and characterization, and may not be subject to production test.

Note 5. When additive latency is enabled for IDD0, current changes by approximately +1%.

Note 6. When additive latency is enabled for IDD1, current changes by approximately +5%.

Note 7. When additive latency is enabled for IDD2N, current changes by approximately +2%.

Note 8. When DLL is disabled for IDD2N, current changes by approximately +16%.

Note 9. When CAL is enabled for IDD2N, current changes by approximately -12%.

Note 10. When gear-down is enabled for IDD2N, current changes by approximately +2%.

Note 11. When CA parity is enabled for IDD2N, current changes by approximately +9%.

- Note 12. When additive latency is enabled for IDD3N, current changes by approximately -2%.
- Note 13. When additive latency is enabled for IDD4R, current changes by approximately +4%.
- Note 14. When read DBI is enabled for IDD4R, current changes by approximately +4%.
- Note 15. When additive latency is enabled for IDD4W, current changes by approximately -2%.
- Note 16. When write DBI is enabled for IDD4W, current changes by approximately +1%.
- Note 17. When write CRC is enabled for IDD4W, current changes by approximately -4%.
- Note 18. When CA parity is enabled for IDD4W, current changes by approximately +15%.
- Note 19. When 2X REF is enabled for IDD5R, current changes by approximately 0%.
- Note 20. When 4X REF is enabled for IDD5R, current changes by approximately 0%.
- Note 21. When 2X REF is enabled for IPP5R, current changes by approximately 0%.
- Note 22. When 4X REF is enabled for IPP5R, current changes by approximately 0%.
- Note 23. IPP0 test and limit is applicable for IDD0 and IDD1 conditions.
- Note 24. IPP3N test and limit is applicable for all IDD2x, IDD3x, IDD4x, and IDD8 conditions; that is, testing IPP3N should satisfy the IPPs for the noted IDD tests.
- Note 25. The IDD values must be derated (increased) when operated between  $85^{\circ}\text{C} < \text{TC} \leq 95^{\circ}\text{C}$ : IPP0, IDD7, and IPP7 must be derated by +3%; IDD0, IDD1, IPP3N, IDD4R and IDD4W must be derated by +13%; IDD2N, IDD2NT, IDD2Q, and IDD3N must be derated by 21%; IDD2P and IDD3P must be derated by +27%; IDD8 must be derated by +37%; IDD5R and IPP5R must be derated by +57%.
- Note 26. IPP6x is applicable to IDD6N, IDD6E, IDD6R, and IDD6A conditions.

**Table 97. Timing Parameters for DDR4-3200**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
tAA	Internal read command to first data	13.75	19 <sup>27</sup>	ns	23-25
tAA_DB1	Internal read command to first data with read DB1 enabled	$t_{AA(min)} + 4t_{CK}$	$t_{AA(max)} + 4t_{CK}$	ns	23-25
trCD	ACT to internal read or write delay time	13.75	-	ns	23-25
trP	PRE command period	13.75	-	ns	23-25
trAS	ACT to PRE command period	32	$9 \times t_{REFI}$	ns	23-25
trC	ACT to ACT or REF command period	45.75	-	ns	23-26
Speed Bins	CWL	Normal	Read DB1	Min.	Max.
tCK(avg)	ACT to ACT or REF command period	9	10	12	1.5
		9,11	11	13	1.25
		9,11	12	14	1.25
		10,12	13	15	1.071
		10,12	14	16	1.071
		11,14	15	18	0.937
		11,14	16	19	0.937
		12,16	17	20	0.833
		12,16	18	21	0.833
		14,18	19	22	0.75
		14,18	20	23	0.75
		16,20	21	25	0.682
		16,20	22	26	0.625
Clock Timing				Min.	Max.
tCK (DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)			8	20
tCK(avg)	Average clock period			0.625	1.9
tCH(avg)	Average high pulse width			0.48	0.52
tCL(avg)	Average low pulse width			0.48	0.52
tCK(abs)	Absolute Clock Period			$t_{CK(avg)}\min + t_{JIT(per)}\min\_tot$	$t_{CK(avg)}\max + t_{JIT(per)}\max\_tot$
tCH(abs)	Absolute clock high pulse width			0.45	-
tCL(abs)	Absolute clock low pulse width			0.45	-
JIT(per)_tot	Clock Period Jitter- total			-32	32
JIT(per)_dj	Clock Period Jitter deterministic			-16	16
tJIT(per,clk)	Clock Period Jitter during DLL locking period			-25	25
tJIT(cc)	Cycle to Cycle Period Jitter			-	62
tJIT(cc,clk)	Cycle to Cycle Period Jitter during DLL locking period			-	50
tERR(2per)	Cumulative error across 2 cycles			-46	46
tERR(3per)	Cumulative error across 3 cycles			-55	55
tERR(4per)	Cumulative error across 4 cycles			-61	61
tERR(5per)	Cumulative error across 5 cycles			-65	65
tERR(6per)	Cumulative error across 6 cycles			-69	69
tERR(7per)	Cumulative error across 7 cycles			-73	73
tERR(8per)	Cumulative error across 8 cycles			-76	76
tERR(9per)	Cumulative error across 9 cycles			-78	78
tERR(10per)	Cumulative error across 10 cycles			-80	80
tERR(11per)	Cumulative error across 11 cycles			-83	83
tERR(12per)	Cumulative error across 12 cycles			-84	84
tERR(nper)	Cumulative error across n =13, 14 . . . 49, 50 cycles			$t_{ERR(nper)}\min = ((1 + 0.68\ln(n)) \times t_{JIT(per)}\min)$ $t_{ERR(nper)}\max = ((1 + 0.68\ln(n)) \times t_{JIT(per)}\max)$	ps
tIS(base)	Command and Address setup time to CK, CK# referenced to V <sub>IH</sub> (AC)/V <sub>IL</sub> (AC) levels			40	-

$t_{IS}(V_{REF})$	Command and Address setup time to CK, CK# referenced to $V_{REF}$ levels	130	-	ps	
$t_{IH}(\text{base})$	Command and Address hold time to CK, CK# referenced to $V_{IH(\text{AC})}/V_{IL(\text{AC})}$ levels	65	-	ps	
$t_{IH}(V_{REF})$	Command and Address hold time to CK, CK# referenced to $V_{REF}$ levels	130	-	ps	
$t_{IPW}$	Control and Address Input pulse width for each input	340	-	ps	
<b>DQ Input Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
$t_{DS}$	Data setup time to DQS, DQS# -- Base (calibrated $V_{REF}$ )	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.28tCK )			
$t_{PDA\_S}$	Data setup time to DQS, DQS# -- Non-calibrated $V_{REF}$	minimum of 0.5UI			
$t_{DH}$	Data hold time from DQS, DQS# -- Base (calibrated $V_{REF}$ )	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.28tCK )			
$t_{PDA\_H}$	Data hold time to DQS, DQS# -- Non-calibrated $V_{REF}$	minimum of 0.5UI			
$t_{DIPW}$	DQ and DM minimum data pulse width for each input	0.58	-	UI	
<b>DQS Strobe Output Timing (DLL enabled)</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
$t_{DQSQ}$	DQS, DQS# to DQ skew, per group, per access	-	0.20	UI	
$t_{QH}$	DQ output hold time per group, per access from DQS,DQS#	0.70	-	UI	
$t_{DVWd}$	Data Valid Window per device per UI: ( $t_{QH} - t_{DQSQ}$ ) of each UI on a given DRAM	0.64	-	UI	
$t_{DVWp}$	Data Valid Window per pin per UI: ( $t_{QH} - t_{DQSQ}$ ) each UI on a pin of a given DRAM	0.72	-	UI	
$t_{LZ(DQ)}$	DQ low impedance time from CK, CK#	-250	160	ps	
$t_{HZ(DQ)}$	DQ high impedance time from CK, CK#	-	160	ps	
<b>Command and Address Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
$t_{CCD\_L}$	CAS# to CAS# command delay for same bank group	max(5nCK,5ns)	-	tCK	14
$t_{CCD\_S}$	CAS# to CAS# command delay for different bank group	4	-	tCK	
$t_{RRD\_S(2K)}$	Activate to Activate Command delay to different bank group for 2KB page size	max(4nCK,5.3ns)	-	tCK	1
$t_{RRD\_L(2K)}$	Activate to Activate Command delay to same bank group for 2KB page size	max(4nCK,6.4ns)	-	tCK	1
$t_{FAW\_2K}$	Four activate window for 2KB page size	max(28nCK,30ns)	-	ns	
$t_{WTR\_S}$	Delay from start of internal write transaction to internal read command for different bank group	max(2nCK,2.5ns)	-	tCK	5,7,8,9,1
$t_{WTR\_S2}$	Delay from start of internal write transaction to internal read command for different bank group	1CK + $t_{WTR\_S}$		tCK	5,7,8,10,1
$t_{WTR\_L}$	Delay from start of internal write transaction to internal read command for same bank group	max(4nCK,7.5ns)	-	tCK	5,9,1
$t_{WTR\_L2}$	Delay from start of internal write transaction to internal read command for same bank group	1CK + $t_{WTR\_L}$		tCK	5,10,1
$t_{RTP}$	Internal Read Command to Precharge Command delay	max(4nCK,7.5ns)	-	ns	1
$t_{WR}$	Write recovery time	15	-	tCK	5,9,1
$t_{WR2}$	Write recovery time	1CK + $t_{WR}$		tCK	5,10,1
$t_{WR\_CRC\_DM}$	Write recovery time when CRC and DM are enabled	$t_{WR} + \max(5nCK,3.75ns)$	-	tCK	6,9,1
$t_{WR\_CRC\_DM2}$	Write recovery time when CRC and DM are enabled	1CK + $t_{WR\_CRC\_DM}$		tCK	6,10,1
$t_{WTR\_S\_CRC\_DM}$	delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	$t_{WTR\_S} + \max(5nCK,3.75ns)$	-	tCK	6,7,8,9,1
$t_{WTR\_S\_CRC\_DM2}$	delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	1CK + $t_{WTR\_S\_CRC\_DM}$		tCK	6,7,8,10,1
$t_{WTR\_L\_CRC\_DM}$	delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L} + \max(5nCK,3.75ns)$	-	tCK	6,9,1
$t_{WTR\_L\_CRC\_DM2}$	delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	1CK + $t_{WTR\_L\_CRC\_DM}$		tCK	6,10,1
$t_{DLLK}$	DLL locking time	1024	-	tCK	2,4
$t_{MRD}$	Mode Register Set command cycle time	8	-	tCK	
$t_{MOD}$	Mode Register Set command update delay	max(24nCK,15ns)	-	tCK	1
$t_{MPRR}$	Multi-Purpose Register Recovery Time	1	-	tCK	
$t_{WR\_MPR}$	Multi Purpose Register Write Recovery Time	$t_{MOD(\min)} + AL + PL$	-	tCK	
$t_{DAL(\min)}$	Auto precharge write recovery + precharge time	Programmed WR + roundup ( $t_{RP}/ tCK(\text{avg})$ )			
<b>CS# to Command Address Latency</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
$t_{CAL}$	CS# to Command Address Latency	6	-	tCK	19
$t_{CALg}$	CS# to Command Address Latency in gear-down mode	8	-	tCK	
$t_{MRD\_CAL}$	Mode Register Set command cycle time in CAL mode	$t_{MOD} + t_{CAL}$	-	tCK	

tMOD_CAL	Mode Register Set update delay in CAL mode	tMOD + tCAL	-	tck	
<b>Data Strobe Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tRPRE	DQS, DQS# differential Read Preamble (1 clock preamble)	0.9	-	tck	20
tRPRE2	DQS, DQS# differential Read Preamble (2 clock preamble)	1.8	-	tck	20
tRPST	DQS, DQS# differential Read Postamble	0.33	-	tck	21
tQSH	DQS, DQS# differential output high time	0.4	-	tck	
tQL	DQS, DQS# differential output low time	0.4	-	tck	
tWPRE	DQS, DQS# differential Write Preamble (1 clock preamble)	0.9	-	tck	
tWPRE2	DQS, DQS# differential Write Preamble (2 clock preamble)	1.8	-	tck	
tWPST	DQS, DQS# differential Write Postamble	0.33	-	tck	
tLZ(DQS)	DQS, DQS# low impedance time (Referenced from RL-1)	-250	160	ps	
tHZ(DQS)	DQS, DQS# high impedance time (Referenced from RL+BL/2)	-	160	ps	
tDQSL	DQS, DQS# differential input low pulse width	0.46	0.54	tck	
tDQSH	DQS, DQS# differential input high pulse width	0.46	0.54	tck	
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge (1 clock preamble)	-0.27	0.27	tck	
tDQSS2	DQS, DQS# rising edge to CK, CK# rising edge (2 clock preamble)	-0.50	0.50	tck	
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tck	
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tck	
tDQSCK(DLL On)	DQS, DQS# rising edge output timing location from rising CK, CK# with DLL On mode	-160	160	ps	
tDQSCKI(DLL On)	DQS, DQS# rising edge output variance window per DRAM	-	260	ps	
<b>Calibration Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tzQinit	Power-up and Reset calibration time	1024	-	tck	
tzQoper	Normal operation Full calibration time	512	-	tck	
tzQCS	Normal operation Short calibration time	128	-	tck	
<b>Reset/Self Refresh Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
txPR	Exit Reset from CKE HIGH to a valid command	tRFC1(min) + 10ns	-	tck	1
tpW_RESET_S	RESET pulse low after power stable	1.0	-	us	
tpW_RESET_L	RESET pulse low at power-up	200	-	us	
tvDDPR	Begin power supply ramp to power supplies stable	-	200	ms	
trPS	RESET# LOW to power supplies stable	0	0	ns	
txS	Exit Self Refresh to commands not requiring a locked DLL	tRFC1(min) + 10ns	-	tck	1
txS_ABORT(min)	SRX to commands not requiring a locked DLL in Self Refresh ABORT	tRFC4(min) + 10ns	-	tck	1
txS_FAST(min)	Exit Self Refresh to ZQCL,ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tRFC4(min) + 10ns	-	tck	1
txSDLL	Exit Self Refresh to commands requiring a locked DLL	tDLLK(min)	-	tck	1
tCKESR	Minimum CKE low width for Self refresh entry to exit timing	tCKE(min) + 1nCK	-	tck	1
tCKESR_PAR	Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKE(min) + 1nCK + PL	-	tck	1
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	max(5nCK,10ns)	-	tck	1
tCKSRE_PAR	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	max(5nCK,10ns) + PL	-	tck	1
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	max(5nCK,10ns)	-	tck	1
<b>Power Down Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
txP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(4nCK, 6ns)	-	tck	1
txP_PAR	Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled.	max(4nCK, 6ns) + PL	-		1
tCKE	CKE minimum pulse width	max(3nCK, 5ns)	-	tck	1
tCPDED	Command pass disable delay	4	-	tck	
tpD	Power Down Entry to Exit Timing	tCKE(min)	9 x tREFI	tck	
tANPD	Begin power-down period prior to CKE registered HIGH	WL - 1CK		tck	
PDE	Power-down entry period: ODT either synchronous or asynchronous	Greater of tANPD or tRFC - Refresh command to CKE LOW time		tck	
PDX	Power-down exit period: ODT either synchronous or asynchronous	tANPD + tXSDLL		tck	
tACTPDEN	Timing of ACT command to Power Down entry	2	-	tck	

tPRPDEN	Timing of PRE or PREA command to Power Down entry	2	-	tck	
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	-	tck	1
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR/tCK(avg))	-	tck	1
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	tck	1
tWRPBC4DEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR/tCK(avg))	-	tck	1
tWRAPBC4DEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	tck	1
tREFPDEN	Timing of REF command to Power Down entry	2	-	tck	
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tck	1
<b>PDA Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tMRD_PDA	Mode Register Set command cycle time in PDA mode	max(16nCK, 10ns)	-	tck	1
tMOD_PDA	Mode Register Set command update delay in PDA mode	tMOD		tck	
<b>ODT Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
taONAS	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1.0	9.0	ns	
taOFAS	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1.0	9.0	ns	
tADC	RTT dynamic change skew	0.26	0.74	tck	
DODTLon	Direct ODT turn-on latency	WL - 2 = CWL + AL + PL - 2		tck	
DODTLoft	Direct ODT turn-off latency	WL - 2 = CWL + AL + PL - 2		tck	
<b>Write Leveling Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
twLMDR	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	tck	
twLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	tck	
twLS	Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	0.13	-	tck	
twLH	Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK# crossing	0.13	-	tck	
twLO	Write leveling output delay	0	9.5	ns	
twLOE	Write leveling output error	0	2	ns	
<b>CA Parity Timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tPAR_UNKNOWN	Commands not guaranteed to be executed during this time	-	PL	tck	
tPAR_ALERT_ON	Delay from errant command to ALERT# assertion	-	PL + 6ns	tck	
tPAR_ALERT_PW	Pulse width of ALERT# signal when asserted	96	192	tck	
tPAR_ALERT_RSP	Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	-	85	tck	
PL	Parity Latency	6	-	tck	
<b>CRC Error Reporting</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tcrc_ALERT	CRC error to ALERT# latency	3	13	ns	
tcrc_ALERT_PW	CRC ALERT# pulse width	6	10	tck	
<b>Geardown timing</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
txPR_GEAR	Exit Reset from CKE High to a valid MRS Gear Down (T2/ Reset)	txPR	-	tck	
txS_GEAR	CKE High Assert to Gear Down Enable time (T2/CKE)	txS	-	tck	
tsync_GEAR <sup>27</sup>	MRS command to Sync pulse time(T3)	tMOD + 4nCK		tck	
tcMD_GEAR <sup>27</sup>	Sync pulse to First valid command(T4)	tMOD	-	tck	
tGEAR_setup	Geardown setup time	2	-	tck	
tGEAR_hold	Geardown hold time	2	-	tck	
<b>tREFI</b>		<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Note</b>
tRFC1 (min)	16Gb	350	-	ns	
tRFC2 (min)	16Gb	260	-	ns	
tRFC4 (min)	16Gb	160	-	ns	
tREFI	Average periodic refresh interval	0°C ≤ T <sub>CASE</sub> ≤ 85°C	-	7.8	μs
		85°C ≤ T <sub>CASE</sub> ≤ 95°C	-	3.9	μs

Note 1. maximum limit not applicable.

Note 2. tDLLK values support the legacy JEDEC tDLLK specifications.

Note 3. DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.

Note 4. Data rate is greater than or equal to 1066 Mb/s.

Note 5. WRITE-to-READ when CRC and DM are both not enabled.

Note 6. WRITE-to-READ delay when CRC and DM are both enabled.

Note 7. Start of internal write transaction is defined as follows:

- For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
- For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

Note 8. For these parameters, the device supports  $t_{nCK} = \text{ROUND}\{t_{PARAM} [\text{ns}]/t_{CK} (\text{AVG}) [\text{ns}]\}$  according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.

Note 9. When operating in 1tCK WRITE preamble mode.

Note 10. When operating in 2tCK WRITE preamble mode.

Note 11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to tRFC refresh time.

Note 12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.

Note 13. Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.

Note 14. JEDEC specifies a minimum of five clocks.

Note 15. The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZ(DQS) MAX on the right side.

Note 16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately  $0.7 \times V_{DDQ}$  as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to  $V_{TT} = V_{DDQ}$ .

Note 17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.

Note 18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20-60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.

Note 19. The actual tCAL minimum is the larger of 3 clocks or 3.748ns/tCK; the table lists the applicable clocks required at targeted speed bin.

Note 20. The maximum READ preamble is bounded by tLZ(DQS) MIN on the left side and tDQSCK (MAX) on the right side. See figure in the Clock to Data Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2tCK toggle mode, as illustrated in the READ Preamble section.

Note 21. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.

Note 22. The tPDA\_S/tPDA\_H parameters may use the tDS/tDH limits, respectively, if the signal is LOW the entire BL8.

Note 23. Speed Bin table is only valid with DLL enabled.

Note 24. When operating in 2tCK write preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

Note 25. The programmed value of CWL must be less than or equal to the programmed value of CL.

Note 26. When calculating tRC in clocks, values may not be used in a combination that violate tRAS or tRP.

Note 27. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

## Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unit less ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

$$nCK = \text{ceiling} [ (\text{parameter\_in\_ns} / \text{application\_tCK\_in\_ns}) - 0.025 ]$$

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

$$nCK = \text{truncate} [ \{(\text{parameter\_in\_ps} \times 1000) / (\text{application\_tCK\_in\_ps}) + 974\} / 1000 ]$$

- Either algorithm yields identical results.

## The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

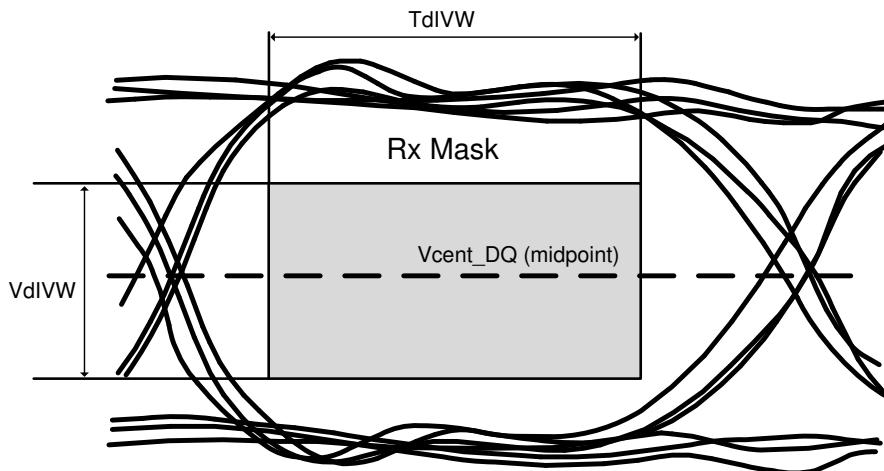


Figure 197. DQ Receiver(Rx) compliance mask

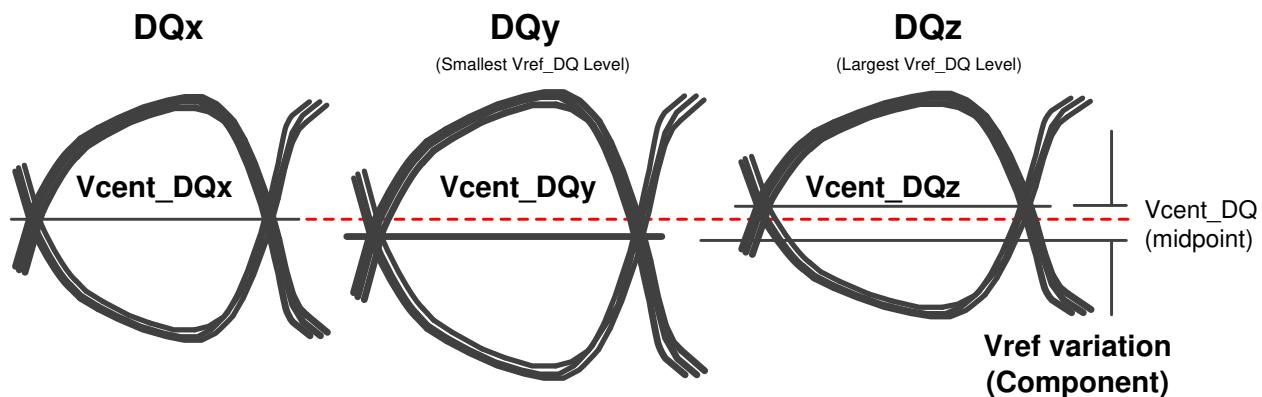
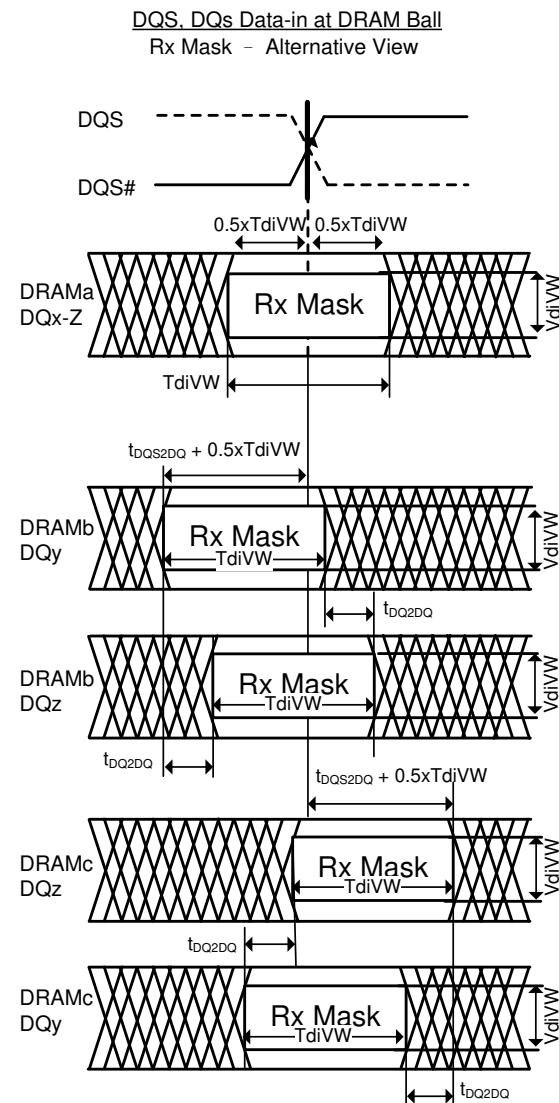
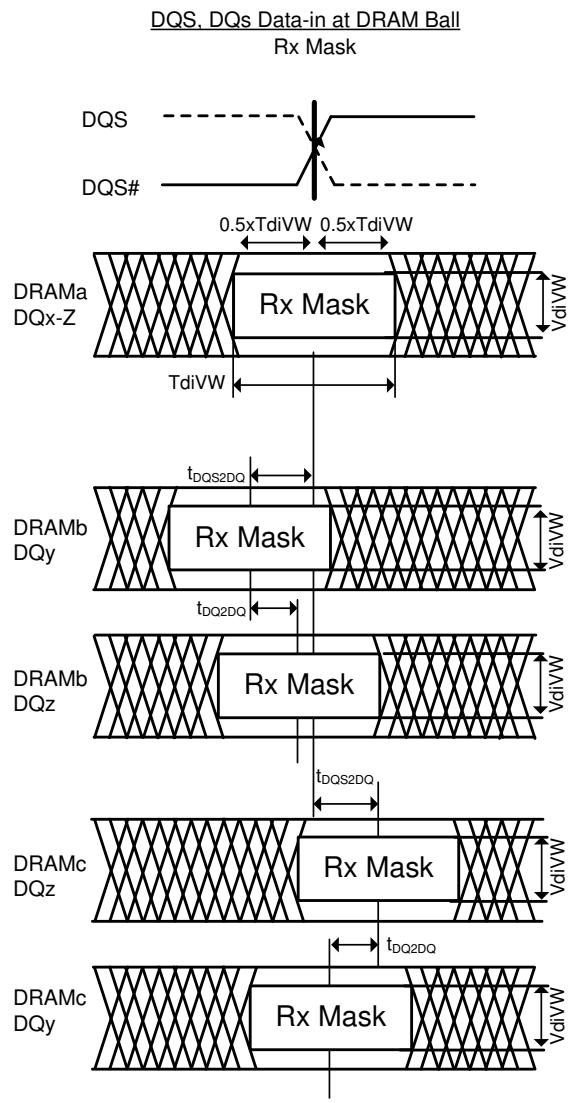


Figure 198. Vcent\_DQ Variation to Vcent\_DQ(midpoint)

The Vref\_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent\_DQ(midpoint), in order to have valid Rx Mask values.

Vcent\_DQ(midpoint) is defined as the midpoint between the largest Vref\_DQ voltage level and the smallest Vref\_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.



NOTE: DQx represents an optimally centered mask.

DQy represents earliest valid mask.

DQz represents latest valid mask.

NOTE: DRAMa represents a DRAM without any DQS/DQ skews.

DRAMb represents a DRAM with early skews (negative  $t_{DQS2DQ}$ ).

DRAMc represents a DRAM with delayed skews (positive  $t_{DQS2DQ}$ ).

NOTE: Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.

$TdiPW$  is not shown; composite data-eyes shown would violate  $TdiPW$ .

VCENT DQ (midpoint) is not shown but is assumed to be midpoint of  $VdiVW$ .

**Figure 199. DQS to DQ and DQ to DQ Timings at DRAM Balls**

All of the timing terms in figure are measured at the  $VdiVW$  voltage levels centered around  $V_{cent\_DQ}$  (midpoint) and are referenced to the DQS/DQS# center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in the figure below: A low to high transition  $t_{r1}$  is measured from  $0.5 \times V_{diVW(max)}$  below  $V_{cent\_DQ}$  (midpoint) to the last transition through  $0.5 \times V_{diVW(max)}$  above  $V_{cent\_DQ}$ (midpoint) while  $t_{r2}$  is measured from the last transition through  $0.5 \times V_{diVW(max)}$  above  $V_{cent\_DQ}$ (midpoint) to the first transition through the  $0.5 \times V_{IH\_AC(min)}$  above  $V_{cent\_DQ}$ (midpoint).

Rising edge slew rate equations:

$$srr1 = V_{diVW(max)} / t_{r1}$$

$$srr2 = (V_{IH\_AC(min)} - V_{diVW(max)}) / (2 \times t_{r2})$$

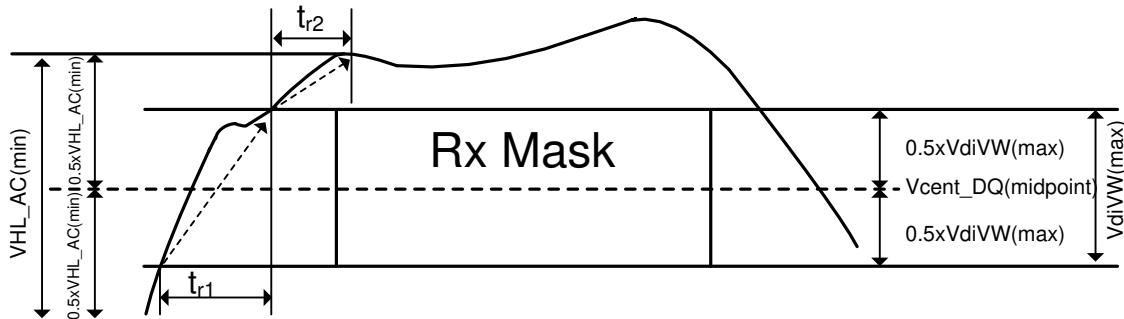


Figure 200. Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in the figure below: A high to low transition  $t_{f1}$  is measured from  $0.5 \times V_{diVW(max)}$  above  $V_{cent\_DQ}$  (midpoint) to the last transition through  $0.5 \times V_{diVW(max)}$  below  $V_{cent\_DQ}$ (midpoint) while  $t_{f2}$  is measured from the last transition through  $0.5 \times V_{diVW(max)}$  below  $V_{cent\_DQ}$ (midpoint) to the first transition through the  $0.5 \times V_{IH\_AC(min)}$  below  $V_{cent\_DQ}$ (pin mid).

Falling edge slew rate equations:

$$srf1 = V_{diVW(max)} / t_{f1}$$

$$srf2 = (V_{IH\_AC(min)} - V_{diVW(max)}) / (2 \times t_{f2})$$

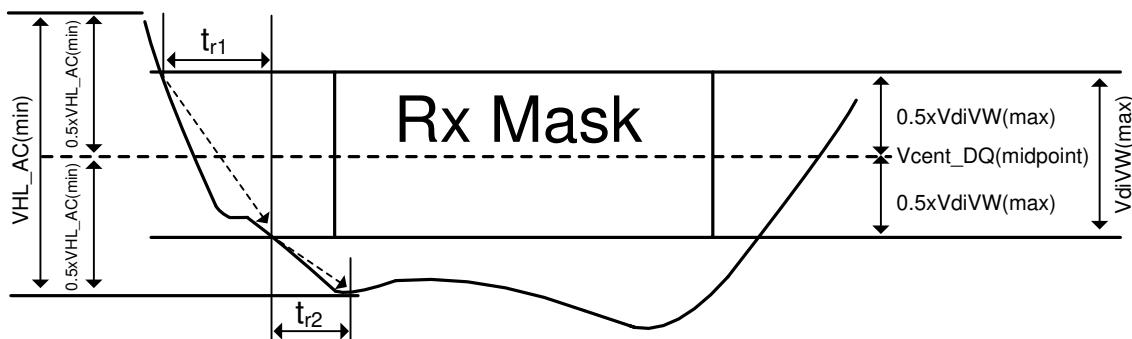


Figure 201. Slew Rate Conditions For Falling Transition

Table 98. DRAM DQs In Receive Mode; \* UI=tck(avg)min/2

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
VdIVW	Rx Mask voltage - pk-pk	-	110	mV	1,2,10
TdIVW	Rx timing window	-	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	140	-	mV	6,10
TdIPW	DQ input pulse width	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.22	0.22	UI*	6,10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.125	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >= 0.935ns	1.0	9	V/ns	8,10
	Input Slew Rate over VdIVW if 0.935ns > tCK >= 0.625ns	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2xsrr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2xsrf1	9	V/ns	9,10

Note 1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent\_DQ( midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a  $BER = 1^{e-16}$  when the RxMask is not violated. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).

Note 2. Defined over the DQ internal Vref range 1.

Note 3. Overshoot and Undershoot Specifications apply.

Note 4. DQ input pulse signal swing into the receiver must meet or exceed VIHL\_AC(min). VIHL\_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e., a valid TdIPW.

Note 5. Q minimum input pulse width defined at the Vcent\_DQ( midpoint).

Note 6. DQS to DQ offset is skew between DQS and DQs within a word (x16) at the DDR4 SDRAM balls over process, voltage, and temperature.

Note 7. DQ to DQ offset is skew between DQs within a word (x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.

Note 8. Input slew rate over VdIVW Mask centered at Vcent\_DQ( midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.

Note 9. Input slew rate between VdIVW Mask edge and VIHL\_AC(min) points.

Note 10. All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdIVW(min), VdIVW(max), and minimum slew rate limits, then either TdIVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

## AC and DC output Measurement levels

### Output Driver DC Electrical Characteristics

The DDR4 driver supports two different  $R_{ON}$  values. These  $R_{ON}$  values are referred as strong(low  $R_{ON}$ ) and weak mode(high  $R_{ON}$ ). A functional representation of the output buffer is shown in the figure below. Output driver impedance  $R_{ON}$  is defined as follows:

The individual pull-up and pull-down resistors ( $R_{ONPu}$  and  $R_{ONPd}$ ) are defined as follows:

$$R_{ONPu} = \frac{V_{DDQ} - V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ONPd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPu} \text{ is off}$$

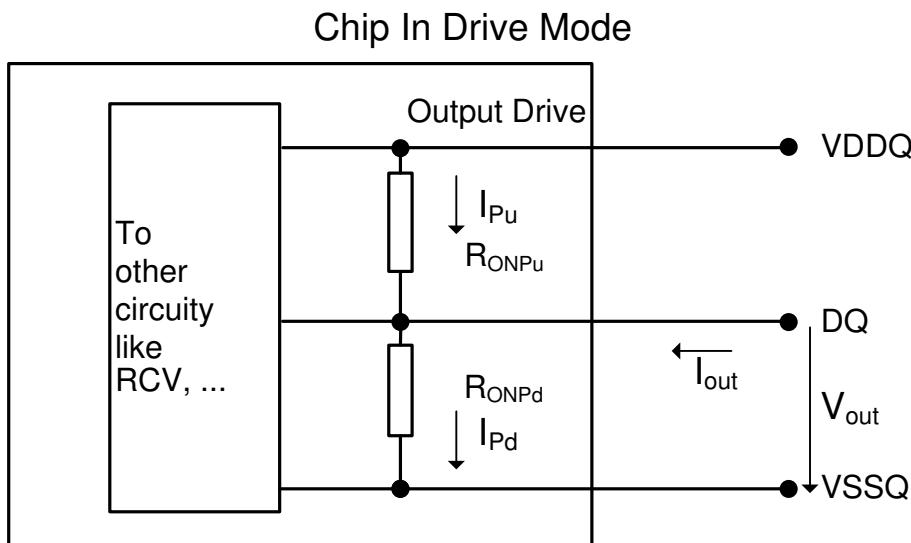


Figure 202. Output driver

**Table 99. Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration**

R <sub>ON_NOM</sub>	Resistor	V <sub>out</sub>	Min.	Nom.	Max.	Unit	Note
34Ω	R <sub>ON34Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.73	1	1.1	RZQ/7	1,2,3
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.83	1	1.1	RZQ/7	1,2,3
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.83	1	1.25	RZQ/7	1,2,3
	R <sub>ON34Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DDQ</sub>	0.9	1	1.25	RZQ/7	1,2,3
		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	0.9	1	1.1	RZQ/7	1,2,3
		V <sub>OHdc</sub> = 1.1 x V <sub>DDQ</sub>	0.8	1	1.1	RZQ/7	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	10	-	23	%	1-4,6,7
Mismatch DQ-DQ within byte variation pull-up, MMPudd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	-	-	10	%	1-5
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		V <sub>OMdc</sub> = 0.8 x V <sub>DDQ</sub>	-	-	10	%	1-4,6,7

Note 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

Note 2. The tolerance limits are specified under the condition that V<sub>DDQ</sub> = V<sub>DD</sub> and that V<sub>SSQ</sub> = V<sub>SS</sub>.

Note 3. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 x V<sub>DDQ</sub>. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 x V<sub>DDQ</sub> and 1.1 x V<sub>DDQ</sub>.

Note 4. DQ-to-DQ mismatch within byte variation for a given component including DQS and DQS# (characterized).

Note 5. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure R<sub>ONPu</sub> and R<sub>ONPd</sub> both at 0.8 x V<sub>DDQ</sub> separately; R<sub>ON\_NOM</sub> is the nominal R<sub>ON</sub> value.

$$MMPuPd = \frac{R_{ONPu} - R_{ONPd}}{R_{TTNOM}} \times 100$$

Note 6. R<sub>ON</sub> variance range ratio to R<sub>ON</sub> Nominal value in a given component, including DQS and DQS#.

$$MMPudd = \frac{R_{ONPuMax} - R_{ONPdMin}}{R_{TTNOM}} \times 100$$

$$MMPddd = \frac{R_{ONPdMax} - R_{ONPdMin}}{R_{TTNOM}} \times 100$$

Note 7. This parameter of x16 device is specified for Upper byte and Lower byte.

## ALERT# output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance  $R_{ON}$  is defined as follows:

$$R_{ONPd} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ONPu} \text{ is off}$$

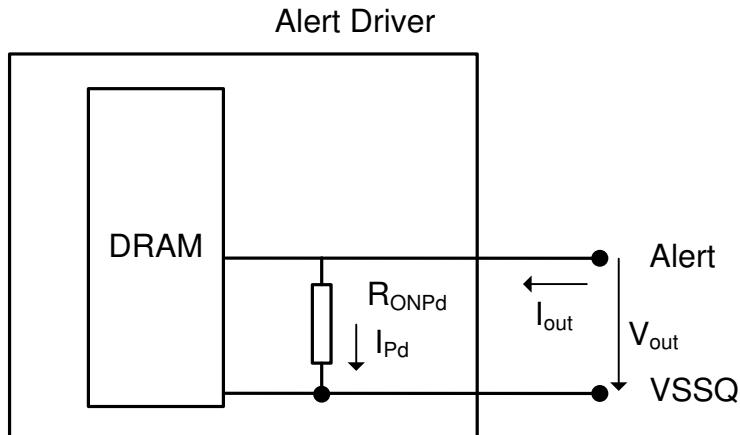


Figure 203. ALERT# output Drive Characteristic

Table 100. ALERT Driver Voltage

Resistor	Vout	Min.	Max.	Unit	Note
$R_{ONPd}$	$V_{OLdc} = 0.1 \times V_{DDQ}$	0.3	1.2	$34\Omega$	1
	$V_{OMdc} = 0.8 \times V_{DDQ}$	0.4	1.2	$34\Omega$	1
	$V_{OHdc} = 1.1 \times V_{DDQ}$	0.4	1.4	$34\Omega$	1

Note 1.  $V_{DDQ}$  voltage is at  $V_{DDQ}$  DC.

## Output Driver Characteristic of Connectivity Test ( CT ) Mode

Following Output driver impedance  $R_{ON}$  will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors ( $R_{ONPu\_CT}$  and  $R_{ONPd\_CT}$ ) are defined as follows:

$$R_{ONPu\_CT} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$

$$R_{ONPd\_CT} = \frac{V_{out}}{|I_{out}|}$$

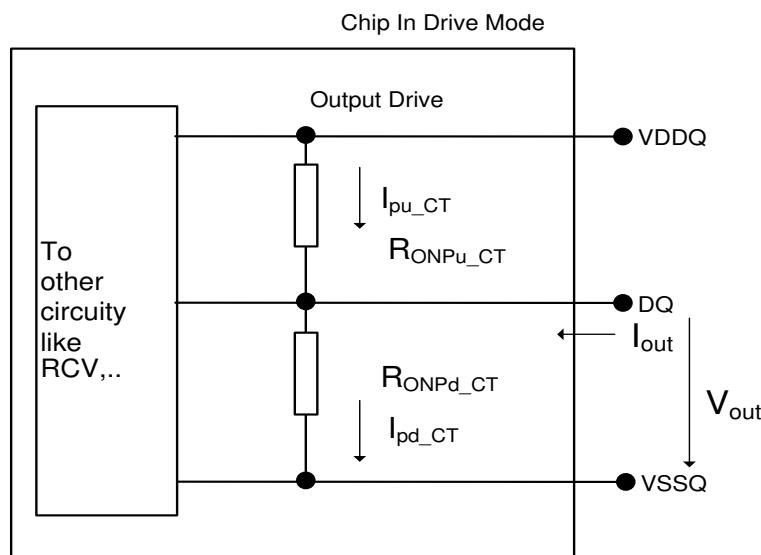


Figure 204. Output Driver Characteristic of Connectivity Test

Table 101. Output Driver Electrical Characteristics during Connectivity Test Mode

$R_{ON\_NOM}$	Resistor	$V_{out}$	Max.	Unit	Note
34Ω	$R_{ONPd\_CT}$	$V_{OBdc} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$V_{OLdc} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$V_{OMdc} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$V_{OHdc} = 1.1 \times V_{DDQ}$	2.5	34Ω	1
	$R_{ONPu\_CT}$	$V_{OBdc} = 0.2 \times V_{DDQ}$	1.9	34Ω	1
		$V_{OLdc} = 0.5 \times V_{DDQ}$	2.0	34Ω	1
		$V_{OMdc} = 0.8 \times V_{DDQ}$	2.2	34Ω	1
		$V_{OHdc} = 1.1 \times V_{DDQ}$	2.5	34Ω	1

Note 1. Assumes  $R_{ZQ} = 240\Omega$ ; ZQ calibration not required

**Single-ended AC & DC Output Levels****Table 102. Single-ended AC & DC output levels**

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

Note 1. The swing of  $\pm 0.15 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$ .

**Differential AC & DC Output Levels****Table 103. Differential AC & DC output levels**

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

Note 1. The swing of  $\pm 0.3 \times V_{DDQ}$  is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of  $50\Omega$  to  $V_{TT} = V_{DDQ}$  at each of the differential outputs.

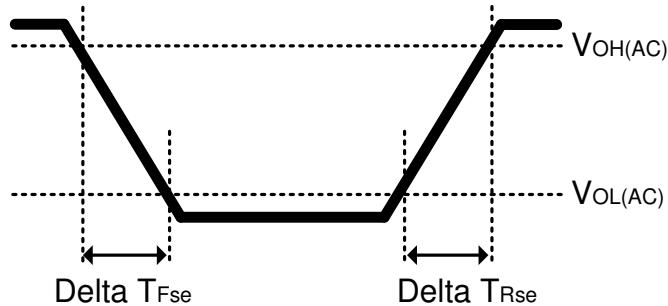
## Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single ended signals.

**Table 104. Single-ended output slew rate definition**

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta T_{Rse}$
Single ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta T_{Fse}$

Note 1. Output slew rate is verified by design and characterization, and may not be subject to production test.



**Figure 205. Single-ended Output Slew Rate Definition**

**Table 105. Single-ended output slew rate**

Symbol	Parameter	DDR4-3200		Unit
		Min.	Max.	
SRQse	Single ended output slew rate	4	9	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For  $R_{ON} = R_{ZQ}/7$  setting

Note 1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

- **Case 1** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

- **Case 2** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

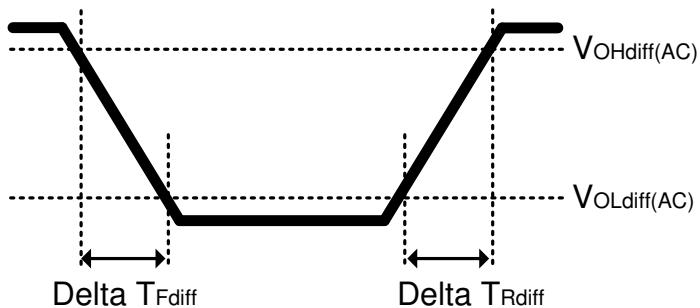
## Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OLdiff(AC)}$  and  $V_{OHdiff(AC)}$  for differential signals.

**Table 106. Differential output slew rate definition**

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta T_{Rdiff}$
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta T_{Fdiff}$

Note 1. Output slew rate is verified by design and characterization, and may not be subject to production test.



**Figure 206. Differential Output Slew Rate Definition**

**Table 107. Differential output slew rate**

Symbol	Parameter	DDR4-3200		Unit
		Min.	Max.	
SRQdiff	Differential output slew rate	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

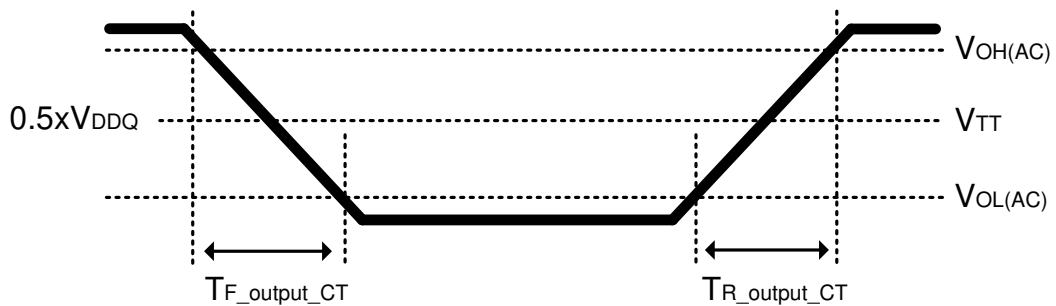
## Single-ended AC and DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

**Table 108. Single-ended AC & DC output levels of Connectivity Test Mode**

Symbol	Parameter	DDR4-3200	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$	V	1

Note 1. The effective test load is  $50\Omega$  terminated by  $V_{TT} = 0.5 \times V_{DDQ}$ .



**Figure 207. Output Slew Rate Definition of Connectivity Test Mode**

**Table 109. Single-ended output slew rate of Connectivity Test Mode**

Symbol	Parameter	DDR4-3200		Unit
		Min.	Max.	
$T_{F\_output\_CT}$	Output signal Falling time	-	10	ns/V
$T_{R\_output\_CT}$	Output signal Rising time	-	10	ns/V

## Test Load for Connectivity Test Mode Timing

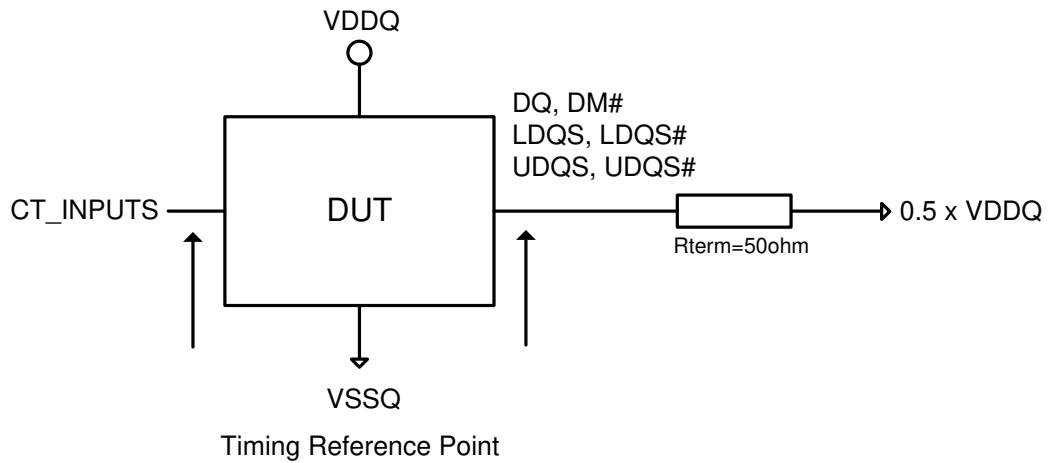


Figure 208. Connectivity Test Mode Timing Reference Load

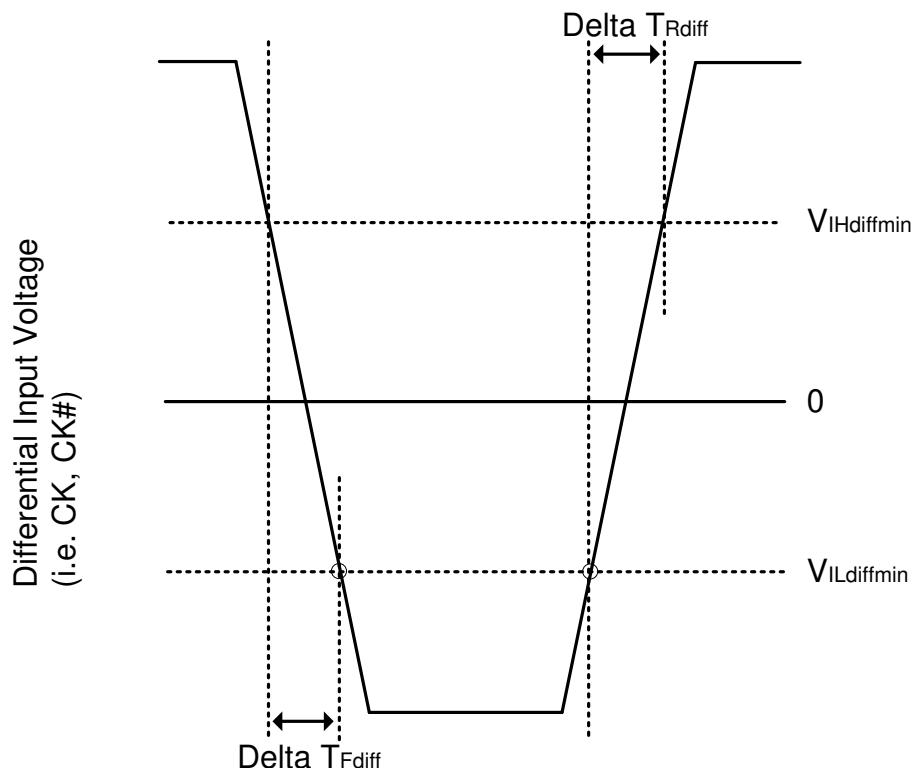
## Slew Rate Definitions

### Slew Rate Definitions for Differential Input Signals (CK)

**Table 110. Differential Input Slew Rate Definition**

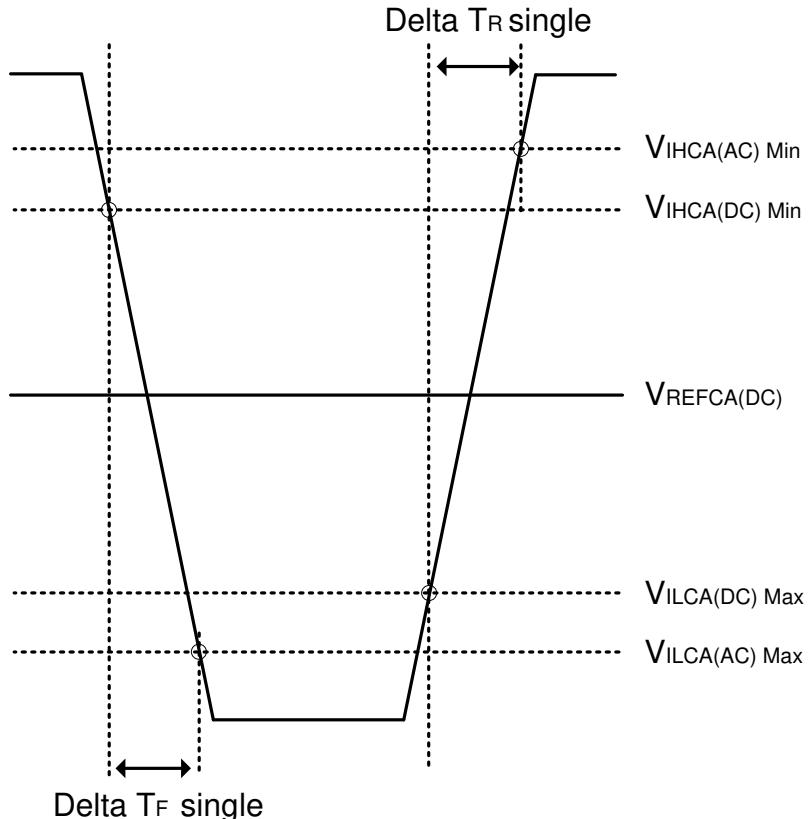
Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK - CK#)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta T_{Rdiff}$
Differential input slew rate for falling edge (CK - CK#)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta T_{Fdiff}$

Note 1. The differential signal (i.e., CK - CK#) must be linear between these thresholds.



**Figure 209. Differential Input Slew Rate Definition for CK, CK#**

## Slew Rate Definition for Single-ended Input Signals ( CMD/ADD )



NOTE 1. Single-ended input slew rate for rising edge = {  $V_{IHCA(AC)Min} - V_{ILCA(DC)Max}$  } /  $\Delta T_R$  single.

NOTE 2. Single-ended input slew rate for falling edge = {  $V_{IHCA(DC)Min} - V_{ILCA(AC)Max}$  } /  $\Delta T_F$  single.

NOTE 3. Single-ended signal rising edge from  $V_{ILCA(DC)Max}$  to  $V_{IHCA(DC)Min}$  must be monotonic slope.

NOTE 4. Single-ended signal falling edge from  $V_{IHCA(DC)Min}$  to  $V_{ILCA(DC)Max}$  must be monotonic slope.

**Figure 210. Single-ended Input Slew Rate definition for CMD and ADD**

## Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK, CK#) must meet the requirements in Table. The differential input cross point voltage  $V_{IX}$  is measured from the actual cross point of true and complement signals to the midlevel between  $V_{DD}$  and  $V_{SS}$ .

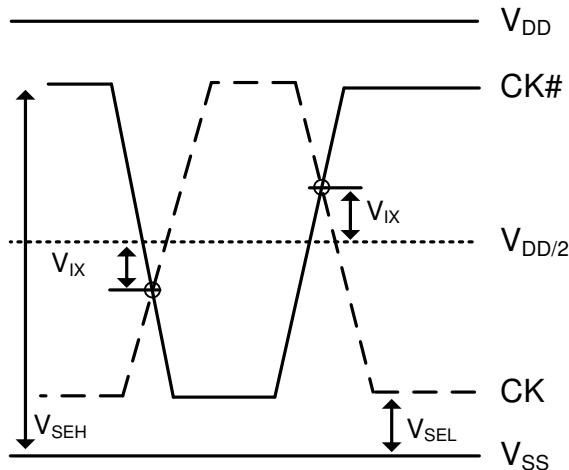


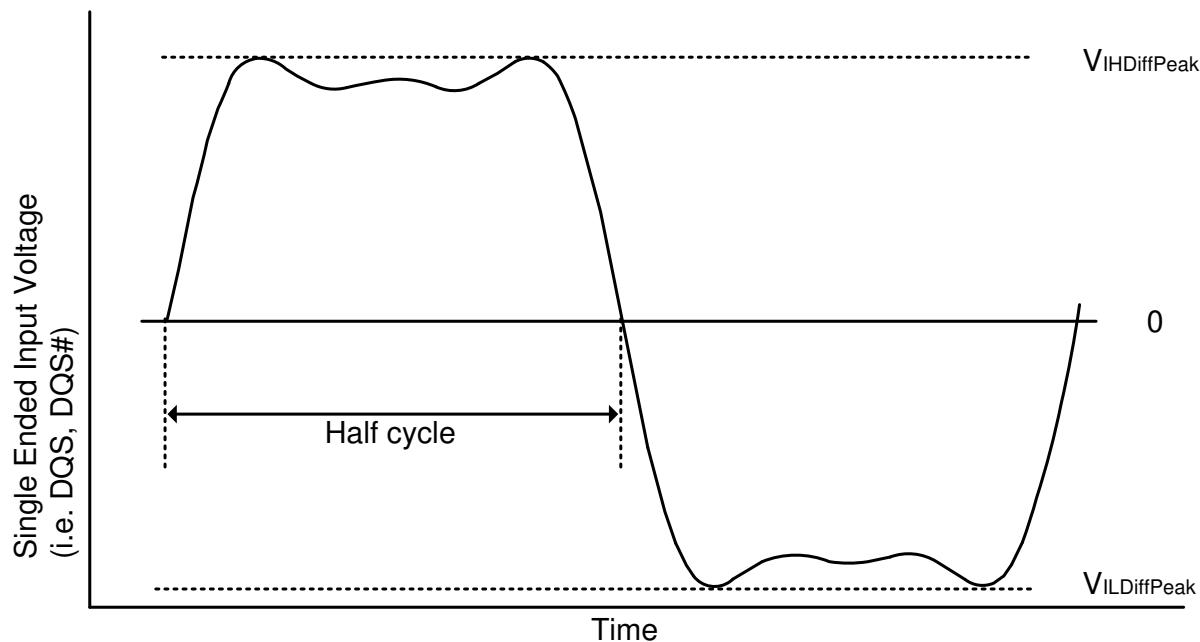
Figure 211. Vix Definition (CK)

Table 111. Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-3200			
		Min.		Max.	
-	Area of $V_{SEH}$ , $V_{SEL}$	$V_{SEL} < V_{DD}/2 - 145 \text{ mV}$	$V_{DD}/2 - 145 \text{ mV} \leq V_{SEL} \leq V_{DD}/2 - 90 \text{ mV}$	$V_{DD}/2 + 90 \text{ mV} \leq V_{SEH} \leq V_{DD}/2 + 145 \text{ mV}$	$V_{SEL} > V_{DD}/2 + 145 \text{ mV}$
$V_{IX}$ (CK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, CK#	-110 mV	$-(V_{DD}/2 - V_{SEL}) + 30 \text{ mV}$	$(V_{SEH} - V_{DD}/2) - 30 \text{ mV}$	110 mV

## AC and DC Logic Input Levels for DQS Signals

### Differential signal definition



**Figure 212. Definition of differential DQS Signal AC-swing Level**

### Differential swing requirements for DQS (DQS – DQS#)

**Table 112. Differential AC and DC Input Levels for DQS**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$V_{IHDiffPeak}$	$V_{IH,DIFF,Peak}$ Voltage	140	-	mV	1,2
$V_{ILDiffPeak}$	$V_{IL,DIFF,Peak}$ Voltage	-	-140	mV	1,2

Note 1. Used to define a differential signal slew-rate.

Note 2. These values are not defined; however, the differential signals DQS – DQS#, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

## Peak voltage calculation method

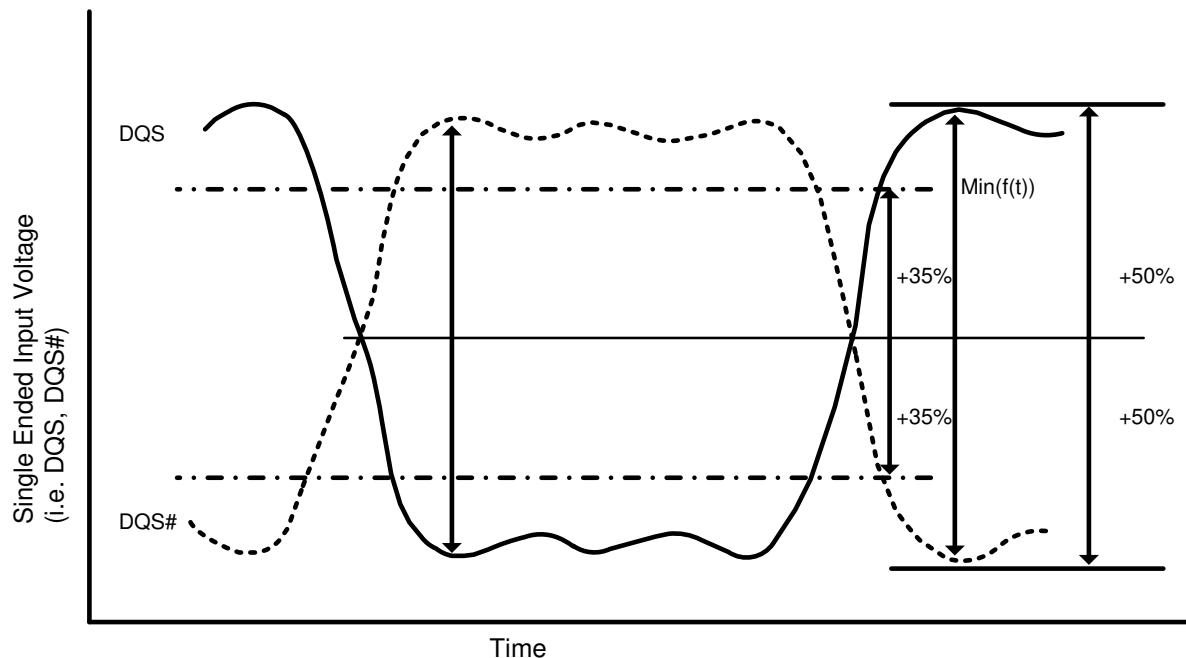
The peak voltage of Differential DQS signals are calculated in a following equation.

$$VIH.DIFF.\text{Peak Voltage} = \text{Max}(f(t))$$

$$VIL.DIFF.\text{Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VDQS}_t - \text{VDQS}_c$$

The  $\text{Max}(f(t))$  or  $\text{Min}(f(t))$  used to determine the midpoint which to reference the  $\pm 35\%$  window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.



**Figure 213. Definition of differential DQS Peak Voltage and range of exempt no monotonic signaling**

## Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS, DQS#) must meet the requirements in the table below. The differential input cross point voltage  $V_{IX\_DQS}$  ( $V_{IX\_DQS\_FR}$  and  $V_{IX\_DQS\_RF}$ ) is measured from the actual cross point of DQS, DQS# relative to the  $V_{DQSmid}$  of the DQS and DQS# signals.

$V_{DQSmid}$  is the midpoint of the minimum levels achieved by the transitioning DQS and DQS# signals, and noted by  $V_{DQS\_trans}$ .  $V_{DQS\_trans}$  is the difference between the lowest horizontal tangent above  $V_{DQSmid}$  of the transitioning DQS signals and the highest horizontal tangent below  $V_{DQSmid}$  of the transitioning DQS signals. A no monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within  $\pm 35\%$  of the midpoint of either  $V_{IH,DIFF,Peak}$  Voltage (DQS rising) or  $V_{IL,DIFF,Peak}$  Voltage (DQS# rising), as shown in the figure below.

A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in the figure below), and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in the figure below) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in the figure below) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in the figure below) is not a valid horizontal tangent.

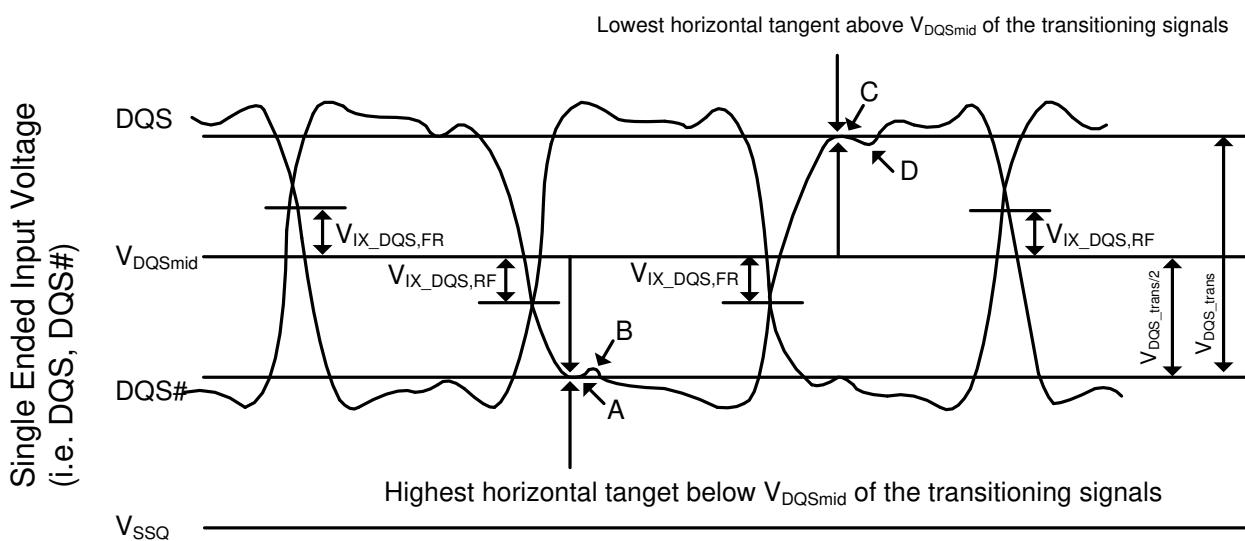


Figure 214. Vix Definition (DQS)

Table 113. Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$V_{IX\_DQS\_Ratio}$	DQS and DQS# crossing relative to the midpoint of the DQS and DQS# signal swings	-	25	%	1,2
$V_{DQSmid\_to\_V_{cent}}$	$V_{DQSmid}$ offset relative to $V_{cent\_DQ}$ (midpoint)	-	$\min(V_{IHdiff}, 50)$	mV	3-5

Note 1.  $V_{IX\_DQS\_Ratio}$  is DQS VIX crossing ( $V_{IX\_DQS\_FR}$  or  $V_{IX\_DQS\_RF}$ ) divided by  $V_{DQS\_trans}$ .  $V_{DQS\_trans}$  is the difference between the lowest horizontal tangent above  $V_{DQSmid}$  of the transitioning DQS signals and the highest horizontal tangent below  $V_{DQSmid}$  of the transitioning DQS signals.

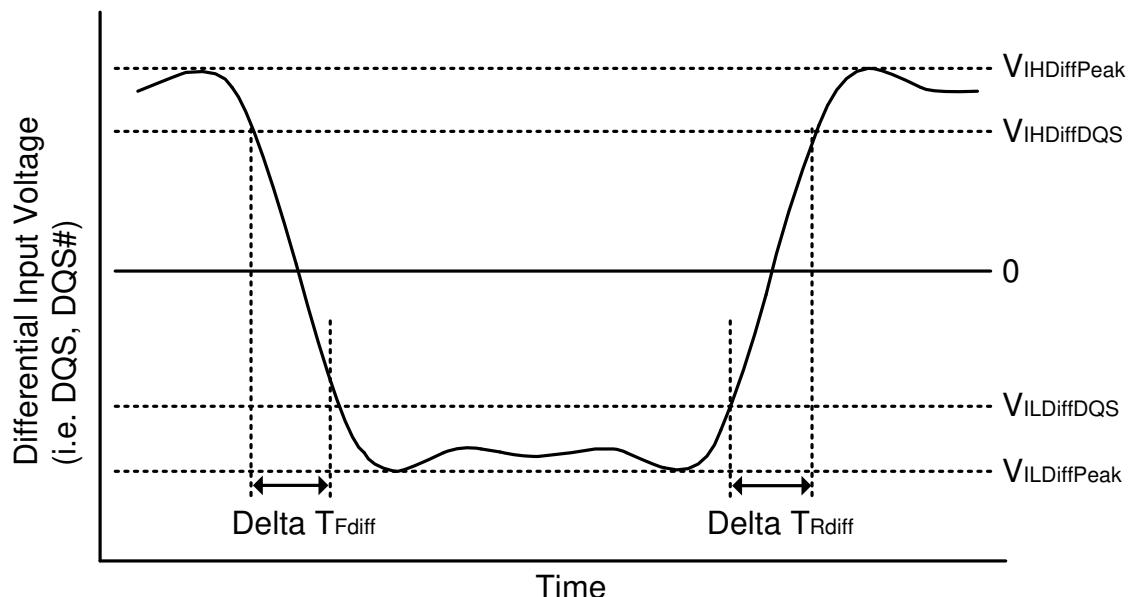
Note 2.  $V_{DQSmid}$  will be similar to the  $V_{REFDQ}$  internal setting value obtained during  $V_{REF}$  Training if the DQS and DQs drivers and paths are matched.

Note 3. The maximum limit shall not exceed the smaller of  $V_{IHdiff}$  minimum limit or 50mV.

Note 4.  $V_{IX}$  measurements are only applicable for transitioning DQS and DQS# signals when toggling data, preamble and high-z states are not applicable conditions.

Note 5. The parameter  $V_{DQSmid}$  is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

## Differential Input Slew Rate Definition



NOTE 1. Differential signal rising edge from  $V_{ILDiff\_DQS}$  to  $V_{IHDiff\_DQS}$  must be monotonic slope.  
 NOTE 2. Differential signal falling edge from  $V_{IHDiff\_DQS}$  to  $V_{ILDiff\_DQS}$  must be monotonic slope.

**Figure 215. Differential Input Slew Rate Definition for DQS, DQS#**

**Table 114. Differential Input Slew Rate Definition for DQS, DQS#**

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS - DQS#)	$V_{ILDiff\_DQS}$	$V_{IHDiff\_DQS}$	$ V_{ILDiff\_DQS} - V_{IHDiff\_DQS}  / \Delta T_{Rdif}$
Differential input slew rate for falling edge (DQS - DQS#)	$V_{IHDiff\_DQS}$	$V_{ILDiff\_DQS}$	$ V_{ILDiff\_DQS} - V_{IHDiff\_DQS}  / \Delta T_{Fdif}$

**Table 115. Differential Input Level for DQS, DQS#**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
$V_{IHDiff\_DQS}$	Differential Input High	110	-	mV	
$V_{ILDiff\_DQS}$	Differential Input Low	-	-110	mV	

**Table 116. Differential Input Slew Rate for DQS, DQS#**

Symbol	Parameter	DDR4-3200		Unit	Note
		Min.	Max.		
SRIdif	Differential Input Slew Rate	2.5	18	V/ns	

## Electrical Characteristics and AC Timing

### Reference Load for AC Timing and Output Slew Rate

Reference Load for AC Timing and Output Slew Rate represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

$R_{ON}$  nominal of DQ, DQS and DQS# drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal =  $1.0 \times V_{DDQ}$ ,

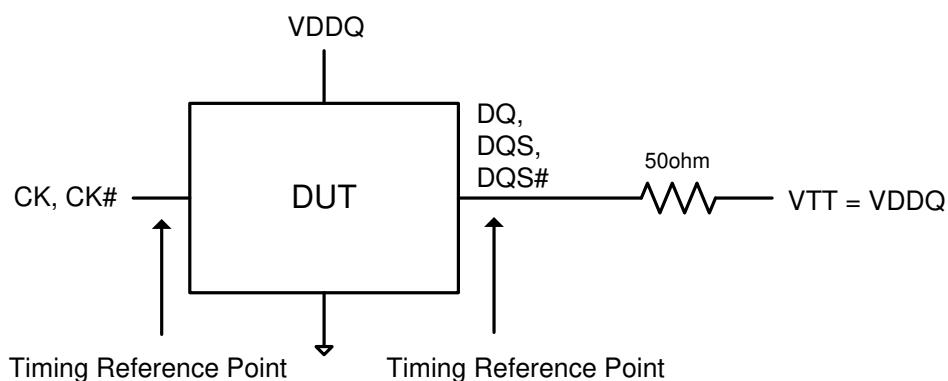
The minimum DC Low level of Output signal =  $\{ 34 / ( 34 + 50 ) \} \times V_{DDQ} = 0.4 \times V_{DDQ}$

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low =  $\{ ( 1 + 0.4 ) / 2 \} \times V_{DDQ} = 0.7 \times V_{DDQ}$

The actual reference level of Output signal might vary with driver  $R_{ON}$  and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



**Figure 216. Reference Load for AC Timing and Output Slew Rate**

## Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the device.

### Definitions for $t_{CK(\text{abs})}$ :

$t_{CK(\text{abs})}$  is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.  $t_{CK(\text{abs})}$  is not subject to production test.

### Definitions for $t_{CK(\text{avg})}$ and $nCK$ :

$t_{CK(\text{avg})}$  is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$t_{CK(\text{avg})} = \left( \sum_{j=1}^N t_{CK(\text{abs})_j} \right) / N$$

Where  $N=200$

### Definitions for $t_{CH(\text{avg})}$ and $t_{CL(\text{avg})}$ :

$t_{CH(\text{avg})}$  is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH(\text{avg})} = \left( \sum_{j=1}^N t_{CH_j} \right) / (N \times t_{CK(\text{avg})})$$

Where  $N=200$

$t_{CL(\text{avg})}$  is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL(\text{avg})} = \left( \sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK(\text{avg})})$$

Where  $N=200$

### Definitions for $t_{ERR(nper)}$ :

$t_{ERR}$  is defined as the cumulative error across  $n$  consecutive cycles of  $n \times t_{CK(\text{avg})}$ .  
 $t_{ERR}$  is not subject to production test.

## Command, Control, and Address Setup, Hold, and Derating

The total  $t_{IS}$  (setup time) and  $t_{IH}$  (hold time) required is calculated to account for slew rate variation by adding the data sheet  $t_{IS(base)}$  values, the  $V_{IH(AC)}/V_{IL(AC)}$  points, and  $t_{IH(base)}$  values, the  $V_{IH(DC)}/V_{IL(DC)}$  points; to the  $\Delta t_{IS}$  and  $\Delta t_{IH}$  derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example:  $t_{IS}$  (total setup time) =  $t_{IS(base)} + \Delta t_{IS}$ . For a valid transition, the input signal has to remain above/below  $V_{IH(AC)}/V_{IL(AC)}$  for the time defined by  $t_{VAC}$ .

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached  $V_{IH(AC)}/V_{IL(AC)}$  at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach  $V_{IH(AC)}/V_{IL(AC)}$ . For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup ( $t_{IS}$ ) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)max}$  and the first crossing of  $V_{IH(AC)min}$  that does not ring back below  $V_{IH(DC)min}$ . Setup ( $t_{IS}$ ) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)min}$  and the first crossing of  $V_{IL(AC)max}$  that does not ring back above  $V_{IL(DC)max}$ .

Hold ( $t_{IH}$ ) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of  $V_{IL(DC)max}$  and the first crossing of  $V_{IH(AC)min}$  that does not ring back below  $V_{IH(DC)min}$ . Hold ( $t_{IH}$ ) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of  $V_{IH(DC)min}$  and the first crossing of  $V_{IL(AC)min}$  that does not ring back above  $V_{IL(DC)max}$ .

**Table 117. Command, Address, Control Setup and Hold Values**

Symbol	Reference	DDR4-3200	Unit
$t_{IS(base)}$ , AC90)	$V_{IH(AC)}/V_{IL(AC)}$	40	ps
$t_{IH(base)}$ , DC65)	$V_{IH(DC)}/V_{IL(DC)}$	65	ps
$t_{IS}/t_{IH(VREF)}$	$V_{IH(DC)}/V_{IL(DC)}$	130	ps

Note 1. Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.

Note 2. Values listed are referenced only; applicable limits are defined elsewhere.

**Table 118. Command, Address, Control Input Voltage Values**

Symbol	Reference	DDR4-3200	Unit
$V_{IH,CA(AC)min}$	$V_{IH(AC)}/V_{IL(AC)}$	90	mV
$V_{IH,CA(DC)min}$	$V_{IH(DC)}/V_{IL(DC)}$	65	mV
$V_{IL,CA(DC)max}$	$V_{IH(DC)}/V_{IL(DC)}$	-65	mV
$V_{IL,CA(AC)max}$	$V_{IH(AC)}/V_{IL(AC)}$	90	mV

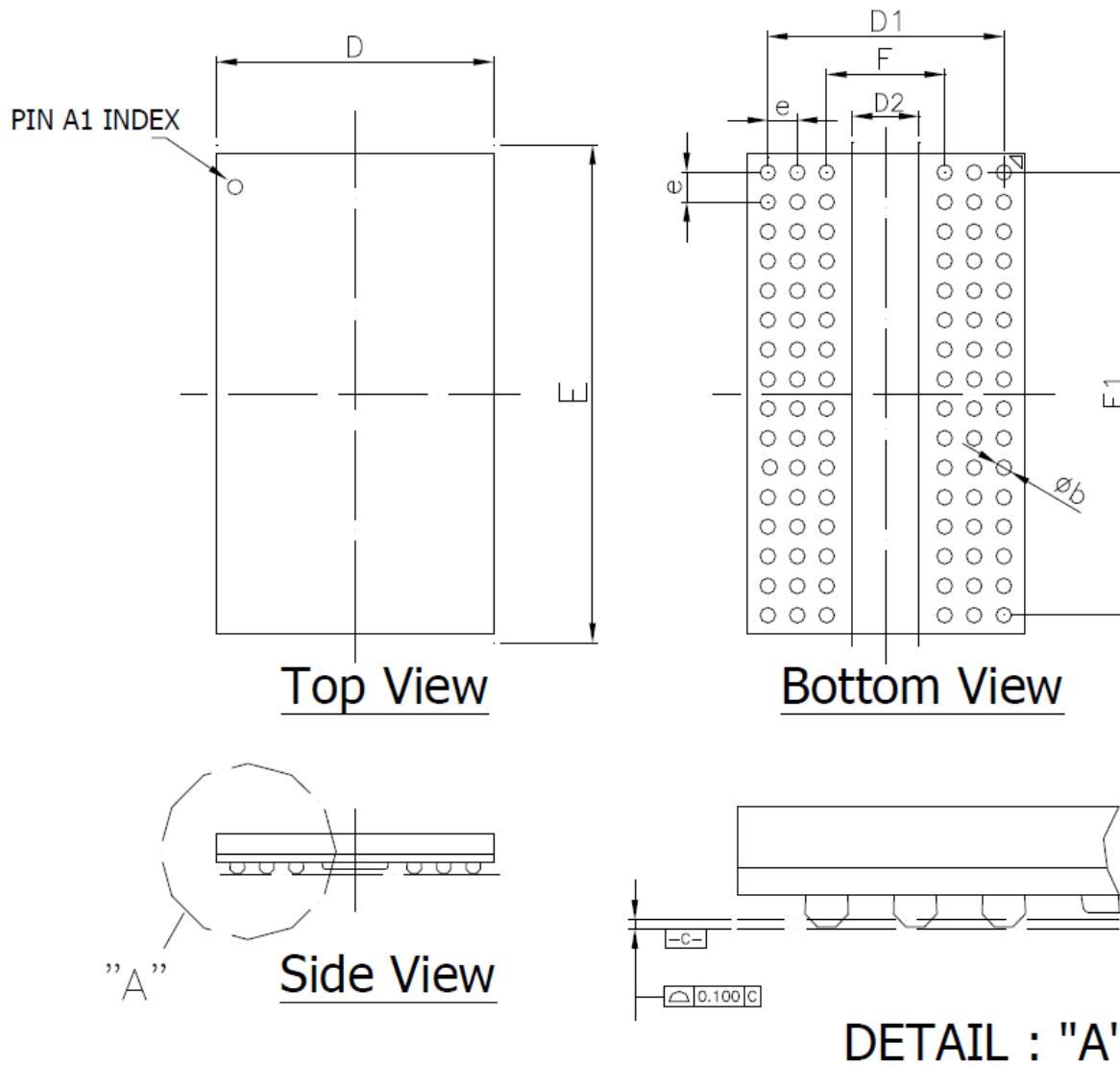
Note 1. Command, Address, Control input levels relative to  $V_{REFCA}$ .

Note 2. Values listed are referenced only; applicable limits are defined elsewhere.

**Table 119. Derating values DDR4-3200 tIS/tIH – AC/DC based**

		$\Delta t_{IS}, \Delta t_{IH}$ derating in [ps] AC/DC based -- $V_{IH(AC)}/V_{IL(AC)} = \pm 90mV$ , $V_{IH(DC)}/V_{IL(DC)} = \pm 65mV$ ; relative to $V_{REFCA}$															
		CK, CK# Differential Slew Rate															
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
CMD, ADDR, CNTL Input Slew rate V/ns	<b>7.0</b>	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	<b>6.0</b>	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	<b>5.0</b>	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	<b>4.0</b>	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	<b>3.0</b>	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	<b>2.0</b>	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	<b>1.5</b>	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	<b>1.0</b>	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	<b>0</b>	<b>0</b>	8	8	23	23
	<b>0.9</b>	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	<b>0.8</b>	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	<b>0.7</b>	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	<b>0.6</b>	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	<b>0.5</b>	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	<b>0.4</b>	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

## Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.013	0.015	0.017	0.33	0.38	0.43
A2	--	0.006	--	--	0.155	--
D	0.291	0.295	0.299	7.40	7.50	7.60
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.472	--	--	12.00	--
F	--	0.126	--	--	3.20	--
e	--	0.031	--	--	0.80	--
b	0.019	0.021	0.023	0.475	0.525	0.575
D2	--	0.071	--	--	1.8	--

Figure 217. 96-Ball FBGA Package 7.5x13x1.2mm(max)