

Embedded Multi-Media Card (e•MMC)

Flash Storage Specification e•MMC 5.1™ HS400

EM74J08HVAGA-H

Revision History

| Rev | Date | Comments |
|------------|-------------------|--|
| 1.00 | December 12, 2023 | Initial release. |
| 1.01 | May 02, 2024 | Updated CID Register (MID / OID / PNM) |

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1 Introduction

The e•MMC™ products follow the JEDEC e•MMC™ 5.1 standard. It is an ideal universal storage solution for many electronic devices, including smart phones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. E•MMC™ encloses the MLC NAND and e•MMC™ controller inside as one JEDEC standard package, providing a standard interface to the host. The e•MMC™ controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

1.1. Product Features

- **Packaged managed NAND flash memory with e•MMC™ 5.1 interface**
- **Backward compatible with all prior e•MMC™ specification revisions**
- **Operating Voltage Support:**
 - V_{CC} : (3.3V) 2.7V ~ 3.6V
 - V_{CCQ} : (1.8V) 1.7V ~ 1.95V / (3.3V) 2.7V ~ 3.6V
- **Temperature:**
 - Operating Temperature: TC = -25°C to +85°C
 - Storage without operation: -40°C to +85°C
- **Compliant with e•MMC™ 5.1 JEDEC Standard Number JESD84-B51**
- **Embedded Multi-Media storage in a single Multi-Chip package.**
- **Package: 153-ball 11.5 x 13.0 x 0.9mm FBGA package**

Table 1-1. Product Information

| Part Number | NAND Density | V_{CC} | V_{CCQ} | Package |
|----------------|--------------|----------|-----------|---------|
| EM74J08HVAGA-H | 16 GB | 3.3V | 1.8V/3.3V | FBGA |

1.2. eMMC™ Specific Feature

- **High-speed eMMC™ protocol**
- **Variable clock frequencies of 0-200MHz**
- **Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with an optional hardware reset**
- **Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits**
- **Bus modes:**
 - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
 - Dual data rate mode (DDR-104) : up to 104MB/s @ 52MHz
 - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
 - High speed, dual data rate mode (HS-400) : up to 400MB/s @ 200MHz
- **Supports alternate boot operation mode to provide a simple boot sequence method**
- **Supports SLEEP/AWAKE (CMD5)**
- **Host initiated explicit sleep mode for power saving**
- **Enhanced write protection with permanent and partial write protection options**
- **Multiple user data partition with enhanced attribute for increased reliability**
- **Error free memory access**
 - Cyclic Redundancy Code (CRC) for reliable command and data communication
 - Internal error correction code (ECC) for improved data storage integrity
 - Internal enhanced data management algorithm
 - Data protection for sudden power failure during program operations
- **Security**
 - Secure block erase commands
 - Enhanced write protection with permanent and partial protection options
- **Power off notification**
- **Field firmware update (FFU)**
- **Production state awareness**
- **Device health report**
- **Command queuing**
- **Enhanced strobe**
- **Cache flushing report**
- **Cache barrier**
- **Background operation control & High Priority Interrupt (HPI)**
- **RPMB throughput improvement**
- **Secure write protection**
- **Pre EOL information**
- **Optimal size**

2 Product Description

The eMMC™ products conform to the JEDEC eMMC™ 5.1 standard. These devices are an ideal universal storage solution for many commercial and industrial applications. In a single integrated packaged device, eMMC™ combines multi-level cell (MLC) NAND flash memory with an onboard eMMC™ controller, providing an industry standard interface to the host system. The integrated eMMC™ controller directly manages NAND flash media which relieves the host processor of these tasks, including flash media error control, wear-leveling, NAND flash management and performance optimization. Future revision to the JEDEC eMMC™ standard will always maintain backward compatibility. The industry standard interface to the host processor ensures compatibility across future NAND flash generations as well, easing product sustainment throughout the product life cycle.

2.1. Device Block Diagram

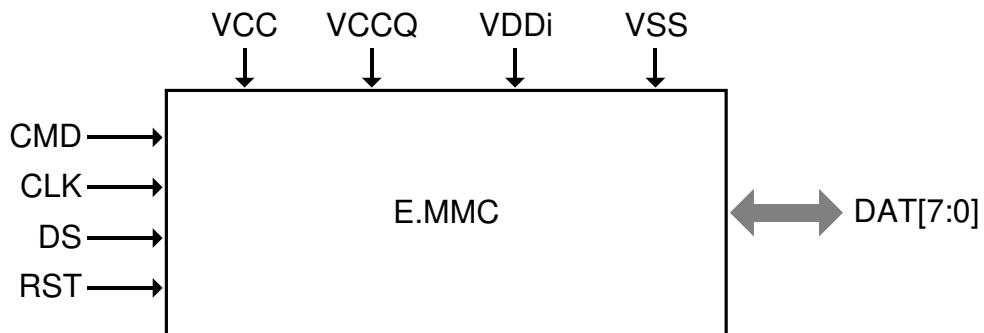


Figure 2-1. Block Diagram

2.2. Package Configuration

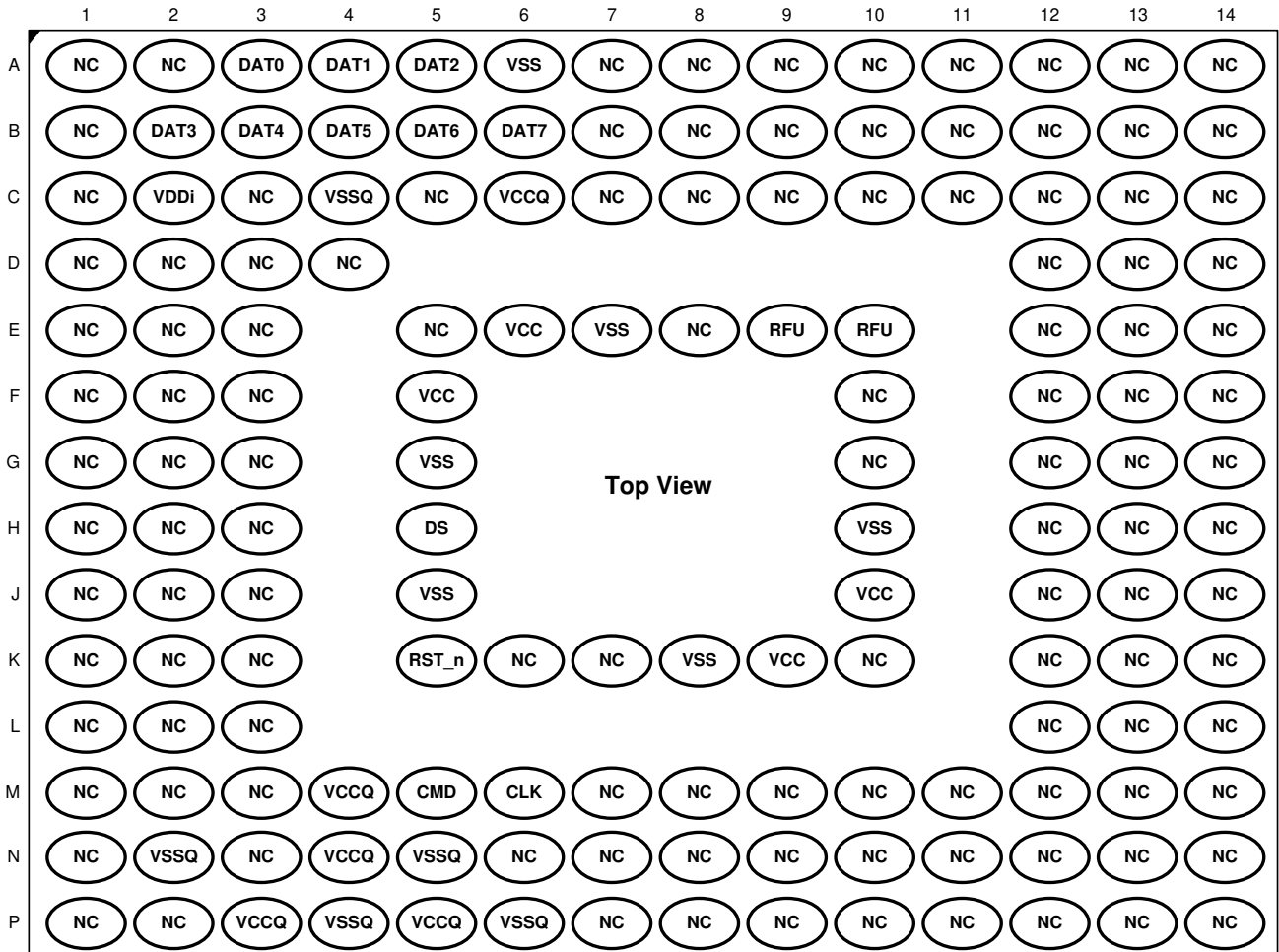


Figure 2-2. 153-FBGA Ball Assignment (Top View)

2.3. Ball Assignment

Table 2-1. Ball Descriptions

| Name | Type | Description |
|--|-----------|---|
| CLK | I | Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency. |
| DAT[7:0] | I/O/PP | Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the eMMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC™ host controller. The eMMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7. |
| CMD | I/O/PP/OD | Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC™ host controller to the eMMC™ device and responses are sent from the device to the host. |
| DS | O | This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge. |
| RST_n | I | Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected. |
| RFU | - | Reserved for future use: These pins are not internally connected. Leave floating |
| NC | - | Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design. |
| VDDi | - | Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor. |
| VCC | S | Supply voltage for core |
| VDDQ | S | Supply voltage for I/O |
| VSS | S | Supply ground for core |
| VSSQ | S | Supply ground for I/O |
| Note: I=Input; O=Output; P=Push-Pull; OD=Open Drain; NC=Not Connected(or logical high); S=Power Supply | | |

2.4. Device Performance

The following table provides sequential read and write speeds for all capacities. Performance numbers may vary under different operating conditions. Values are given in HS400 bus mode.

Table 2-2. Sequential Read / Write Performance

| Product | Typical value (MB/s) | | Dynamic booster value (MB/s) | |
|----------------|----------------------|------------------|------------------------------|------------------|
| | Read Sequential | Write Sequential | Read Sequential | Write Sequential |
| EM74J08HVAGA-H | 290 | 35 | 290 | 110 |

Note 1: Performance numbers might be subject to changes without notice.

2.5. Power Consumption

The device current consumption for various device configurations is defined in the power level field of the EXT_CSD register. The table below summarizes the power consumption values.

Table 2-3. Device Power Consumption

| Product | Read(mA) | | Write(mA) | | Standby(mA) | |
|----------------|------------|-----------|------------|-----------|-------------|-----------|
| | VCCQ(1.8V) | VCC(3.3V) | VCCQ(1.8V) | VCC(3.3V) | VCCQ(1.8V) | VCC(3.3V) |
| EM74J08HVAGA-H | 158 | 68 | 93 | 61 | 0.052 | 0.026 |

Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, VCC= 3.3V±5%, VCCQ=1.8V±5%

Note 2: Standby current is measured at VCC=3.3V±5%, 8-bit bus width without clock frequency.

Note 3: Current numbers might be subject to changes without notice.

2.6. Device and Partition Capacity

The device NAND flash capacity is divided across two boot partitions (4096 KB each), a Replay Protected Memory Block (RPMB) partition (4096 KB), and the main user storage area. Four additional general purpose storage partitions can be created from the user partition. These partitions can be factory preconfigured or configured in-field by following the procedure outlined in the JEDEC e•MMC™ specification JESD84-B51. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and mapping tables. Additionally, several NAND blocks are held in reserve to boost performance and extend the life of the e•MMC™ device. The following table determines the specific capacity of each partition. This information is reported in the device EXT_CSD registers. The contents of this register are also listed in the Appendix.

Table 2-4. Partition Capacity

| User density | Boot partition 1 | Boot partition 2 | RPMB |
|-------------------|------------------|------------------|---------|
| 15675162624 Bytes | 4096 KB | 4096 KB | 4096 KB |

2.7. e•MMC™ Bus Modes

The device supports all bus modes defined in the JEDEC e•MMC™5.1 specification. The following table summarizes these patterns.

Table 2-5. e•MMC™ Bus Modes

| Mode | Data Rate | IO Voltage | Bus Width | CLK Frequency | Maximum Data Bus Throughput |
|----------------|-----------|-------------|-----------|---------------|-----------------------------|
| Legacy MMC | Single | 3.3V / 1.8V | 1, 4, 8 | 0 – 26 MHz | 26 MB/s |
| High Speed SDR | Single | 3.3V / 1.8V | 4, 8 | 0 – 52 MHz | 52 MB/s |
| High Speed DDR | Dual | 3.3V / 1.8V | 4, 8 | 0 – 52 MHz | 104 MB/s |
| HS200 | Single | 1.8V | 4, 8 | 0 – 200 MHz | 200 MB/s |
| HS400 | Dual | 1.8V | 8 | 0 – 200 MHz | 400 MB/s |

3 Device Register

3.1. Card Identification Register (CID)

The Card Identification (CID) register is a 128-bit register that contains device identification information used during the eMMC™ protocol device identification phase. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

3.2. Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC™. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

3.3. Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Table 3-1. eMMC™ Register

| Name | Width (Bytes) | Description | Implementation |
|---------|---------------|---|----------------|
| CID | 16 | Device Identification number, an individual number for identification. | Mandatory |
| RCA | 2 | Relative Device Address is the Device system address, dynamically assigned by the host during initialization. | Mandatory |
| DSR | 2 | Driver Stage Register, to configure the Device's output drivers. | Optional |
| CSD | 16 | Device Specific Data, information about the Device operation conditions. | Mandatory |
| OCR | 4 | Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device. | Mandatory |
| EXT_CSD | 512 | Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0 | Mandatory |

Register Settings:

Applied Products: EM74J08HVAGA-H (ST74JH)

OCR Register Setting:

| OCR Register Definitions OCR bit | VDD voltage window | High Voltage Multi-Media Card | Dual voltage Multi-Media Card and eMMC™ |
|---|--|--------------------------------------|---|
| [6:0] | Reserved | 00 00000b | 00 00000b |
| [7] | 1.70 - 1.95V | 0b | 1b |
| [14:8] | 2.0-2.6V | 000 0000b | 000 0000b |
| [23:15] | 2.7-3.6V | 1 1111 1111b | 1 1111 1111b |
| [28:24] | Reserved | 0 0000b | 0 0000b |
| [30:29] | Access Mode | 00b (byte mode) 10b (sector mode) | 00b (byte mode) 10b (sector mode) |
| [31] | (Device power up status bit (busy)) ¹ | | |
| Note1 : This bit is set to LOW if the Device has not finished the power up routine. | | | |

CID Register Setting:

| CID Fields Name | Field | Width | CID slice | Value |
|-----------------------|-------|-------|-----------|------------------------|
| Manufacturer ID | MID | 8 | [127:120] | D5h |
| Reserved | | 6 | [119:114] | 0h |
| Device/BGA | CBX | 2 | [113:112] | 1h |
| OEM/Application ID | OID | 8 | [111:104] | 40h |
| Product name | PNM | 48 | [103:56] | (535437344A48h) ST74JH |
| Product revision | PRV | 8 | [55:48] | 01h |
| Product serial number | PSN | 32 | [47:16] | Random by Production |
| Manufacturing date | MDT | 8 | [15:8] | month, year |
| CRC7 checksum | CRC | 7 | [7:1] | - (Note 1) |
| not used, always "1" | - | 1 | [0] | 1h |

Note1. The description are same as eMMC™ JEDEC standard.

CSD Register Setting:

| Name | Field | Width | CSD-slice | Value |
|--|--------------------|-------|-----------|-------|
| CSD structure | CSD_STRUCTURE | 2 | [127:126] | 3h |
| System specification version | SPEC_VERS | 4 | [125:122] | 4h |
| Reserved | - | 2 | [121:120] | 0h |
| Data read access-time 1 | TAAC | 8 | [119:112] | 4Fh |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC | 8 | [111:104] | 1h |
| Max. bus clock frequency | TRAN_SPEED | 8 | [103:96] | 32h |
| Device command classes | CCC | 12 | [95:84] | 8F5h |
| Max. read data block length | READ_BL_LEN | 4 | [83:80] | 9h |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | [79:79] | 0h |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | [78:78] | 0h |
| Read block misalignment | READ_BLK_MISALIGN | 1 | [77:77] | 0h |
| DSR implemented | DSR_IMP | 1 | [76:76] | 0h |
| Reserved | - | 2 | [75:74] | 0h |
| Device size | C_SIZE | 12 | [73:62] | FFFh |
| Max. read current @ VDD min | VDD_R_CURR_MIN | 3 | [61:59] | 7h |
| Max. read current @ VDD max | VDD_R_CURR_MAX | 3 | [58:56] | 7h |
| Max. write current @ VDD min | VDD_W_CURR_MIN | 3 | [55:53] | 7h |
| Max. write current @ VDD max | VDD_W_CURR_MAX | 3 | [52:50] | 7h |
| Device size multiplier | C_SIZE_MULT | 3 | [49:47] | 7h |
| Erase group size | ERASE_GRP_SIZE | 5 | [46:42] | 1Fh |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | [41:37] | 1Fh |
| Write protect group size | WP_GRP_SIZE | 5 | [36:32] | 0Fh |
| Write protect group enable | WP_GRP_ENABLE | 1 | [31:31] | 1h |
| Manufacturer default ECC | DEFAULT_ECC | 2 | [30:29] | 0h |
| Write speed factor | R2W_FACTOR | 3 | [28:26] | 2h |
| Max. write data block length | WRITE_BL_LEN | 4 | [25:22] | 9h |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | [21:21] | 0h |
| Reserved | - | 4 | [20:17] | 0h |
| Content protection application | CONTENT_PROT_APP | 1 | [16:16] | 0h |
| File format group | FILE_FORMAT_GRP | 1 | [15:15] | 0h |
| Copy flag (OTP) | COPY | 1 | [14:14] | 0h |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | [13:13] | 0h |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | [12:12] | 0h |
| File format | FILE_FORMAT | 2 | [11:10] | 0h |
| ECC code | ECC | 2 | [9:8] | 0h |
| CRC | CRC | 7 | [7:1] | 2Eh |
| Not used, always '1' | - | 1 | [0:0] | 1h |

Extended CSD Register:

| Name | Field | Size (Bytes) | CSD-slice | Value |
|---|---|--------------|-----------|-------|
| Properties Segment | | | | |
| Reserved (note1) | - | 6 | [511:506] | 0h |
| Extended Security Commands Error | EXT_SECURITY_ERR | 1 | [505] | 0h |
| Supported Command Sets | S_CMD_SET | 1 | [504] | 1h |
| HPI features | HPI_FEATURES | 1 | [503] | 1h |
| Background operations support | BKOPS_SUPPORT | 1 | [502] | 1h |
| Max packed read commands | MAX_PACKED_READS | 1 | [501] | 3Ch |
| Max packed write commands | MAX_PACKED_WRITES | 1 | [500] | 20h |
| Data Tag Support | DATA_TAG_SUPPORT | 1 | [499] | 1h |
| Tag Unit Size | TAG_UNIT_SIZE | 1 | [498] | 3h |
| Tag Resources Size | TAG_RES_SIZE | 1 | [497] | 0h |
| Context management capabilities | CONTEXT_CAPABILITIES | 1 | [496] | 5h |
| Large Unit size | LARGE_UNIT_SIZE_M1 | 1 | [495] | 17h |
| Extended partitions attribute support | EXT_SUPPORT | 1 | [494] | 3h |
| Supported modes | SUPPORTED_MODES | 1 | [493] | 01h |
| FFU features | FFU_FEATURES | 1 | [492] | 0h |
| Operation codes timeout | OPERATION_CODE_TIME_OUT | 1 | [491] | 0h |
| FFU Argument | FFU_ARG | 4 | [490:487] | 65535 |
| Barrier support | BARRIER_SUPPORT | 1 | [486:486] | 1h |
| Reserved (note1) | Reserved | 177 | [485:309] | - |
| CMD Queuing Support | CMQ_SUPPORT | 1 | [308:308] | 1h |
| CMD Queuing Depth | CMQ_DEPTH | 1 | [307:307] | 0Fh |
| Reserved (note1) | Reserved | 1 | [306:306] | - |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4 | [305:302] | 0h |
| Vendor proprietary health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 32 | [301:270] | 0h |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | [269] | 1h |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | [268] | 1h |
| Pre EOL information | PRE_EOL_INFO | 1 | [267] | 1h |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | [266] | 1h |
| Optimal write size | OPTIMAL_WRITE_SIZE | 1 | [265] | 8h |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | [264] | 1h |
| Device version | DEVICE_VERSION | 2 | [263:262] | 0h |
| Firmware version | FIRMWARE_VERSION | 8 | [261:254] | 1h* |
| Power class for 200MHz, DDR at VCC=3.6V | PWR_CL_DDR_200_360 | 1 | [253] | 0h |

| | | | | |
|---|------------------------------------|---|-----------|-----------|
| Cache size | CACHE_SIZE | 4 | [252:249] | 512 |
| Generic CMD6 timeout | GENERIC_CMD6_TIME | 1 | [248] | 19h |
| Power off notification(long) time out | POWER_OFF_LONG_TIME | 1 | [247] | 3h |
| Background operations status | BKOPS_STATUS | 1 | [246] | 0h |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | [245:242] | 0h |
| 1st initialization time after partitioning | INI_TIMEOUT_AP | 1 | [241] | 64h |
| Cache Flushing Policy | CACHE_FLUSH_POLICY | 1 | [240] | 1h |
| Power class for 52MHz, DDR at 3.6V | PWR_CL_DDR_52_360 | 1 | [239] | 0h |
| Power class for 52MHz, DDR at 1.95V | PWR_CL_DDR_52_195 | 1 | [238] | 0h |
| Power class for 200MHz at 3.6V | PWR_CL_200_360 | 1 | [237] | 0h |
| Power class for 200MHz, at 1.95V | PWR_CL_200_195 | 1 | [236] | 0h |
| Minimum Write Performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | [235] | 0h |
| Minimum Read Performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | [234] | 0h |
| Reserved (note1) | - | 1 | [233] | - |
| TRIM Multiplier | TRIM_MULT | 1 | [232] | 5h |
| Secure Feature support | SEC_FEATURE_SUPPORT | 1 | [231] | 55h |
| Secure Erase Multiplier | SEC_ERASE_MULT | 1 | [230] | 1Eh |
| Secure TRIM Multiplier | SEC_TRIM_MULT | 1 | [229] | 1Eh |
| Boot information | BOOT_INFO | 1 | [228] | 7h |
| Reserved (note1) | - | 1 | [227] | - |
| Boot partition size | BOOT_SIZE_MULT1 | 1 | [226] | 20h |
| Access size | ACC_SIZE | 1 | [225] | 7h |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | [224] | 1h |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | 1 | [223] | 5h |
| Reliable write sector count | REL_WR_SEC_C | 1 | [222] | 1h |
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | [221] | 10h |
| Sleep current (VCC) | S_C_VCC | 1 | [220] | 8h |
| Sleep current (VCCQ) | S_C_VCCQ | 1 | [219] | 8h |
| Production state awareness Timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | [218] | 14h |
| Sleep/awake timeout | S_A_TIMEOUT | 1 | [217] | 13h |
| Sleep Notification time out | SLEEP_NOTIFICATION_TIME | 1 | [216] | 0Fh |
| Sector Count | SEC_COUNT | 4 | [215:212] | 01D32800h |
| Secure Write Protect Information | SECURE_WP_INFO | 1 | [211] | 1h |
| Minimum Write Performance for 8bit at 52MHz | MIN_PERF_W_8_52 | 1 | [210] | 8h |

| | | | | |
|--|-----------------------|---|-------|-------------|
| Minimum Read Performance for 8bit at 52MHz | MIN_PERF_R_8_52 | 1 | [209] | 8h |
| Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52 | 1 | [208] | 8h |
| Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_R_8_26_4_52 | 1 | [207] | 8h |
| Minimum Write Performance for 4bit at 26MHz | MIN_PERF_W_4_26 | 1 | [206] | 8h |
| Minimum Read Performance for 4bit at 26MHz | MIN_PERF_R_4_26 | 1 | [205] | 8h |
| Reserved (note1) | – | 1 | [204] | – |
| Power class for 26MHz at 3.6V 1 R | PWR_CL_26_360 | 1 | [203] | 0h |
| Power class for 52MHz at 3.6V 1 R | PWR_CL_52_360 | 1 | [202] | 0h |
| Power class for 26MHz at 1.95V 1 R | PWR_CL_26_195 | 1 | [201] | 0h |
| Power class for 52MHz at 1.95V 1 R | PWR_CL_52_195 | 1 | [200] | 0h |
| Partition switching timing | PARTITION_SWITCH_TIME | 1 | [199] | 3h |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | [198] | 9h |
| I/O Driver Strength | DRIVER_STRENGTH | 1 | [197] | 1Fh |
| Device type | CARD_TYPE | 1 | [196] | 57h |
| Reserved (note1) | – | 1 | [195] | – |
| CSD structure version | CSD_STRUCTURE | 1 | [194] | 2h |
| Reserved (note1) | – | 1 | [193] | – |
| Extended CSD revision | EXT_CSD_REV | 1 | [192] | 08h |
| Modes Segment | | | | |
| Command set | CMD_SET | 1 | [191] | 0h |
| Reserved (note1) | – | 1 | [190] | – |
| Command set revision | CMD_SET_REV | 1 | [189] | 0h |
| Reserved (note1) | – | 1 | [188] | – |
| Power class | POWER_CLASS | 1 | [187] | 0h |
| Reserved (note1) | – | 1 | [186] | – |
| High-speed interface timing | HS_TIMING | 1 | [185] | 1h (note 3) |
| Strobe Support | STROBE_SUPPORT | 1 | [184] | 1h |
| Bus width mode | BUS_WIDTH | 1 | [183] | 2h (note 4) |
| Reserved (note1) | – | 1 | [182] | – |
| Erased memory content | ERASED_MEM_CONT | 1 | [181] | 0h |
| Reserved (note1) | – | 1 | [180] | – |
| Partition configuration | PARTITION_CONFIG | 1 | [179] | 0h |
| Boot config protection | BOOT_CONFIG_PROT | 1 | [178] | 0h |
| Boot bus Conditions | BOOT_BUS_CONDITIONS | 1 | [177] | 0h |
| Reserved (note1) | – | 1 | [176] | – |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | [175] | 0h |

| | | | | |
|--|-----------------------------|----|-----------|-----|
| Boot write protection status registers | BOOT_WP_STATUS | 1 | [174] | 0h |
| Boot area write protection register | BOOT_WP | 1 | [173] | 0h |
| Reserved (note1) | – | 1 | [172] | – |
| User area write protection register | USER_WP | 1 | [171] | 0h |
| Reserved (note1) | – | 1 | [170] | – |
| FW configuration | FW_CONFIG | 1 | [169] | 0h |
| RPMB Size | RPMB_SIZE_MULT | | [168] | 20h |
| Write reliability setting register | WR_REL_SET | | [167] | 1Fh |
| Write reliability parameter register | WR_REL_PARAM | 1 | [166] | 15h |
| Start Sanitize operation | SANITIZE_START | 1 | [165] | 0h |
| Manually start background operations | BKOPS_START | 1 | [164] | 0h |
| Enable background operations handshake | BKOPS_EN | 1 | [163] | 0h |
| H/W reset function | RST_n_FUNCTION | 1 | [162] | 0h |
| HPI management | HPI_MGMT | 1 | [161] | 0h |
| Partitioning Support | PARTITIONING_SUPPORT | 1 | [160] | 7h |
| Max Enhanced Area Size | MAX_ENH_SIZE_MULT | 3 | [159:157] | 934 |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | [156] | 0h |
| Partitioning Setting | PARTITION_SETTING_COMPLETED | 1 | [155] | 0h |
| General Purpose Partition Size | GP_SIZE_MULT 4 | 3 | [154:152] | 0h |
| General Purpose Partition Size | GP_SIZE_MULT3 | 3 | [151:149] | 0h |
| General Purpose Partition Size | GP_SIZE_MULT2 | 3 | [148:146] | 0h |
| General Purpose Partition Size | GP_SIZE_MULT1 | 3 | [145:143] | 0h |
| Enhanced User Data Area Size | ENH_SIZE_MULT | 3 | [142:140] | 0h |
| Enhanced User Data Start Address | ENH_START_ADDR | 4 | [139:136] | 0h |
| Reserved (note1) | – | 1 | [135] | – |
| Bad Block Management mode | SEC_BAD_BLK_MGMNT | 1 | [134] | 0h |
| Reserved (note1) | – | 1 | [133] | – |
| Package Case Temperature is controlled | TCASE_SUPPORT | 1 | [132] | 0h |
| Periodic Wake-up | PERIODIC_WAKEUP | 1 | [131] | 0h |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | [130] | 1h |
| Reserved (note1) | – | 2 | [129:128] | – |
| Vendor Specific Fields | VENDOR_SPECIFIC_FIELD | 64 | [127:64] | – |
| Native sector size | NATIVE_SECTOR_SIZE | 1 | [63] | 0h |
| Sector size emulation | USE_NATIVE_SECTOR | 1 | [62] | 0h |
| Sector size | DATA_SECTOR_SIZE | 1 | [61] | 0h |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | 1 | [60] | 0h |
| Class 6 commands control | CLASS_6_CTRL | 1 | [59] | 0h |

| | | | | |
|--|------------------------------------|----|---------|-----------|
| Number of addressed group to be Released | DYNCAP_NEEDED | 1 | [58] | 0h |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | [57:56] | 0h |
| Exception events status | EXCEPTION_EVENTS_STATUS | 2 | [55:54] | 0h |
| Extended Partitions Attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | [53:52] | 0h |
| Context configuration | CONTEXT_CONF | 15 | [51:37] | 0h |
| Packed command status | PACKED_COMMAND_STATUS | 1 | [36] | 0h |
| Packed command failure index | PACKED_FAILURE_INDEX | 1 | [35] | 0h |
| Power Off Notification | POWER_OFF_NOTIFICATION | 1 | [34] | 0h |
| Control to turn the Cache ON/OFF | CACHE_CTRL | 1 | [33] | 0h |
| Flushing of the cache | FLUSH_CACHE | 1 | [32] | 0h |
| Control to turn the Barrier ON/OFF | BARRIER_CTRL | 1 | [31] | 0h |
| Mode config | MODE_CONFIG | 1 | [30:30] | 0h |
| Mode operation codes | MODE_OPERATION_CODES | 1 | [29:29] | 0h |
| Reserved (note1) | Reserved | 2 | [28:27] | - |
| FFU status | FFU_STATUS | 1 | [26:26] | 0h |
| Per loading data size | PRE_LOADING_DATA_SIZE | 4 | [25:22] | 0h |
| Max pre loading data size | MAX_PRE_LOADING_DATA_SIZE | 4 | [21:18] | 00E8CE00h |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1 | [17:17] | 01h |
| Secure removal type | SECURE_REMOVAL_TYPE | 1 | [16:16] | 39h |
| Command Queue Mode enable | CMQ_MODE_EN | 1 | [15:15] | 0h |
| Reserved (note1) | Reserved | 15 | [14:0] | - |

Note 1. Reserved bits should read as "0."

Note 2. Obsolete values should be don't care.

Note 3. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing. If the host sets value 2 the Device changes its timing to HS200 interface timing, If the host sets HS_TIMING[3:0] to 0x3, the device changes its timing to HS400 interface timing. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Note 4. It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.

Note 5. * Changed by Firmware release note.

4 Operating Temperature and Voltage Range

Table 4-1. Device Operating Temperature

| Parameter | Rating | Unit |
|-------------------------------|-----------|------|
| Operating temperature (Tcase) | -25 ~ +85 | °C |

Table 4-2. Device Operating Voltage

| Parameter | Symbol | Min | Nom | Max | Unit |
|--------------------------|-------------------|-----|-----|------|------|
| Supply voltage (NAND) | VCC | 2.7 | 3.3 | 3.6 | V |
| Supply voltage (I/O) | VCCQ ¹ | 2.7 | 3.3 | 3.6 | V |
| | | 1.7 | 1.8 | 1.95 | V |
| Supply power-up for 3.3V | tPRUH | | | 35 | ms |
| Supply power-up for 1.8V | tPRUL | | | 25 | ms |

Note 1.VCCQ (I/O) 3.3 volt range is not supported while operating in HS200 & HS400 modes.

5 Package Outline Information

Table 5-1. FBGA (11.5 x 13 x 0.9mm) Dimension Table

| Symbol | Dimension in inch | | | Dimension in mm | | |
|--------|-------------------|--------|-------|-----------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.030 | 0.032 | 0.035 | 0.75 | 0.825 | 0.900 |
| A1 | 0.007 | 0.009 | 0.011 | 0.175 | 0.225 | 0.275 |
| A2 | 0.021 | 0.024 | 0.026 | 0.54 | 0.60 | 0.66 |
| D | 0.449 | 0.453 | 0.457 | 11.40 | 11.50 | 11.60 |
| E | 0.508 | 0.512 | 0.516 | 12.90 | 13.00 | 13.10 |
| D1 | -- | 0.256 | -- | -- | 6.50 | -- |
| E1 | -- | 0.256 | -- | -- | 6.50 | -- |
| D2 | -- | 0.098 | -- | -- | 2.50 | -- |
| E2 | -- | 0.098 | -- | -- | 2.50 | -- |
| SD | -- | 0.0098 | -- | -- | 0.25 | -- |
| SE | -- | 0.0098 | -- | -- | 0.25 | -- |
| e | -- | 0.020 | -- | -- | 0.50 | -- |
| b | 0.010 | 0.012 | 0.014 | 0.25 | 0.30 | 0.35 |

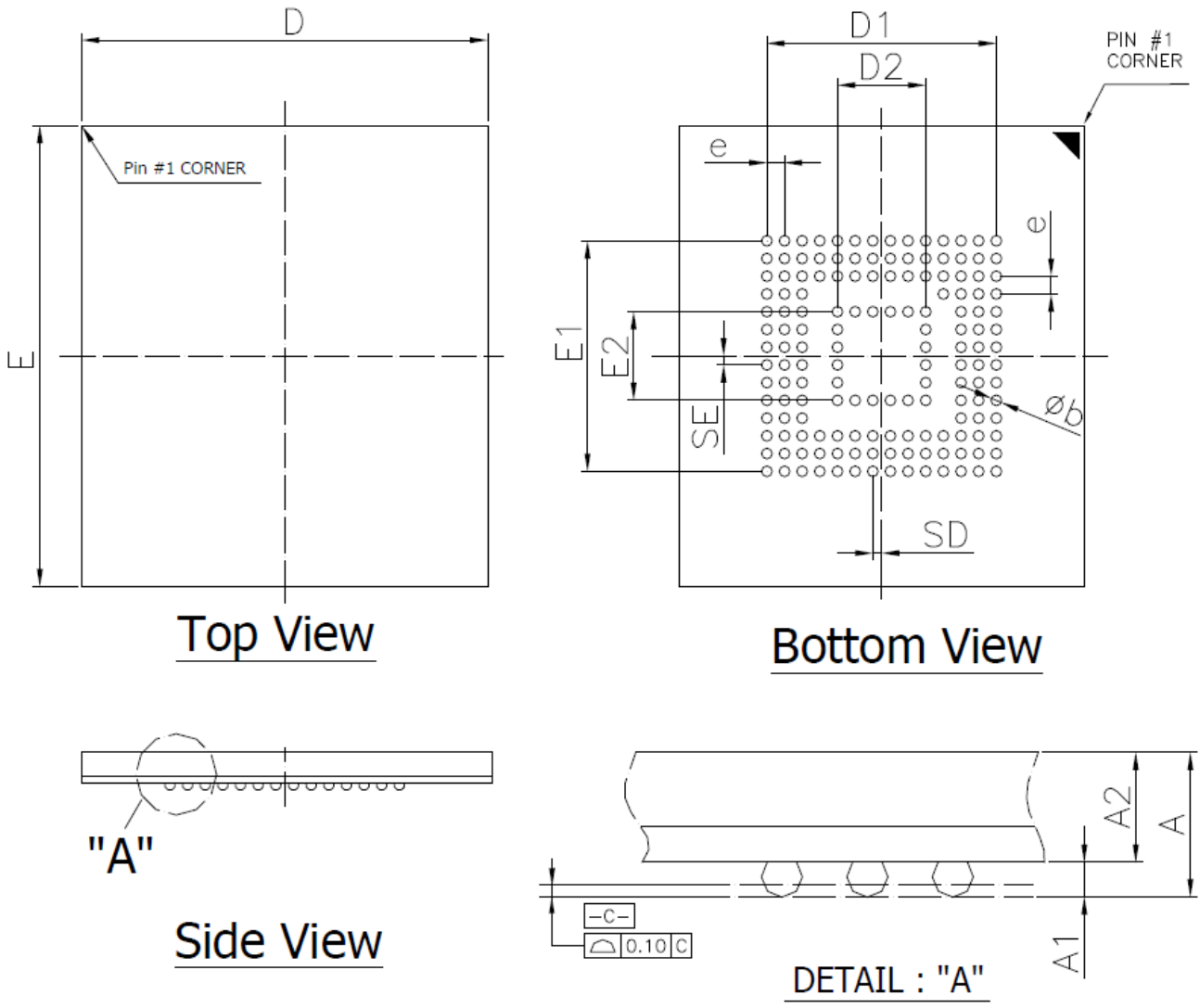


Figure 5-1. Package Outline Drawing Information for FBGA