Etron 鈺創科技
Etron Technology, Inc.

SPI NAND Flash Datasheet

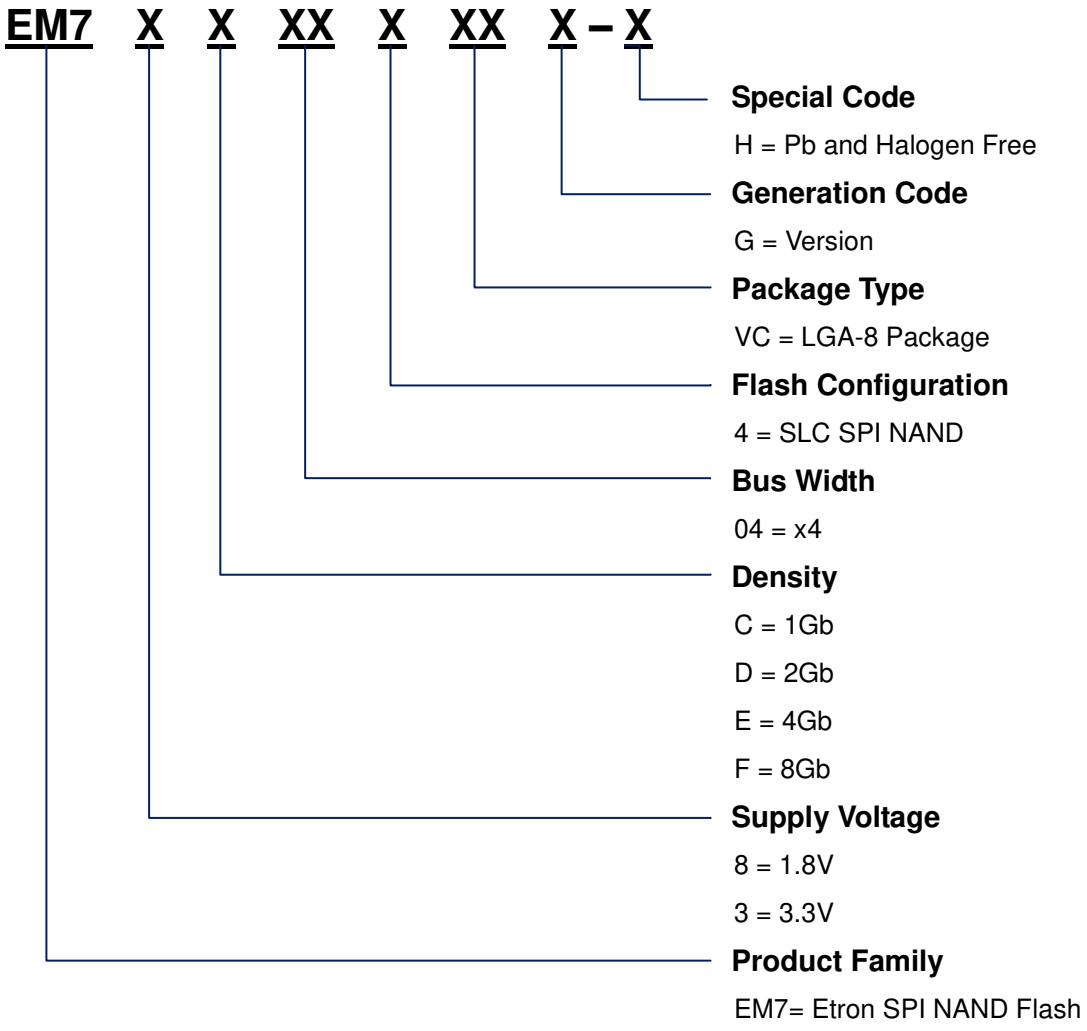
Serial Peripheral Interface (SPI)

Model
EM73C044VCG-H

Advance
Revision 1.2
June 6, 2024

SPI NAND Part Numbering Information

Etron SPI NAND Flash devices are categorized in the following diagram based on the features and densities



Etron Technology, Inc. reserves the right to change products or specification without notice.

Revision History

Rev	Date	Comments
1.0	September 13, 2023	Initial release
1.1	January 10, 2024	1. Removed Permanent Block Protection (PBP) 2. Updated DC/AC Characteristics 3. Added HOLD# Timing
1.2	June 6, 2024	1. Added the Table 1-4 ECC Protection and Spare Area

Contents

List of Figures

List of Tables

1 Introduction

1.1 Features

- **Flash Features**
  - Block Size: (Page size)×(64 page/block)
  - Page Size: 2048 + 64 bytes
  - SPI Capacity: 1Gb (1024 blocks)
- **SPI power supply voltage**
  - Full voltage range for 3.3V : 2.7 to 3.6V
- **Clock Frequency**
  - Up to 104MHz (for VCC 3.3V)
- **Standard, Dual and Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- **Performance (Typical)**
  - Page Program Time: 350us
  - Page Read Time (tR): 45us
  - Block Erase Time: 4ms
- **Reliability**
  - On-chip ECC correction Program
  - Blocks 0-9 are good at the time of shipment
  - 100,000 Program / Erase cycles (Typical)
  - 10 Year Data Retention (Typical)
- **Package (Pb Free and Halogen Free)**
  - 8-pin LGA-8 (8 x 6 x 0.8mm)
- **Temperature**
  - Operating Temperature: -40°C to +85°C
- **Security Features**
  - One Time Programmable (OTP) area
  - Hardware program/erase disabled during power transition

Table 1-1. Product Information

Part Number	Density	VCC	ECC	Page Size	Block	Device	Package
EM73C044VCG-H	1Gbits	3.3V	4bit	2048+64 Bytes	64 Pages	1024 Blocks	LGA-8

1.2 General Description

SPI (Serial Peripheral Interface) NAND Flash provides a low cost and low pin count solution to alternate SPI-NOR in high density non-volatile memory storage solution for embedded systems.

SPI NAND Flash is an SLC NAND Flash memory device based on the standard parallel NAND Flash. The serial electrical interface follows the industry-standard serial peripheral interface. The command sets is similar to the SPI-NOR command sets but with some modifications to handle NAND specific functions and new features are added to extend applications. The SPI NAND flash device has total 8 pin count, including six signal lines plus VCC and GND.

Each block of the serial NAND Flash device is subdivided into 64 programmable pages. Each page consists of a data storage region and a spare area. The data storage region is used to storage data user programmed and the spare area is typically used for memory management and error correction functions.

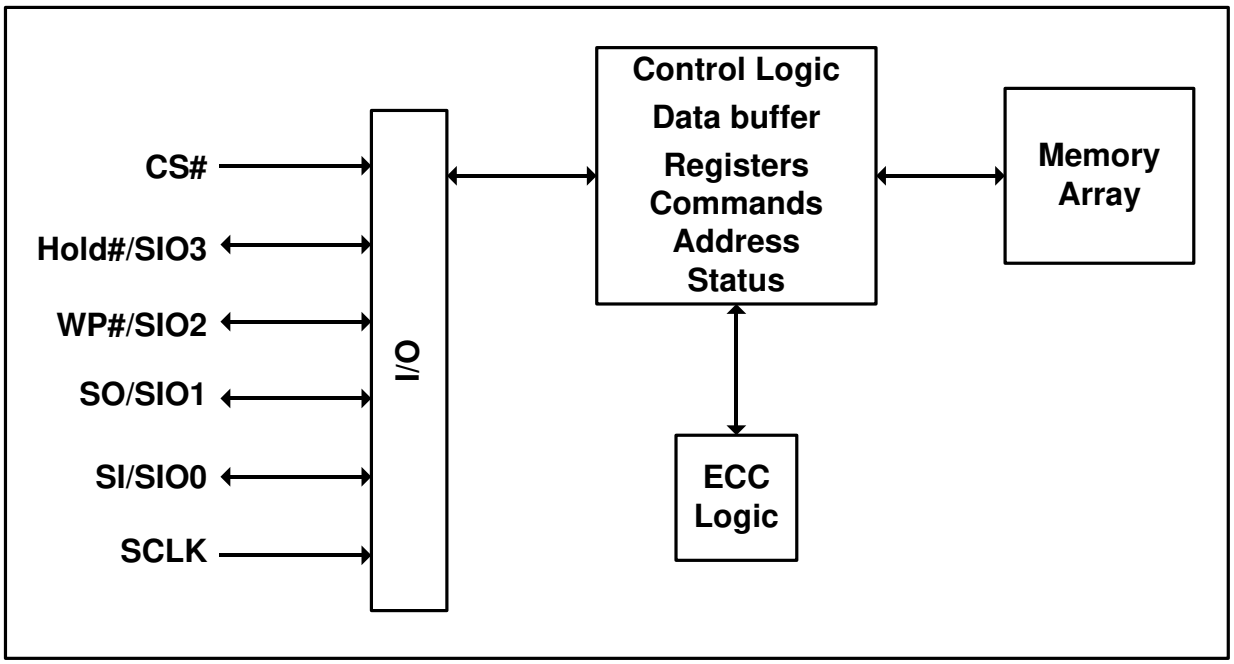


Figure 1-1. Functional Block Diagram

1.3 Memory Mapping Diagram

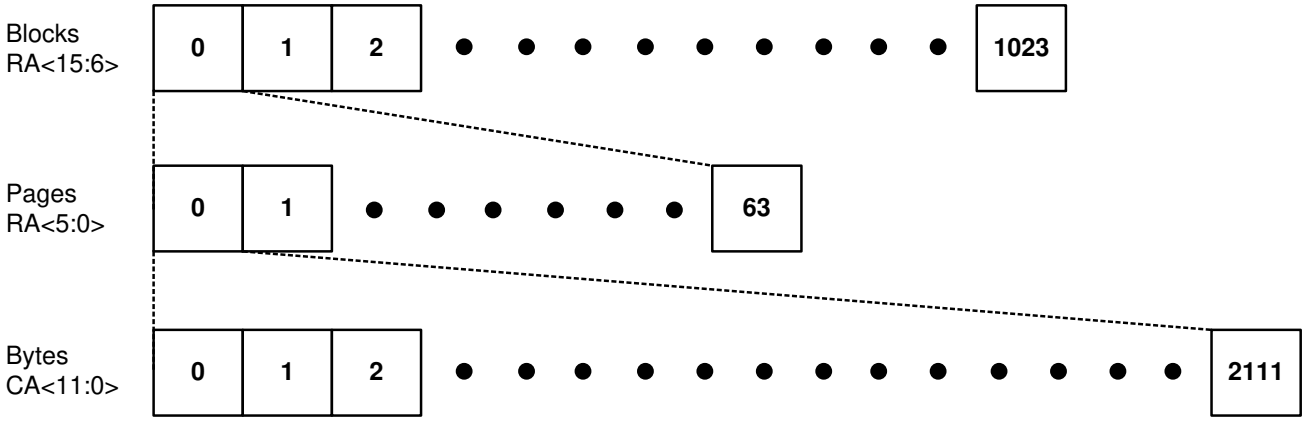


Figure 1-2. Memory Mapping Diagram

Notes:

1. RA: Row Address. The RA can to index and select the block.
   RA[5:0]: for Page Range 0~63.
   RA[15:6] : for 1G, have 0~1023 blocks range.

2. CA: Column Address. The CA[11:0] can only access 0~2111 bytes, include 2K(2048)bytes and 64Byte *OOB.
   *OOB : Each page of a NAND flash has an “out of band” (OOB) area to hold Error Correcting Code (ECC) and other metadata.

1.4 Pin Configuration

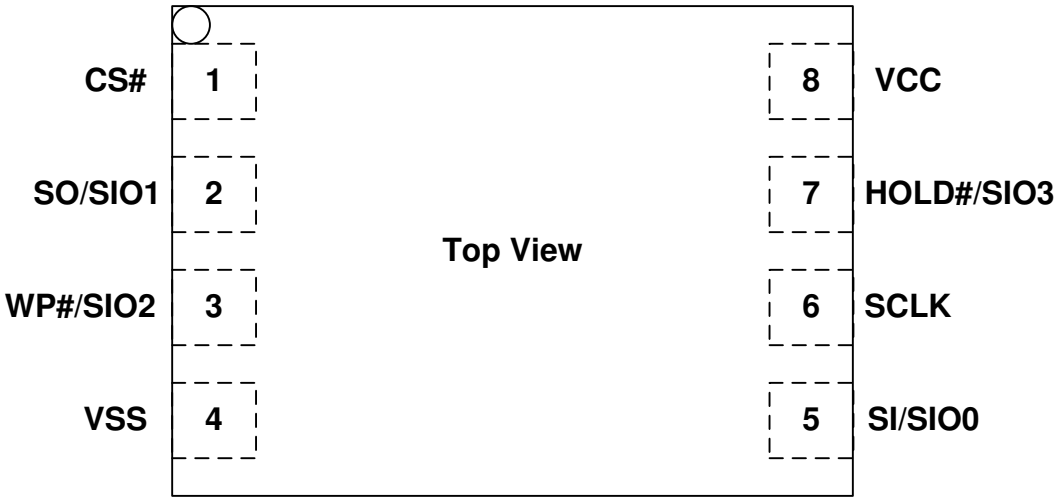


Figure 1-3. Pin Assignments

Table 1-2. Pin Descriptions

Pin Name	Type	Description
SCLK	Input	Serial Clock
SI/SIO0	I/O	Serial Data Input / Serial Data IO0
SO/SIO1	I/O	Serial Data Output / Serial Data IO1
WP#/SIO2	I/O	Write Protect / Serial Data IO2
Hold#/SIO3	I/O	Hold / Serial Data IO3
CS#	Input	Chip Select
VCC	Supply	Power Supply
VSS	Ground	Ground

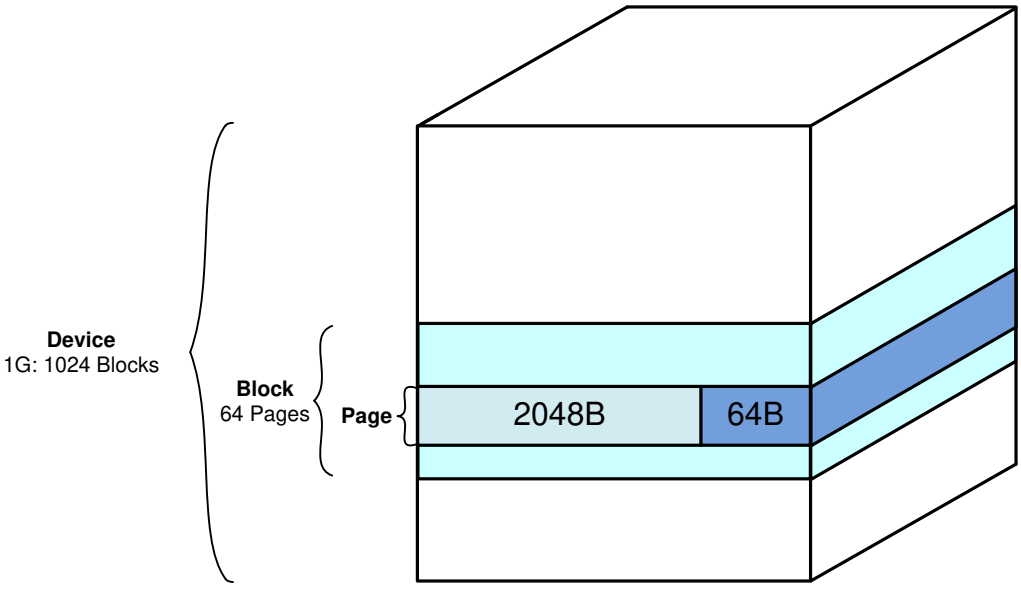
Note:

1. A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.

1.5 Array Organization

Table 1-3. Array Descriptions

Density	Number of Blocks	Number of Pages	Page Size	Device Size
1G	1024	64	2K+64B	128MB+4MB



1 page (program unit) = (2K+64) bytes
1 block (Erase unit) = (2K+64)*64 pages = (128K + 4K) bytes
1G device = (128K+4K)*1024 blocks = (128MB+4MB)

Figure 1-4. Array Organization

Table 1-4. ECC Protection and Spare Area

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main Area 01	Data storage region 01
200h	3FFh	Yes	Main Area 02	Data storage region 02
400h	5FFh	Yes	Main Area 03	Data storage region 03
600h	7FFh	Yes	Main Area 04	Data storage region 04
800h	80Fh	Yes	Spare Area 01	Meta data 01
810h	81Fh	Yes	Spare Area 02	Meta data 02
820h	82Fh	Yes	Spare Area 03	Meta data 03
830h	83Fh	Yes	Spare Area 04	Meta data 04

2 Device Operation

2.1 SPI Mode

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams shown in this data sheet are mode 0.

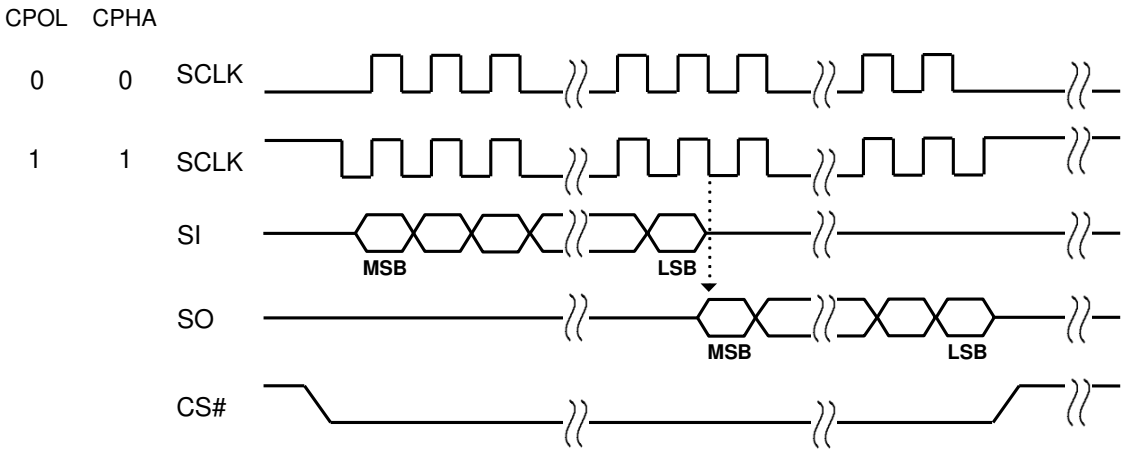


Figure 2-1. Timing Diagram of SPI Modes

Note:

1. SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
2. When CS# is 0, the device is placed in active mode. When CS# goes 1, the device is placed in inactive mode and SO is High-Z.

2.1.1 Standard SPI

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO).

2.1.2 Dual SPI

The device supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1.

2.1.3 Quad SPI

The device supports the x4 and Quad commands operation. These commands allow data to be transferred to or from the device at four times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1. The WP# and the HOLD# pins become SIO2 and SIO3.

2.2 Hold Mode

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of writing status register, programming or erasing in progress.

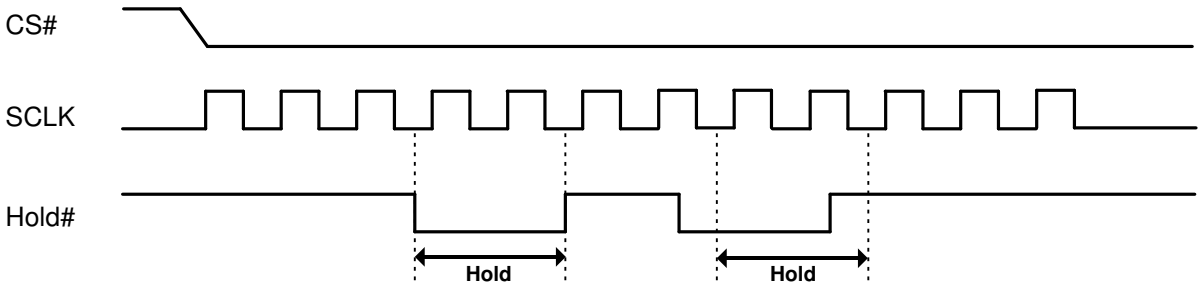


Figure 2-2. Hold Condition Diagram

Note:
Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

3 Commands Description

Table 3-1. SPI NAND Command Set

Command	Op Code	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Nth Byte
Write Disable	04H	-	-	-	-	-	-
Write Enable	06H	-	-	-	-	-	-
Block Erase (Block size)	D8H	A23-A16	A15-A8	A7-A0	-	-	-
Program Load	02H	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load x4 IO	32H	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Execute	10H	A23-A16	A15-A8	A7-A0	-	-	-
Page Read (to Cache)	13H	A23-A16	A15-A8	A7-A0	-	-	-
Read from Cache x1 IO	03H/0BH	A15-A8	A7-A0	Dummy	D7-D0	Next data	Wrap
Read from Cache x2 IO	3BH	A15-A8	A7-A0	Dummy	(D7-D0)x2	Next data	Wrap
Read from Cache x4 IO	6BH	A15-A8	A7-A0	Dummy	(D7-D0)x4	Next data	Wrap
Read from Cache Dual IO	BBH	A15-A0	Dummy(1)	(D7-D0)x2	Next data	Next data	Wrap
Read from Cache Quad IO	EBH	A15-A0	Dummy(1)	(D7-D0)x4	Next data	Next data	Wrap
Read ID	9FH	Dummy	MID	DID	Wrap	Wrap	Wrap
Reset	FFH	-	-	-	-	-	-
Get Feature	0FH	A7-A0	D7-D0	-	-	-	-
Set Feature	1FH	A7-A0	D7-D0	-	-	-	-

Note:

1. The number of dummy cycles is 8 cycles.

4 Write Operations

The WRITE ENABLE (WREN, 06H) command is for setting the Write Enable Latch (WEL) bit. The WRITE DISABLE (WRDI, 04H) command is for clearing the WEL bit.

As with any command that changes the memory contents, the WRITE ENABLE command must be executed at first in order to set the WEL bit to 1. For more information, please refer to the Page Read operation sequence, PAGE PROGRAM operation sequence, Internal Data Move operation sequence, BLOCK ERASE operation sequence and OTP operation sequence.

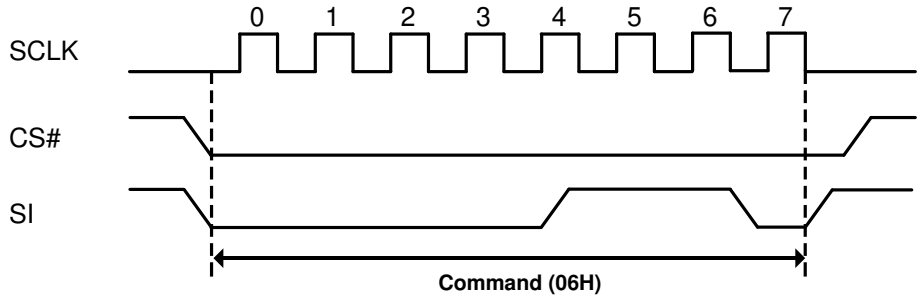


Figure 4-1. Write Enable (06H) Sequence Diagram

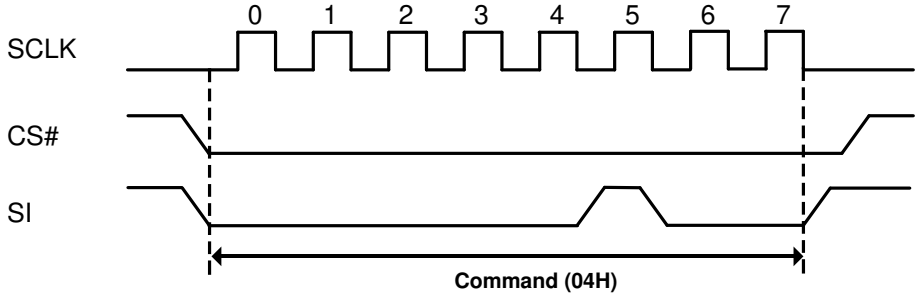


Figure 4-2. Write Disable (04H) Sequence Diagram

5 Feature Operations

The GET FEATURE (0FH) and SET FEATURE (1FH) commands are used to monitor the device status and alter the device behavior.

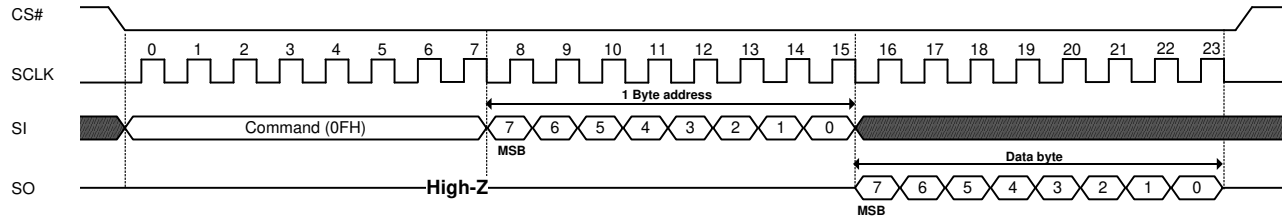
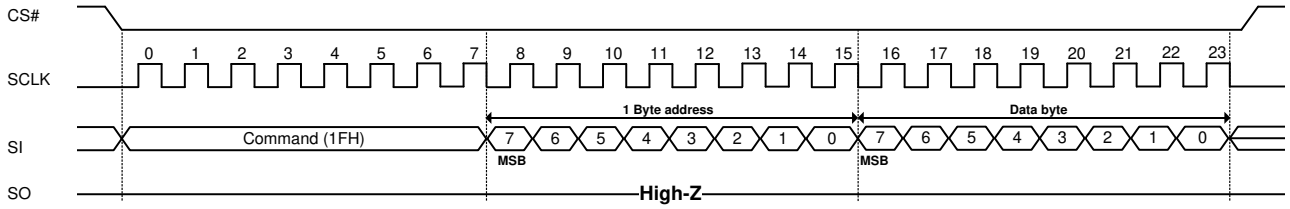


Figure 5-1. Get Feature (0FH) Sequence Diagram



The SET FEATURE command is valid only when WP# pin = 1.

Figure 5-2. Set Feature (1FH) Sequence Diagram

Table 5-1. Feature Register Table

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Protect	A0H	BRWD	BP3	BP2	BP1	BP0	INV	HWP_EN(1)	Reserved
Configuration	B0H	CFG2	CFG1	HWP_LD(1)	ECC_EN(3)	Reserved	Reserved	CFG0	Reserved
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Notes:

1. HWP_EN must be enabled first before block unlock region is set
2. HWP_LD when set to 1, this bit along with the register A0H [6:0] can only be cleared during POR
3. ECC_EN must be always set to 1

6 Read Operations

6.1 Read ID (9FH)

The Read ID command is used to identify the SPI NAND. The Read ID command outputs the manufacturer ID with address byte 00H and outputs the device ID when address byte is 01H.

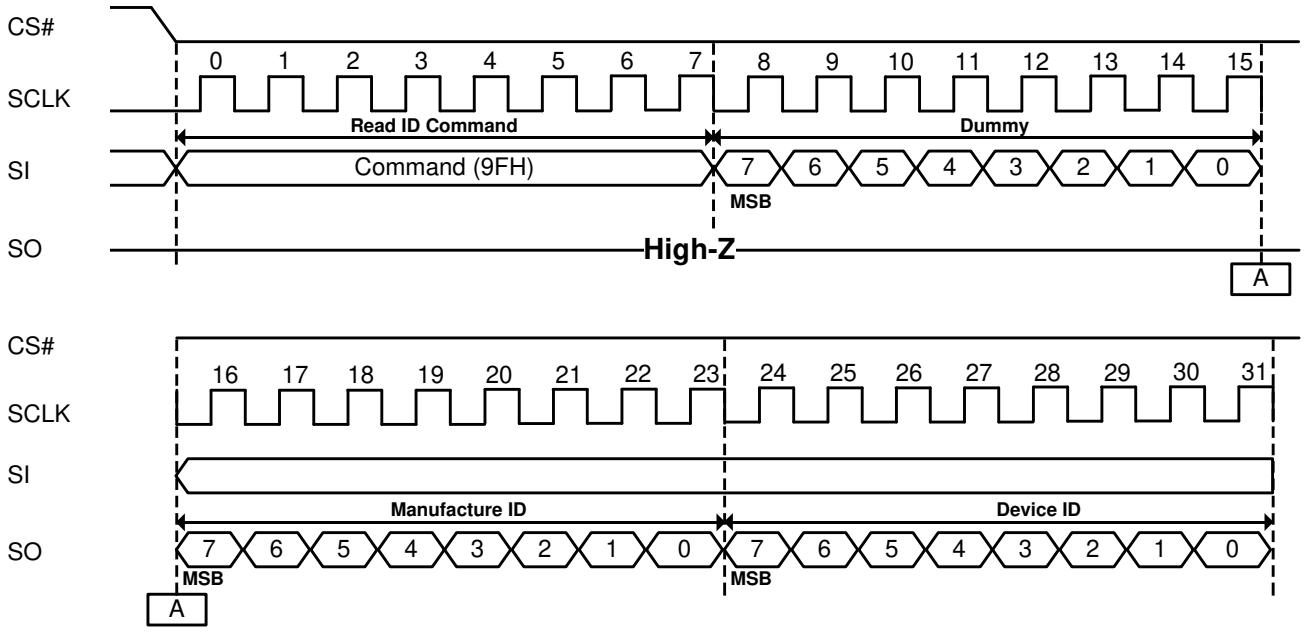


Figure 6-1. Read ID (9FH) Sequence Diagram

Table 6-1. ID Definition Table

Address Byte	Value	R/W	Description
00h	01h	R	Manufacturer ID
01h	15h	R	Device ID

6.2 Page Read

The Page Read (13H) command transfers the data from the NAND array to the cache memory. The command sequence is described as follows:

I. 13H (Page Read to Cache)
II. 0FH (GET FEATURE command to read the status)
III. Read from Cache memory
- 03H or 0BH (Read from Cache x1 IO) / 3BH (Read from Cache x2 IO) / 6BH (Read from Cache x4 IO)
- BBH (Read from Cache Dual IO) / EBH (Read from Cache Quad IO)

The Page Read command requires a 24-bit address consisting of dummy bits and block/page address bits. After the block/page addresses are registered, the device starts transferring from the main array to the cache register, and is busy for tRD time. During the busy time, the GET FEATURE command needs to be issued to monitor the status of Page Read. After finishing the Page Read successfully, the Read from Cache command can be issued in order to read the data out of the cache. The Read from Cache command requires 16 bits of column address which consists of wrap bits and column address bits. The number of bits of column address depends on the page size in different flash. Refer to figures below to view the entire READ operation.

6.2.1 Page Read to Cache (13H)

The waveform of Page Read to Cache (13H) is shown as follows, Do not toggle the CS# until the “Status Register” check is completed.

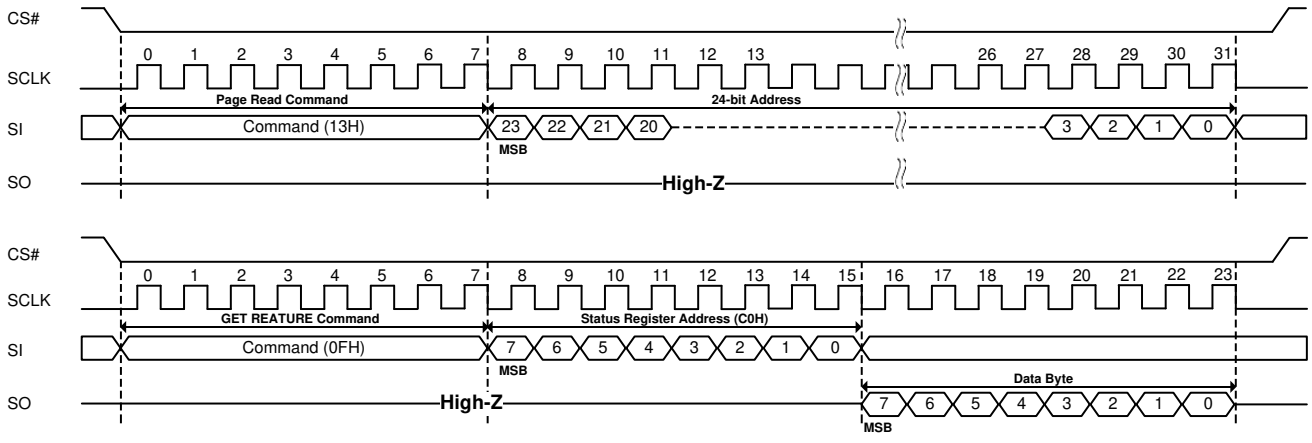


Figure 6-2. Page Read to Cache (13H) Sequence Diagram

6.2.2 Read from Cache x1 IO (03H/0BH)

The Read from Cache x1 IO (03H/0BH) consists of an OP code followed by 16-bit column address. The column address is composed of wrap bits and column address bits.

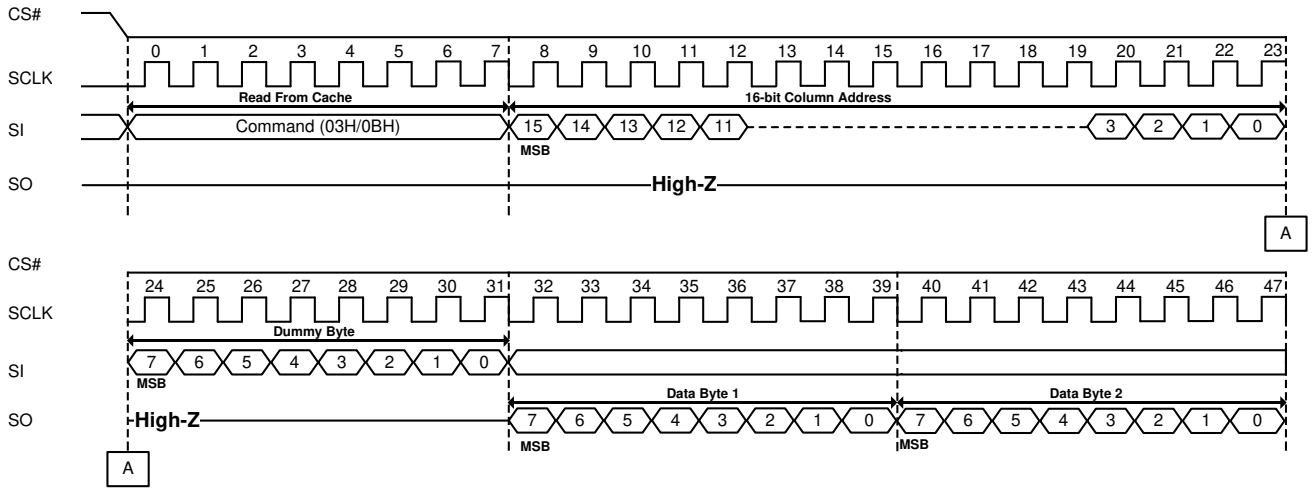


Figure 6-3. Read from Cache x1 IO (03H/0BH) Sequence Diagram

6.2.3 Read from Cache x2 IO (3BH)

The Read from Cache x2 IO (3BH) command is similar to the Read from Cache x1 IO (03H/0BH) but the command uses two pins to output data. The data output pins include the SI (SIO0) and the SO (SIO1).

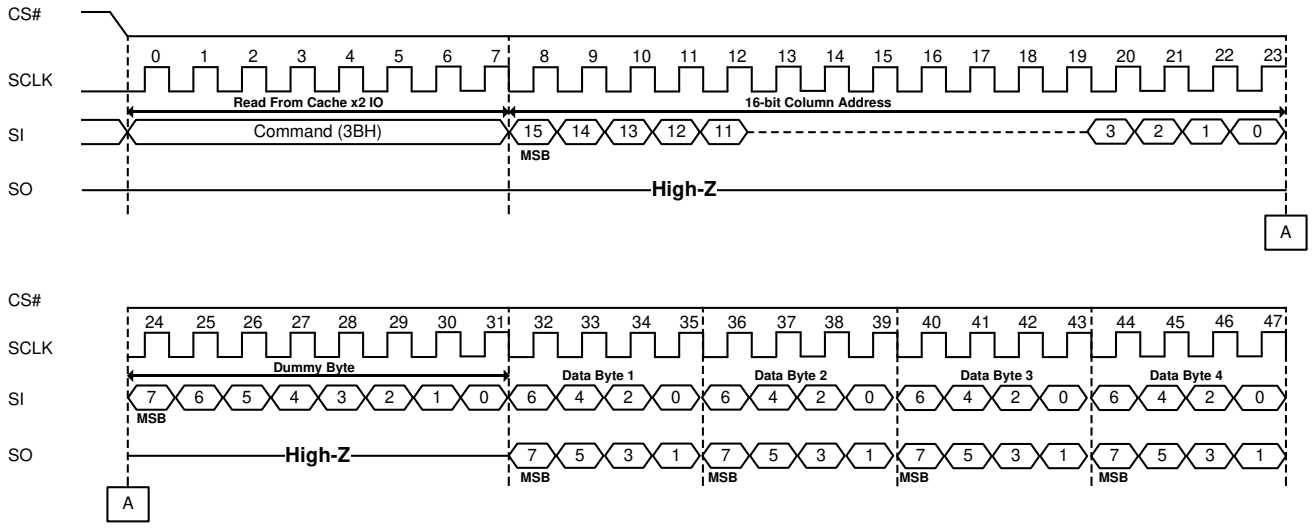


Figure 6-4. Read from Cache x2 IO (3BH) Sequence Diagram

6.2.4 Read from Cache x4 IO (6BH)

The Read from Cache x4 IO (6BH) command is similar to the Read from Cache x1 IO (03H/0BH) and the Read from Cache x2 IO (3BH) but the command uses four pins to output data. The four pins include the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

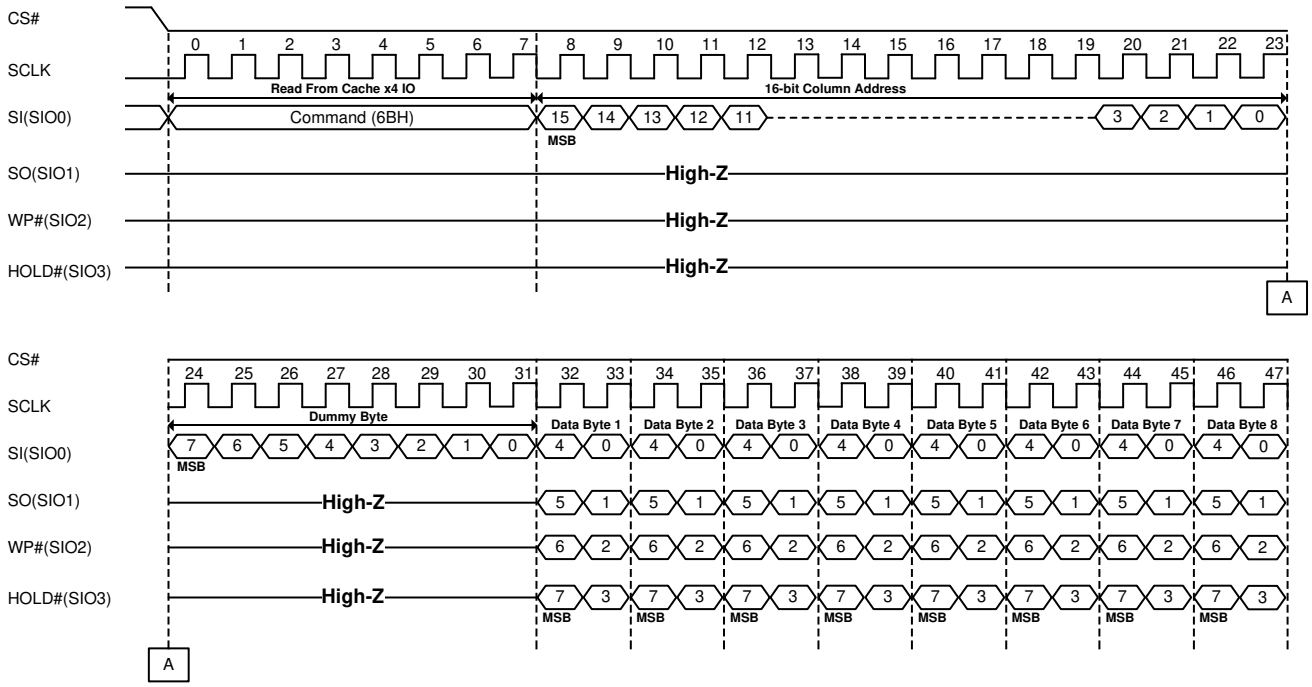


Figure 6-5. Read from Cache x4 IO (6BH) Sequence Diagram

6.2.5 Read from Cache Dual IO (BBH)

The Read from Cache Dual IO command (BBH) is similar to the Read from Cache x2 IO command (3BH) and uses both of SI (SIO0) and SO (SIO1) as input bin. Each bit in 16-bit column address and the followed dummy byte will be latched in during the falling edge of SCLK, then the cache contents will be shifted out 2-bit in a clock cycle through the SI (SIO0) and the SO (SIO1).

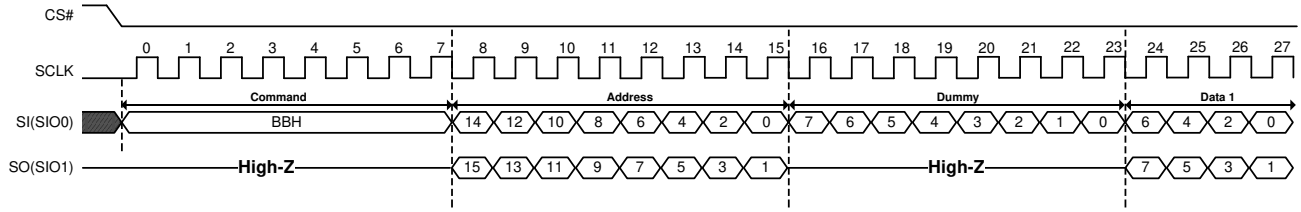


Figure 6-6. Read from Cache Dual IO (BBH) Sequence Diagram

6.2.6 Read from Cache Quad IO (EBH)

The Read from Cache Quad IO (EBH) command is similar to the Read from Cache x4 IO (6BH) command and has 4 input pins which are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). Each bit in 16-bit column address and the followed dummy byte will be latched in during the raising edge of SCLK through these four input pins, and then the cache contents will be shifted out 4-bit in a clock cycle through SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

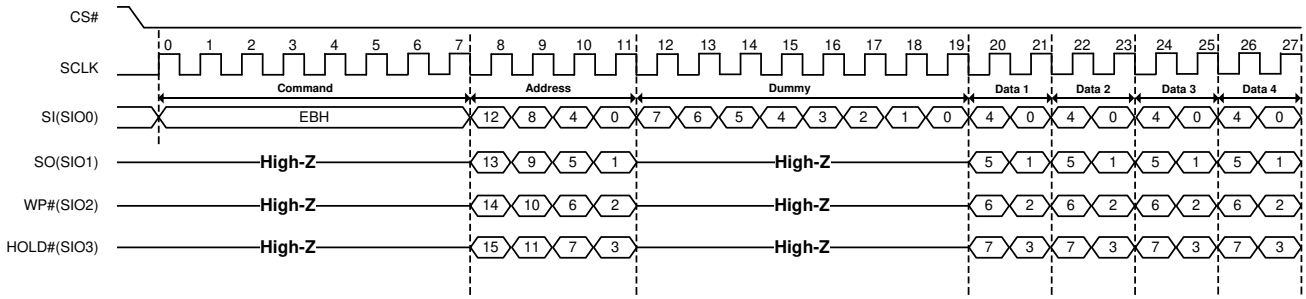


Figure 6-7. Read from Cache Quad (EBH) Sequence Diagram

7 Program Operations

The PAGE PROGRAM sequence transfers the data from the host to NAND flash array through cache memory. The operation sequence programs the first byte to last byte of data within a page. If more than page size, then those additional bytes are ignored by the cache memory. The PAGE PROGRAM sequence is as follows:

I. 06H (WRITE ENABLE when WEL bit is 0)
II. PROGRAM LOAD
- 02H (PROGRAM LOAD) / 32H (PROGRAM LOAD x4)
III. 10H (PROGRAM EXECUTE)
IV. 0FH (GET FEATURE command to read the status)

At first, the WRITE ENABLE (06H) command is used to set the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to issuing a program execute (10h). The PROGRAM LOAD (02H/32H) command is issued then and the PROGRAM LOAD command can only be issued one time in a PAGE PROGRAM sequence. Secondly, the PROGRAM EXECUTE (10H) command is issued to program the data into the page. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE PROGRAM. After finishing the PAGE PROGRAM successfully, the OIP and WEL bit in status register (C0H) will be set to 0.

7.1 Program Load (PL) (02H)

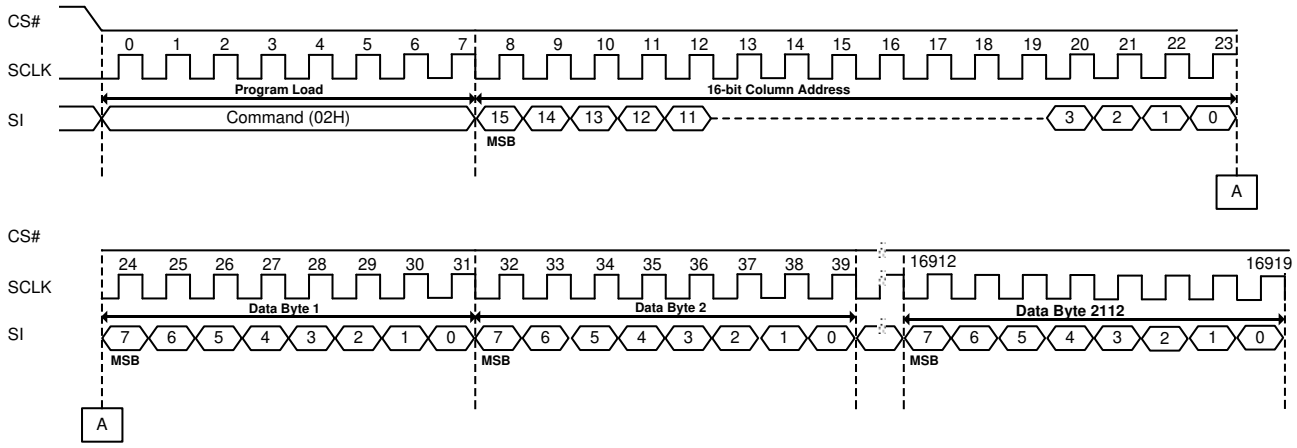


Figure 7-1. Program Load (02H) Sequence Diagram

7.2 Program Load x4 IO (PL x4) (32H)

The PROGRAM LOAD x4 IO (32H) command is similar to the PROGRAM LOAD (02H) command but with four input pins to transfer data in. The four input pins are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

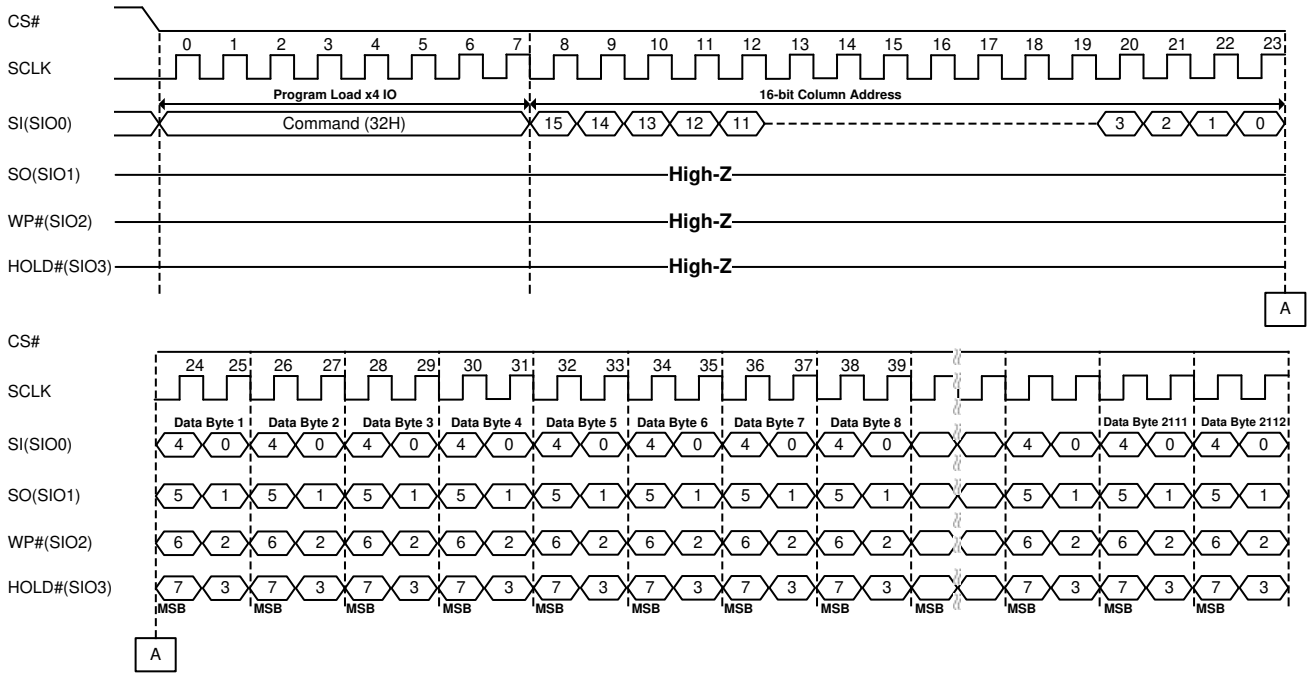


Figure 7-2. Program Load x4 IO (32H) Sequence Diagram

7.3 Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) command must be issued after the data is loaded and the WEL bit is set to HIGH. The PROGRAM EXECUTE (10H) command will transfer data from the cache to the main array. The PROGRAM EXECUTE (10H) consists of an 8-bit Op code, followed by a 24-bit address which including dummy bits and page/block address. This operation needs to wait the busy time. The OIP bit in status register (C0H) will be HIGH until controller finishes the program. The P_FAIL bit in status register (C0H) will be set HIGH if program fail.

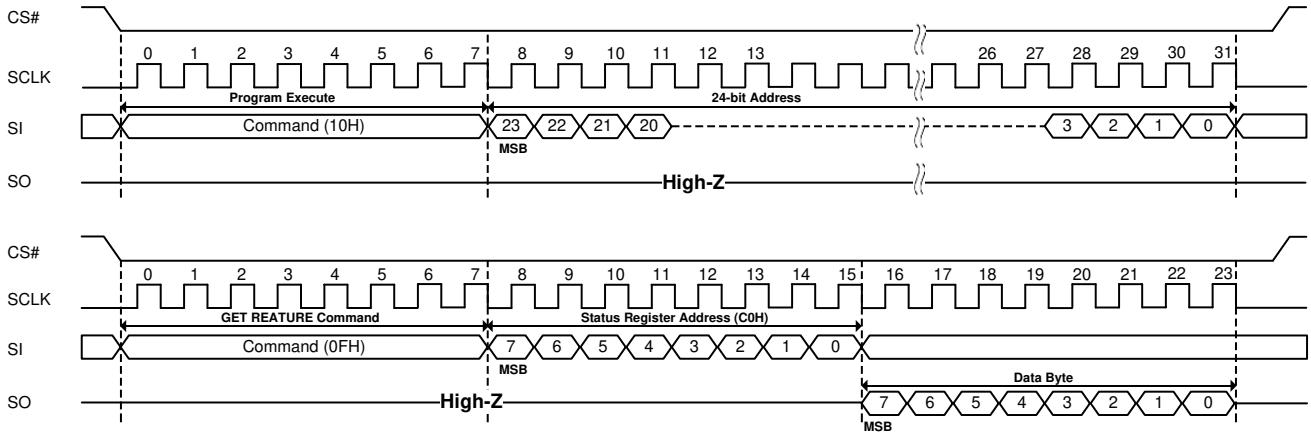


Figure 7-3. Program Execute (10H) Sequence Diagram

8 Erase Operation- Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as follows:

I. 06H (WRITE ENABLE command)
II. D8H (BLOCK ERASE command)
III. 0FH (GET FEATURE command to read the status register)

Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically).

Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit in status register can reflect whether the block be erased successfully or not.

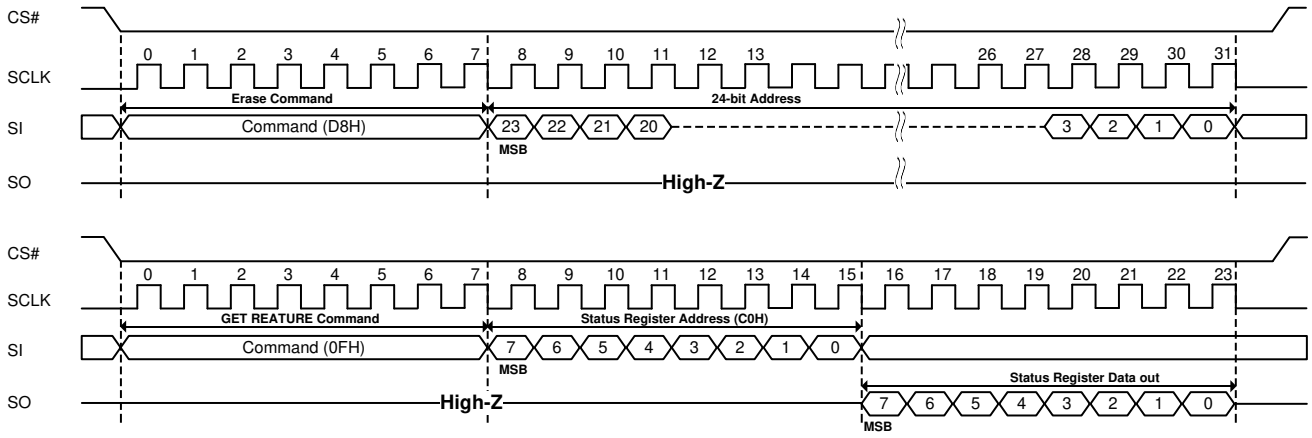


Figure 8-1. Block Erase (D8H) Sequence Diagram

9 Power-On Process and Reset Operation

During Power on Reset, the first page data of page 0 is auto-loaded to the buffer register.

The reset command FFh, does not clear the feature registers but does clear the configuration register bits CFG[2:0] placing the device in normal operation.

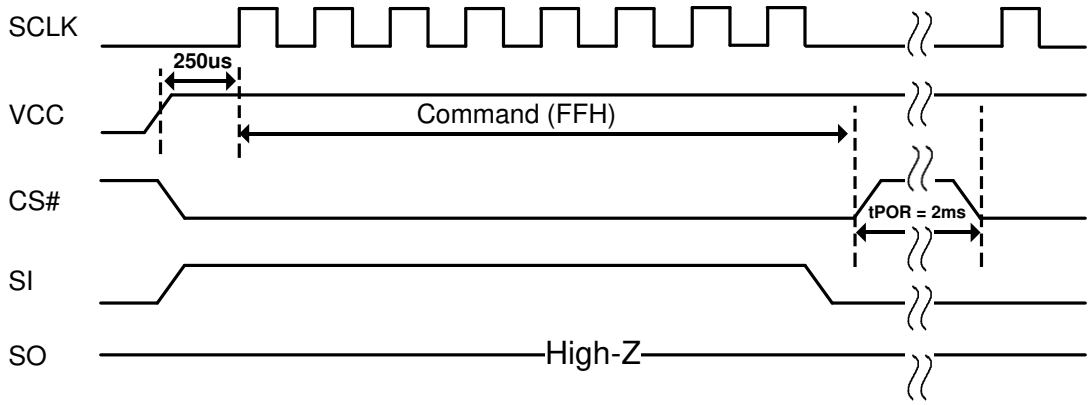


Figure 9-1. Power Up Timing Diagram

10 One-Time Programmable (OTP) Function

10.1 OTP Definition

Table 10-1. OTP State

CFG2	CFG1	CFG0	Description
0	0	0	Normal Operation (default)
0	1	0	Access OTP Area
1	1	0	Access to OTP data protection bit to lock OTP area

Note: The device contains a one-time programmable (OTP) area, that consists of (62 pages), accessed by SET/GET FEATURES commands.

10.2 OTP Read

OTP Read: 62 pages accessible for user data located in Block 6 from page 2 to page 63

1. Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x50.
2. Page Read command (13h) with Block/Page address (0x0182-0x01BF).
   GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready.
3. Read Buffer (03h) command to read the data out.
4. Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x10 to exit.
5. Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

10.3 OTP Program

OTP Program: 62 pages accessible for user data located in Block 6 from page 2 to page 63

1. Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x50 for ECC enabled.
2. Use Write Enable command 06h.
3. Program using Load command x1 (02h), Quad Program Data Load (32h).
4. Program Execute command x1 (10h) with Block/Page address (0x0182-0x01BF).
5. Use GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready.
6. Use SET FEATURES command (1Fh) with feature address B0h and value of 0x10 to exit.
7. After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verify P_Fail bit is not set.

10.4 OTP Data Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. The following sequence is used to protect and prevent further programming of the OTP area:

1. Use SET FEATURES command (1Fh) with feature address B0h and data value of 0xC0.
2. Use Write Enable command 06h.
3. Program execute command (10h) with row address 00h.
4. Verify until OIP bit not busy and P_FAIL bit 0 using GET FEATURE command (0Fh) with status register address (C0h).

11 Hardware Write Protection (HWP)

Hardware write protection prevents the block protection state from hardware modifications.

The following command sequence enables hardware write protection: The SET FEATURE command is issued on feature address A0h. Then, the HWP_EN bit-state is set to 0 as the default after power up.

The BRWD bit is operated in conjunction with HWP_EN bit. When BRWD is set to 1 and WP# is LOW, none of the other block protect register A0H bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked. Also, when the WP#/Hold# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and HWP_EN bits = 0 after power up.

Table 11-1. Block Protect Bits Table (A0H [6:2])

BP3	BP2	BP1	BP0	INV	Protect Rows
0	0	0	0	X	All Blocks Unlocked
0	0	0	1	0	Lower 1/1024 Blocks Locked
0	0	1	0	0	Lower 1/512 Blocks Locked
0	0	1	1	0	Lower 1/256 Blocks Locked
0	1	0	0	0	Lower 1/128 Blocks Locked
0	1	0	1	0	Lower 1/64 Blocks Locked
0	1	1	0	0	Lower 1/32 Blocks Locked
0	1	1	1	0	Lower 1/16 Blocks Locked
1	0	0	0	0	Lower 1/8 Blocks Locked
1	0	0	1	0	Lower 1/4 Blocks Locked
1	0	1	0	0	Lower 1/2 Blocks Locked
1	0	1	1	0	All Blocks Locked
0	0	0	1	1	Upper 1/1024 Blocks Locked
0	0	1	0	1	Upper 1/512 Blocks Locked
0	0	1	1	1	Upper 1/256 Blocks Locked
0	1	0	0	1	Upper 1/128 Blocks Locked
0	1	0	1	1	Upper 1/64 Blocks Locked
0	1	1	0	1	Upper 1/32 Blocks Locked
0	1	1	1	1	Upper 1/16 Blocks Locked
1	0	0	0	1	Upper 1/8 Blocks Locked
1	0	0	1	1	Upper 1/4 Blocks Locked
1	0	1	0	1	Upper 1/2 Blocks Locked
1	0	1	1	1	All Blocks Locked
1	1	X	X	X	All Blocks Locked
1	1	1	1	1	All Blocks Locked (default)

1. The feature registers are volatile. Each POR will reset these registers to the default value (0x7C).
2. HWP_EN must be enabled first before block unlock region is set

12 Status Register

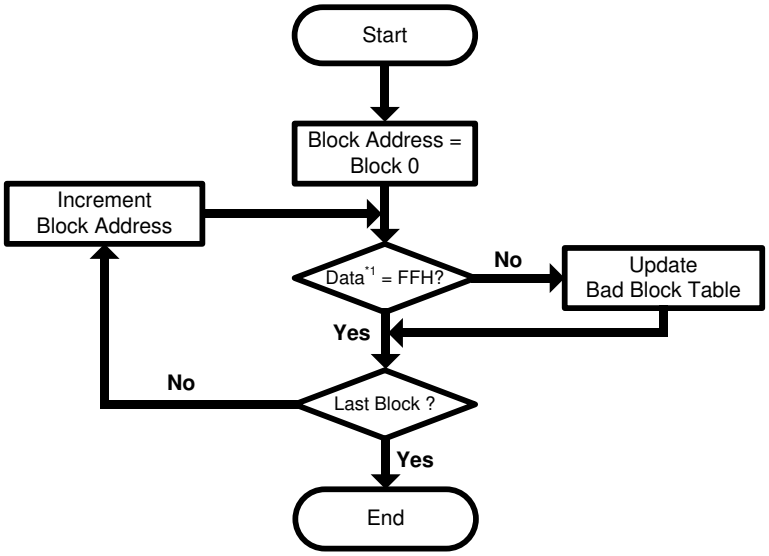
The content of status register can be read by issuing the GET FEATURE (0FH) command, followed by the status register address C0H. The meaning of each bit in status register is listed as follows:

Table 12-1. Status Register Bit Description

Bit	Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred. It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command.
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred. It will also be set if the user attempts to erase a locked region. This bit is cleared at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates that the current status of the write enable latch(WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS1, ECCS0	ECC Status	This bit provides ECC status as follows: 00b = No bit errors were detected 01b = 1-2 bit error corrected 10b = 3-4 bit error corrected 11b = uncorrectable

13 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written before shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block. The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. Blocks 0 - 9 are guaranteed good at the time of shipment.



*1: Check for FFh at the 1st byte in the spare area of the 1st, 2nd, and last pages.

Figure 13-1. Bad Block Test Flow

Table 13-1. Valid Block Information

	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	1004	-	1024	Blocks

14 Absolute Maximum Ratings

Table 14-1. Absolute Maximum Ratings

Symbol	Parameters	Max	Unit
TBIAS	Temperature under Bias	-40 ~ 105	°C
TSTG	Storage Temperature	-55 ~ 125	°C
VIO	Input or Output Voltage(3.3V)	-0.6 ~ 4.6	V
VCC	Supply Voltage(3.3V)	-0.6 ~ 4.6	V

Notes:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the table Absolute Maximum Ratings “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.
3. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions.

Table 14-2. Recommended Operating Conditions

Symbol	Parameters	Max	Unit
TA	Ambient Operating Temperature	-40 ~ 85	°C
VCC	VCC Supply Voltage (Typical 3.3V)	2.7 ~ 3.3	V

15 Characteristics

Table 15-1. Operation Characteristics

Parameters	Min	Typ	Max	Unit
Erase one block	-	4	10	ms
Program from cache to flash	-	350	600	us
Read from flash into cache	-	45	250	us
Reset Time (Ready /Read /Program /Erase)	-	-	5 /6 /10 /500	us

Table 15-2. DC Characteristics

Symbol	Parameters (Test Conditions)	Min	Typ	Max	Unit
ICC1	Standby current (CS# = VIH, Vin= 0V or VCC)	-	20	100	µA
ICC2	Read current	-	25	35	mA
ICC3	Array program current	-	20	25	mA
ICC4	Array erase current	-	20	25	mA
ILI	Input leakage current	-	-	±10	µA
ILO	Output leakage current	-	-	±10	µA
VIH	DC Input high voltage	VCC x 0.8	-	VCC + 0.3	V
VIL	DC Input low voltage	-0.3	-	VCC x 0.2	V
VOH	Output high voltage (IOH=-400 µA)	2.4	-	-	V
VOL	Output low voltage (IOL=2.1mA)	-	-	0.4	V
VLKO	Erase and program lockout voltage	-	1.8	-	V

Table 15-3. AC Characteristics (T = -40 ~ 85°C, V = 2.7 ~ 3.6V, CL = 30pF)

Parameters	Symbol	Min	Typ	Max	Unit
Clock Frequency	FC	-	-	104	MHz
Clock High Time	tCH	4.316	-	-	ns
Clock Low Time	tCL	4.316	-	-	ns
Serial Clock Rise Time	tCLCH	1.3	-	-	V/ns
Serial Clock Fall Time	tCHCL	1.3	-	-	V/ns
CS# Active Setup Time	tSLCH	4.316	-	-	ns
CS# Active Hold Time	tCHSH	4.316	-	-	ns
CS# Not Active Setup Time	tSHCH	2.877	-	-	ns
CS# Not Active Hold Time	tCHSL	2.877	-	-	ns
CS# High Time	tSHSL / tCS	30	-	-	ns
Output Disable Time	tSHQZ	-	-	10	ns
Output Hold Time	tCLQX	2	-	-	ns
Data In Setup Time	tDVCH	2.5	-	-	ns
Data In Hold Time	tCHDX	1.75	-	-	ns
Hold# Low Setup Time relative to Clock	tHLCH	5	-	-	ns
Hold# High Setup Time relative to Clock	tHHCH	5	-	-	ns
Hold# High Hold Time relative to Clock	tCHHL	5	-	-	ns
Hold# Low Hold Time relative to Clock	tCHHH	5	-	-	ns
Hold# Low To High-Z Output	tHLQZ	-	-	12	ns
Hold# High To Output	tHHQX	-	-	9	ns
Clock Low To Output Valid	tCLQV	-	-	7	ns
WP# Setup Time Before CS# Low	tWHSL	20	-	-	ns
WP# Hold Time After CS# High	tSHWL	100	-	-	ns
Data transfer from cell to register tR with internal ECC on	tR	-	45	250	µs

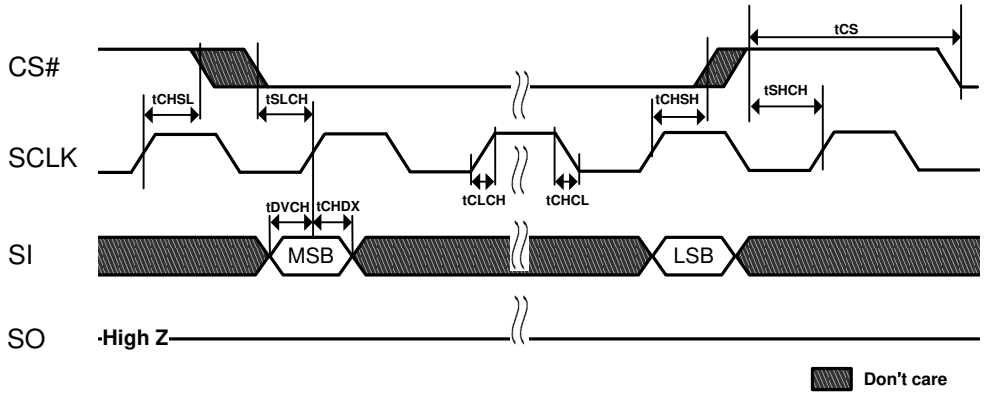


Figure 15-1. Serial Input Timing

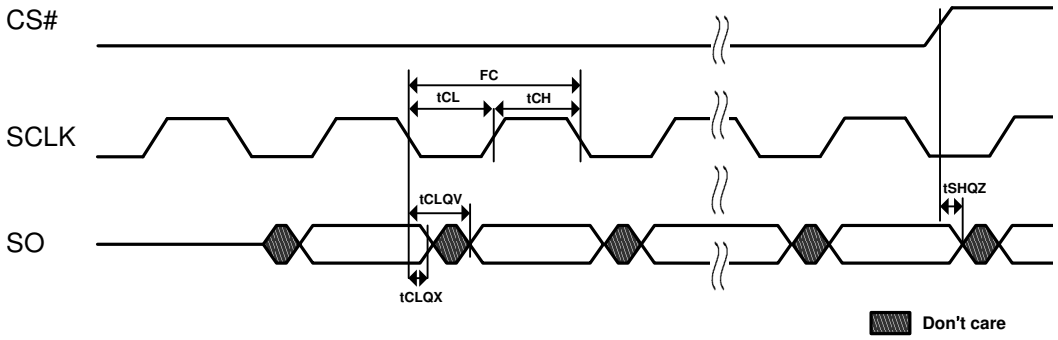


Figure 15-2. Serial Output Timing

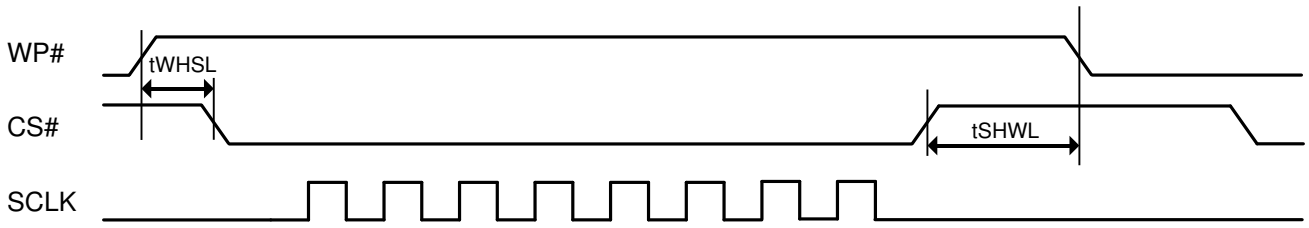


Figure 15-3. WP# Timing

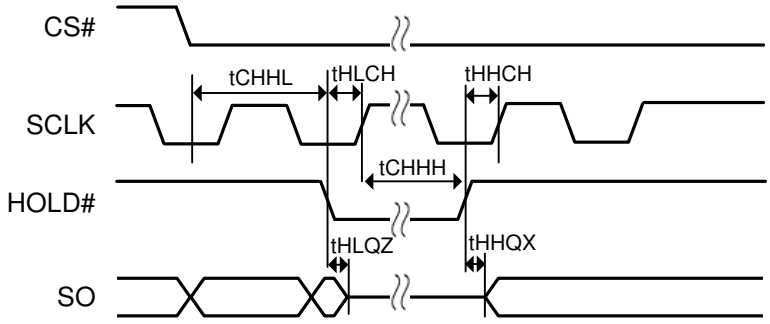


Figure 15-4. HOLD# Timing

16 Package Outline Information

Table 16-1. LGA (8 x 6 x 0.8mm) Dimension Table

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.0276	0.0295	0.0315	0.70	0.75	0.80
A1	0.021 BASIC			0.53 BASIC		
D	0.311	0.315	0.319	7.90	8.00	8.10
E	0.232	0.236	0.240	5.90	6.00	6.10
D1	0.295 BASIC			7.50 BASIC		
E1	0.150 BASIC			3.81 BASIC		
e	0.050 BASIC			1.27 BASIC		
b	0.014	0.016	0.018	0.35	0.40	0.45
L	0.018	0.020	0.022	0.45	0.50	0.55
L1	0.167	0.169	0.171	4.25	4.30	4.35
L2	0.132	0.134	0.136	3.35	3.40	3.45
R	0.008 BASIC			0.20 REF		
K	0.018 BASIC			0.45 REF		

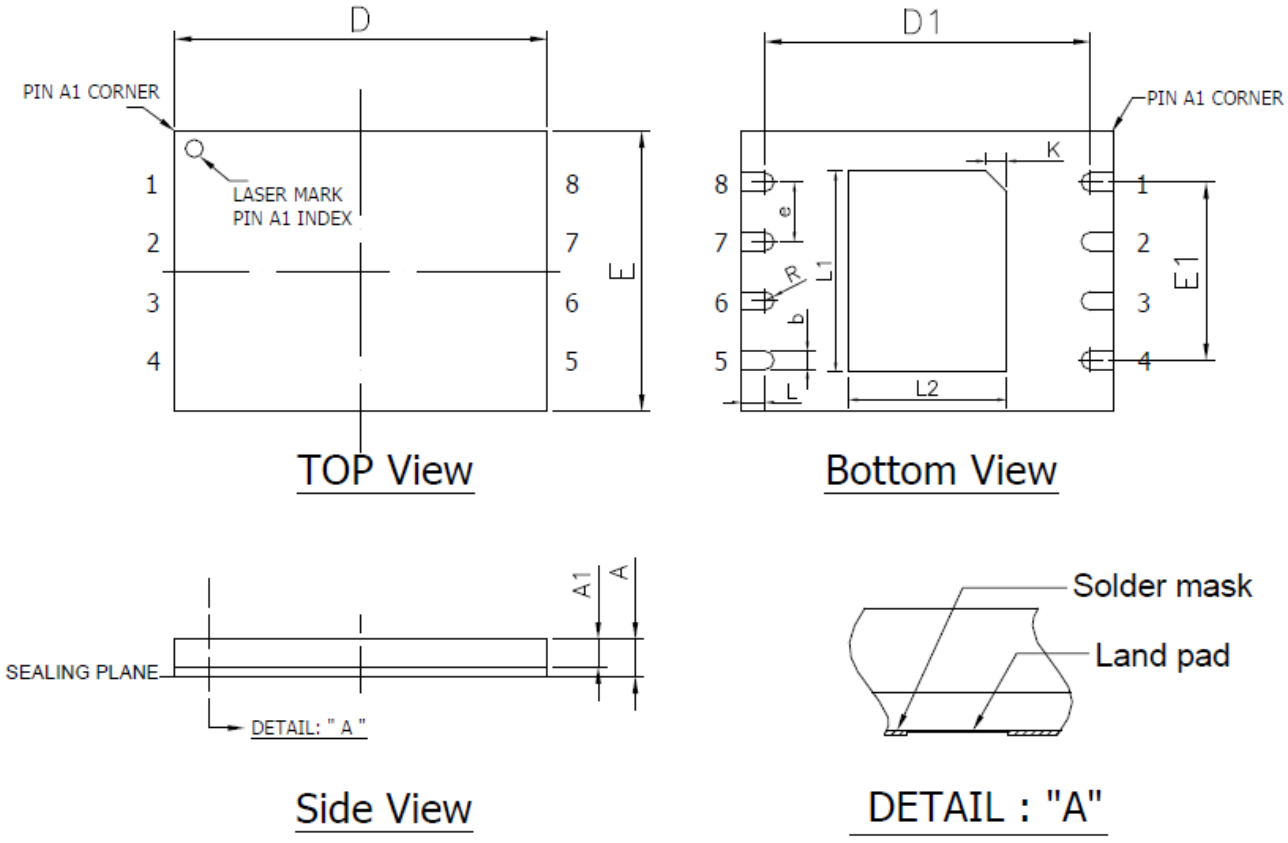


Figure 16-1. LGA (8 x 6 x 0.8mm) Package Outline Drawing Information