Etron 鈺創科技
Etron Technology, Inc.

SPI NAND Flash Datasheet

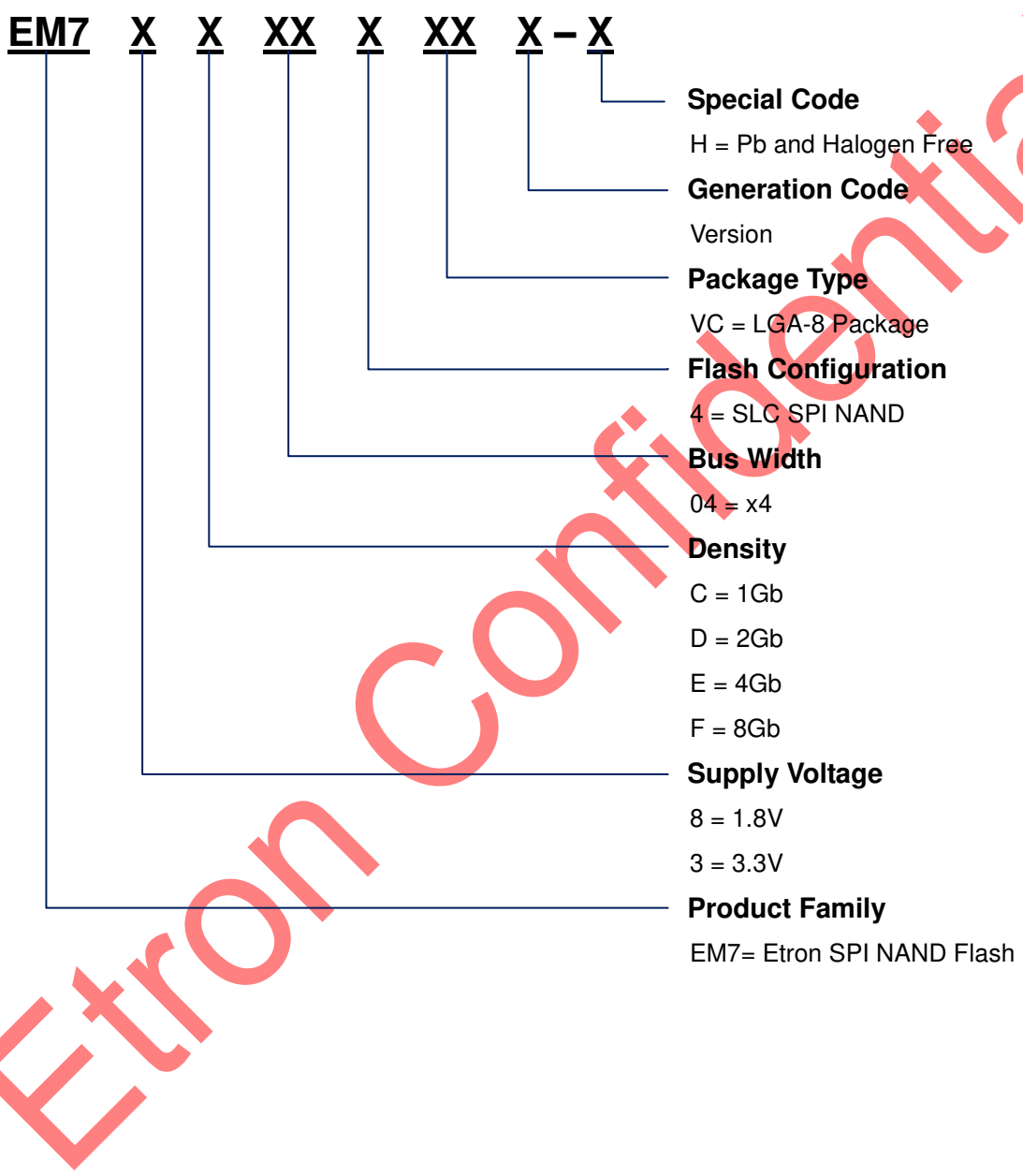
Serial Peripheral Interface (SPI)

Model
EM73C044VCF-H

Advance
Revision 1.00
November 29, 2021

SPI NAND Part Numbering Information

Etron SPI NAND Flash devices are categorized in the following diagram based on the features and densities



Etron Technology, Inc. reserves the right to change products or specification without notice.

Revision History

Rev	Date	Comments
1.00	November 29, 2021	Initial release

Contents

List of Figures

List of Tables

1 Introduction

1.1 Features

- **Single-Level Cell (SLC) NAND Flash**
- **Operating Voltage Support**
  - VCC: 3.3V (3.0V to 3.6V)
- **Clock Frequency**
  - Up to 120MHz
- **Standard, Dual and Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- **ECC Protection**
  - 4bit ECC for each 512bytes + 16bytes
- **Package (Pb Free and Halogen Free)**
  - 8-pin LGA-8 (8 x 6 x 0.8mm)
- **OTP Protection**
  - 64 pages one time programmable
- **Performance (Typical)**
  - Page Program Time: 600us
  - Page Read Time: 70us
  - Block Erase Time: 3ms
- **Operating Current**
  - Read Operation Current: 25mA
  - Program Operation Current: 25mA
  - Erase Operation Current: 30mA
  - 120uA maximum standby current
- Endurance
  - P/E cycles: more than 60,000/cycles
- Data Retention
  - 10/years
- **Temperature**
  - Operating Temperature: -40°C to +85°C
  - Storage Temperature: -65°C to +150°C

Table 1-1. Product Information

Part Number	Density	VCC	ECC	Page Size	Block	Device	Package
EM73C044VCF-H	1Gbits	3.3V	4bit	2048+64 Bytes	64 Pages	1024 Blocks	LGA-8

1.2 General Description

SPI (Serial Peripheral Interface) NAND provides a low cost and low pin count solution to alternate SPI-NOR in high density non-volatile memory storage solution for embedded systems.

SPI NAND is a flash memory device with SLC NAND of the standard parallel NAND. The serial electrical interface follows the industry-standard serial peripheral interface. The command sets are similar to SPI-NOR command sets. Some modifications have been made for handling NAND-specific functions. Besides, new features are added to extend applications. The SPI NAND has 8 pin counts in total, including six signal lines plus VCC and GND.

Each block of the serial NAND is subdivided into 64 programmable pages. Each page consists of a data storage region and a spare area. The data storage region is used to store user-programmed data and the spare area is typically used for memory management and error correction functions.

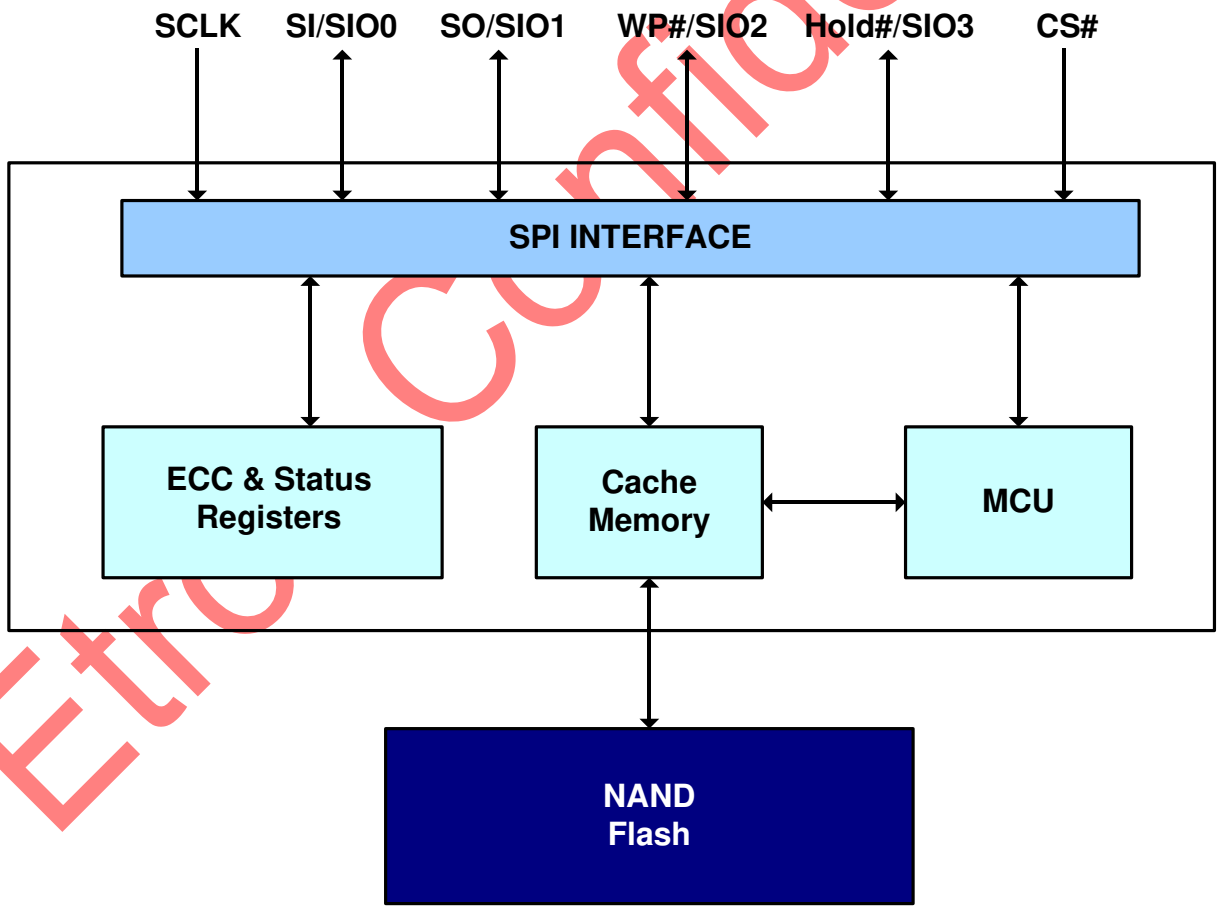


Figure 1-1. Functional Block Diagram

1.3 Memory Mapping Diagram

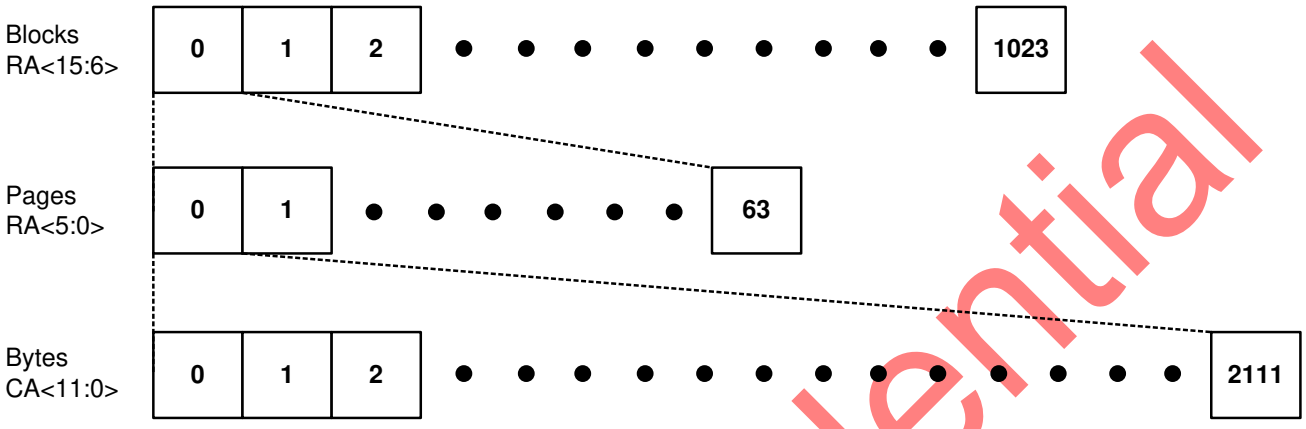


Figure 1-2. Memory Mapping Diagram

Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

1.4 ECC Protection and Spare Area

Table 1-2. ECC Protection and Spare Area

Start Address	End Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main Area 01	Data storage region 01
200h	3FFh	Yes	Main Area 02	Data storage region 02
400h	5FFh	Yes	Main Area 03	Data storage region 03
600h	7FFh	Yes	Main Area 04	Data storage region 04
800h	803h	No(2)	Spare Area 01	Meta data 01-1
804h	807h	Yes		Meta data 01-2
808h	80Bh	No(2)	Spare Area 02	Meta data 02-1
80Ch	80Fh	Yes		Meta data 02-2
810h	813h	No(2)	Spare Area 03	Meta data 03-1
814h	817h	Yes		Meta data 03-2
818h	81Bh	No(2)	Spare Area 04	Meta data 04-1
81Ch	81Fh	Yes		Meta data 04-2
820h	83Fh	Yes	Spare Area 05	Internal ECC parity area(1)

Notes:

1. When ECC is enabled, the internal ECC parity area only can be read, and the data is 'FF'.
2. The 1st to 4th bytes in the meta data are unprotected by ECC.

1.5 Pin Configuration

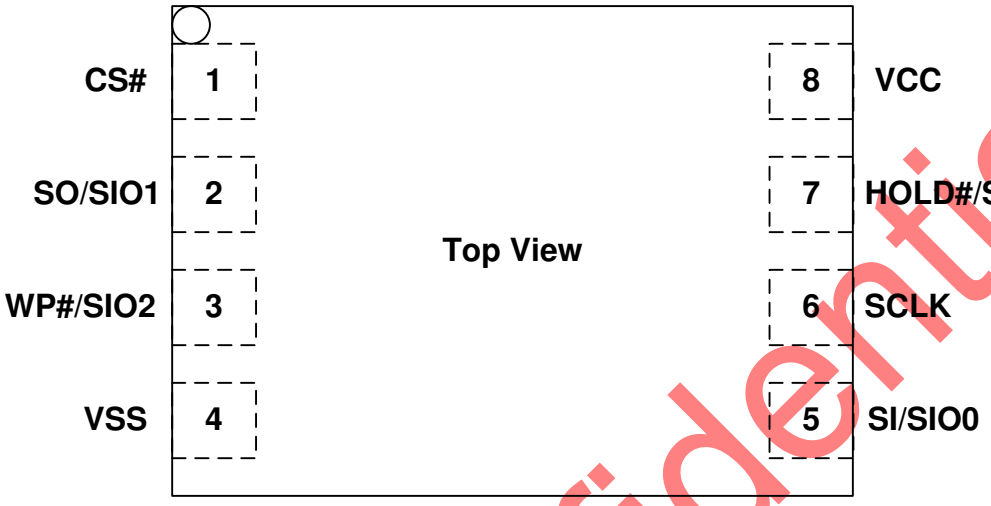


Figure 1-3. Pin Assignments

Table 1-3. Pin Descriptions

Pin Name	Type	Description
CS#	Input	Chip Select
SCLK	Input	Serial Clock
SI/SIO0	I/O	Serial Data Input / Serial Data IO0
SO/SIO1	I/O	Serial Data Output / Serial Data IO1
WP#/SIO2	I/O	Write Protect / Serial Data IO2
Hold#/SIO3	I/O	Hold / Serial Data IO3
VCC	Supply	Power Supply
VSS	Ground	Ground

2 Device Operation

2.1 SPI Mode

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams shown in this data sheet are mode 0.

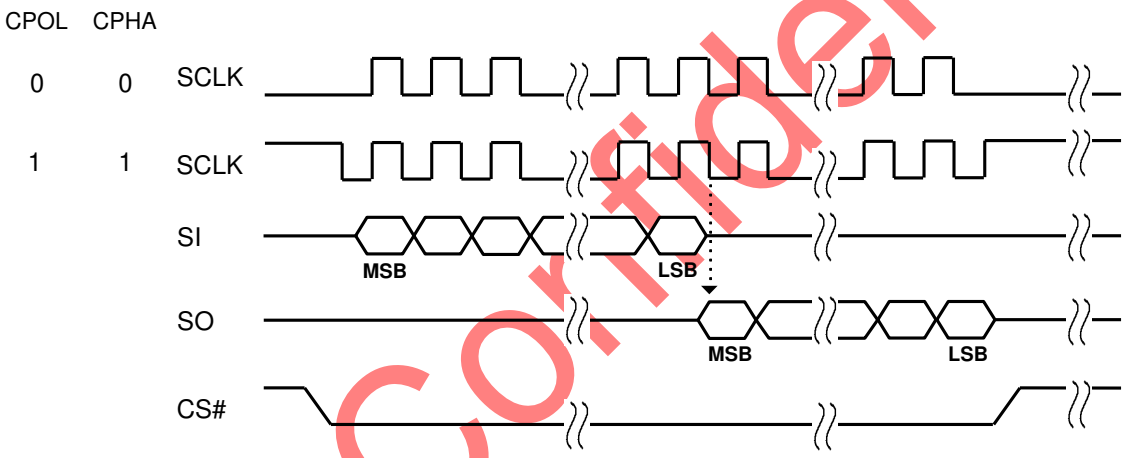


Figure 2-1. Timing Diagram of SPI Modes

Note:

1. SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
2. When CS# is 0, the device is placed in active mode. When CS# goes 1, the device is placed in inactive mode and SO is High-Z.

2.1.1 Standard SPI

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO).

2.1.2 Dual SPI

The device supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1.

2.1.3 Quad SPI

The device supports the x4 and Quad commands operation. These commands allow data to be transferred to or from the device at four times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1. The WP# and the HOLD# pins become SIO2 and SIO3. Once use the Quad SPI Mode, the Quad Enable (QE) bit of OTP register (B0[0]) must be set to 1[1].

[1] Reference the Table 3-1 and the Table 5-1.

2.2 Hold Mode

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of writing status register, programming or erasing in progress.

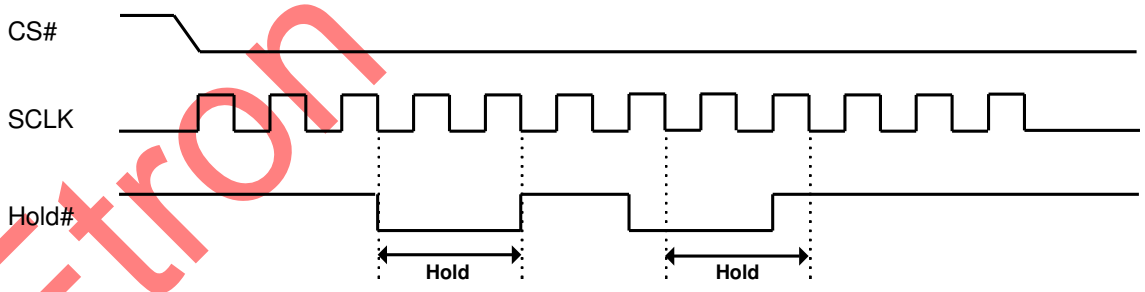


Figure 2-2. Hold Condition Diagram

Note:
Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. When SCLK is HIGH and HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

2.3 Write Protection Mode

Write protect (WP#) provides hardware protection mode. The WP# prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

3 Commands Description

Table 3-1. SPI NAND Command Set

Command	Op Code	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Nth Byte
Write Disable	04H	-	-	-	-	-	-
Write Enable	06H	-	-	-	-	-	-
Block Erase (Block size)	D8H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Program Load	02H	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load x4 IO	32H	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Execute	10H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Program Load Random Data	84H(1)	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load Random Data x4 IO	C4H/34H(1)	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Load Random Data Quad IO	72H(1)(2)	A15-A0	(D7-D0)x4	Next data	Next data	Next data	-
Page Read (to Cache)	13H(3)	A23-A16	A15-A8	A7-A0	-	-	-
Read from Cache x1 IO	03H/0BH	A15-A8	A7-A0	Dummy	D7-D0	Next data	Wrap
Read from Cache x2 IO	3BH	A15-A8	A7-A0	Dummy	(D7-D0)x2	Next data	Wrap
Read from Cache x4 IO	6BH	A15-A8	A7-A0	Dummy	(D7-D0)x4	Next data	Wrap
Read from Cache Dual IO	BBH	A15-A0	Dummy	(D7-D0)x2	Next data	Next data	Wrap
Read from Cache Quad IO	EBH(2)	A15-A0	Dummy	(D7-D0)x4	Next data	Next data	Wrap
Read ID	9FH(3)	A7-A0	MID	DID	Wrap	Wrap	Wrap
Reset	FFH	-	-	-	-	-	-
Get Feature	0FH(3)	A7-A0	D7-D0	-	-	-	-
Set Feature	1FH(3)	A7-A0	D7-D0	-	-	-	-

Note:

1. These commands are only available in Internal Data Move operation.
2. Quad Enable (QE) bit needs to be set to 1 when these commands are issued.
3. If QE = 1, do not make HOLD#/SIO3 = 0, when these commands are issued.

4 Write Operations

The WRITE ENABLE (WREN, 06H) command is for setting the Write Enable Latch (WEL) bit. The WRITE DISABLE (WRDI, 04H) command is for clearing the WEL bit.

As with any command that changes the memory contents, the WRITE ENABLE command must be executed at first in order to set the WEL bit to 1. For more information, please refer to the Page Read operation sequence, PAGE PROGRAM operation sequence, Internal Data Move operation sequence, BLOCK ERASE operation sequence and OTP operation sequence.

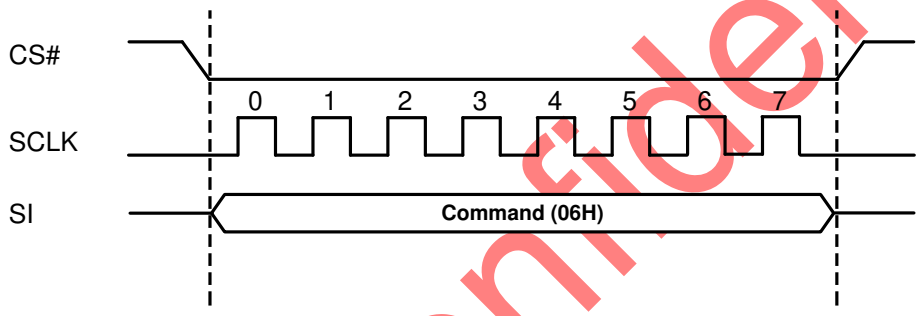


Figure 4-1. Write Enable (06H) Sequence Diagram

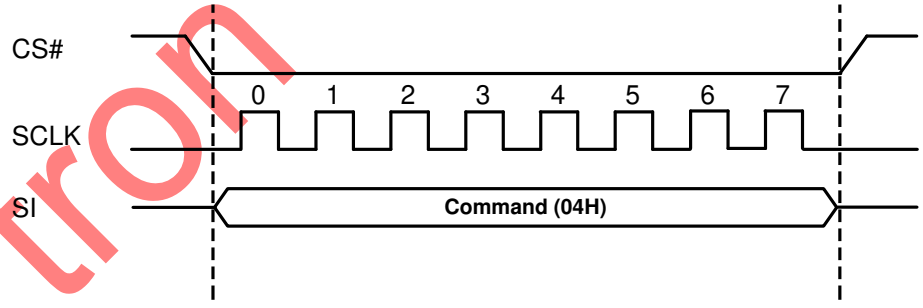


Figure 4-2. Write Disable (04H) Sequence Diagram

5 Feature Operations

The GET FEATURE (0FH) and SET FEATURE (1FH) commands are used to monitor the device status and alter the device behavior.

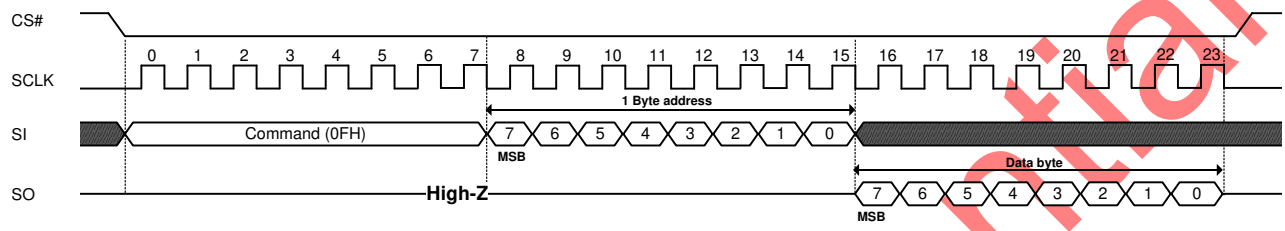
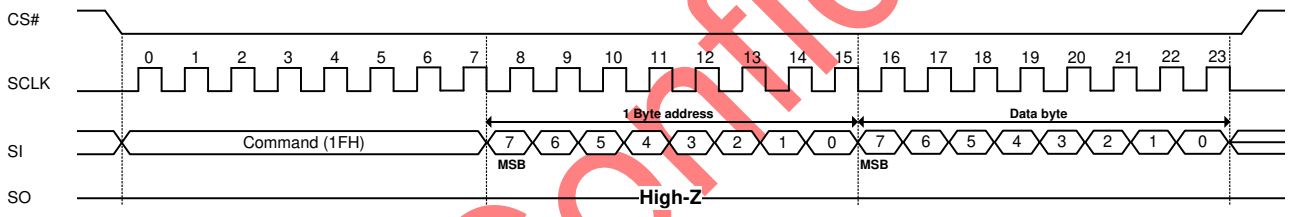


Figure 5-1. Get Feature (0FH) Sequence Diagram



Notes : If the status OIP = 1, the 'Set Feature (1FH)' command will be disable

Figure 5-2. Set Feature (1FH) Sequence Diagram

Table 5-1. Feature Register Table

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0H	BRWD(R/W)	Reserved	BP2(R/W)	BP1(R/W)	BP0(R/W)	INV(R/W)	CMP(R/W)	Reserved
OTP	B0H	OTP_PRT(R)	OTP_EN(R/W)	Reserved	ECC_EN(R/W)	Reserved	Reserved	Reserved	QE(R/W)
Status	C0H	Reserved	Reserved	ECCS1(R)	ECCS0(R)	P_FAIL(R)	E_FAIL(R)	WEL(R)	OIP(R)

Note:

1. (R/W)：This bit can be read & programmed.
2. (R)：This bit only can be read.
3. Reserved：Default value 0h.
4. The ECC status of register C0H will be cleared when ECC is disabled.
5. The default value of feature register is A0H=0x38 , B0H=0x10 , C0H=0x00.

6 Read Operations

6.1 Read ID (9FH)

The Read ID command is used to identify the SPI NAND. The Read ID command outputs the manufacturer ID with address byte 00H and outputs the device ID when address byte is 01H.If the SCLK keeps outputting, the SO will repeatedly outputs the MID/DID.

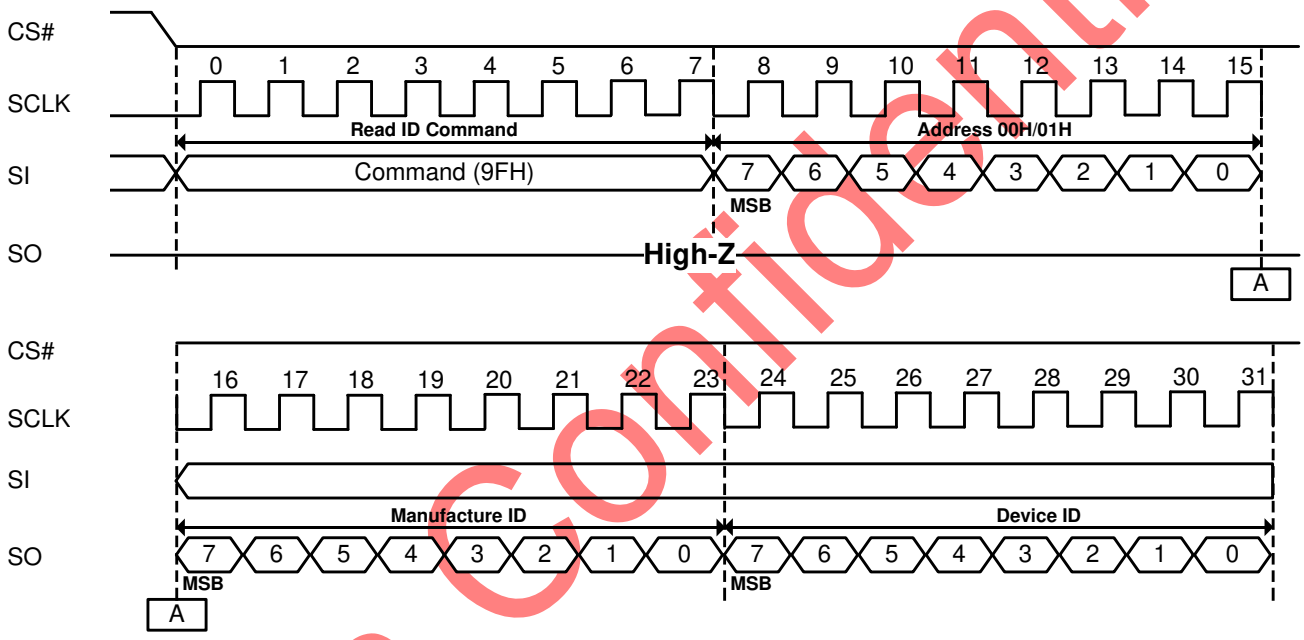


Figure 6-1. Read ID (9FH) Sequence Diagram

Table 6-1. ID Definition Table

Address Byte	Value	R/W	Description
00h	D5h	R	Manufacturer ID: Etron
01h	25h	R	Device ID: EM73C044VCF-H

6.2 Page Read (13H)

The Page Read (13H) command transfers the data from the NAND array to the cache memory. The command sequence is described as follows:

I. 13H (Page Read to Cache)
II. 0FH (GET FEATURE command to read the status)
III. Read from Cache memory
- 03H or 0BH (Read from Cache x1 IO) / 3BH (Read from Cache x2 IO) / 6BH (Read from Cache x4 IO)
- BBH (Read from Cache Dual IO) / EBH (Read from Cache Quad IO)

The Page Read command requires a 24-bit address consisting of dummy bits and block/page address bits. After the block/page addresses are registered, the device starts transferring from the main array to the cache register, and is busy for tRD time. During the busy time, the GET FEATURE command needs to be issued to monitor the status of Page Read. After finishing the Page Read successfully, the OIP bit in status register (C0H) will be set to 0. Then the Read from Cache command can be issued in order to read the data out of the cache.

The Read from Cache command requires 16 bits of column address which consists of wrap bits and column address bits. The number of bits of column address depends on the page size in different flash.

Value of wrap bit is defined as follows:

Table 6-2. 24-bit address consisting of dummy bits and block/page address bits

Row Address	24-Bits Address	
Block	Dummy Bits	Page/Block address bits (1)
1024	RA <23:16>	RA <15:0>

Table 6-3. Wrap Bit Definition (2)

Wrap <2>	Wrap <1>	Wrap <0>	Wrap Length (Byte)
0	0	X	2112
0	1	X	2048
1	0	X	64
1	1	X	16

Note:
1. Please refer the Figure 1-2 .
2. Wrap bit has 3 bits and located at the first 3 bits in 16-bits column address.

6.2.1 Page Read to Cache (13H)

The waveform of Page Read to Cache (13H) is shown as follows:

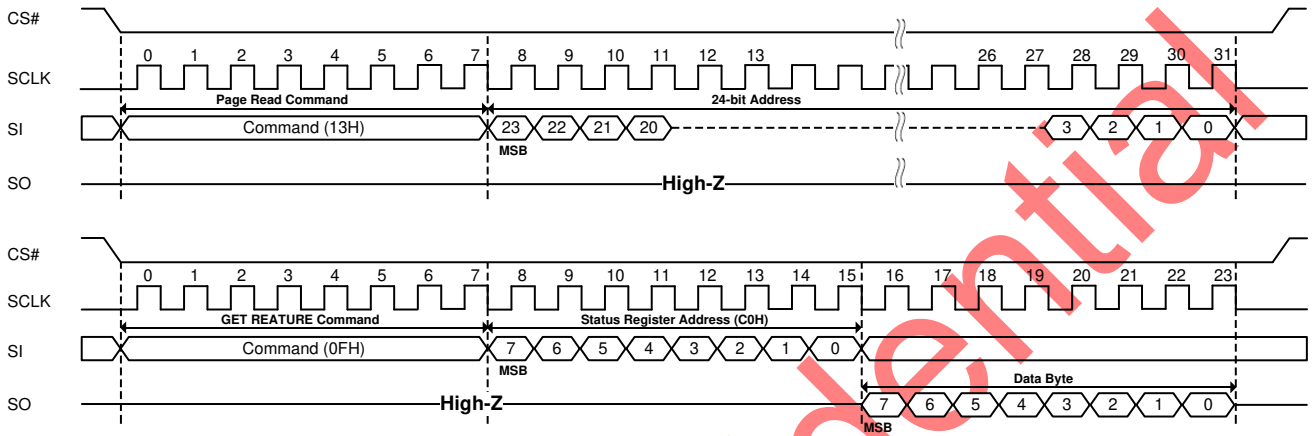


Figure 6-2. Page Read to Cache (13H) Sequence Diagram

6.3 Read from Cache x1 IO (03H/0BH)

The Read from Cache x1 IO (03H/0BH) consists of an OP code followed by 16-bit column address. The column address is composed of wrap bits and column address bits. Refer the Read from Cache x1 IO sequence diagram as follows:

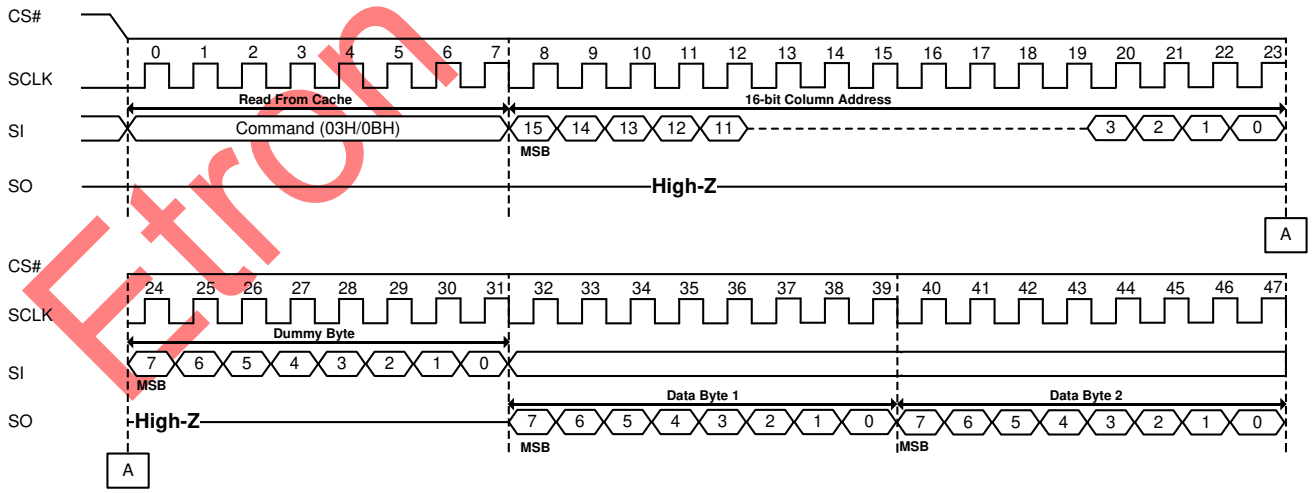


Figure 6-3. Read from Cache x1 IO (03H/0BH) Sequence Diagram

6.4 Read from Cache x2 IO (3BH)

The Read from Cache x2 IO (3BH) command is similar to the Read from Cache x1 IO (03H/0BH) but the command uses two pins to output data. The data output pins include the SI (SIO0) and the SO (SIO1). The Read from Cache x2 IO (3BH) sequence diagram is shown as follows:

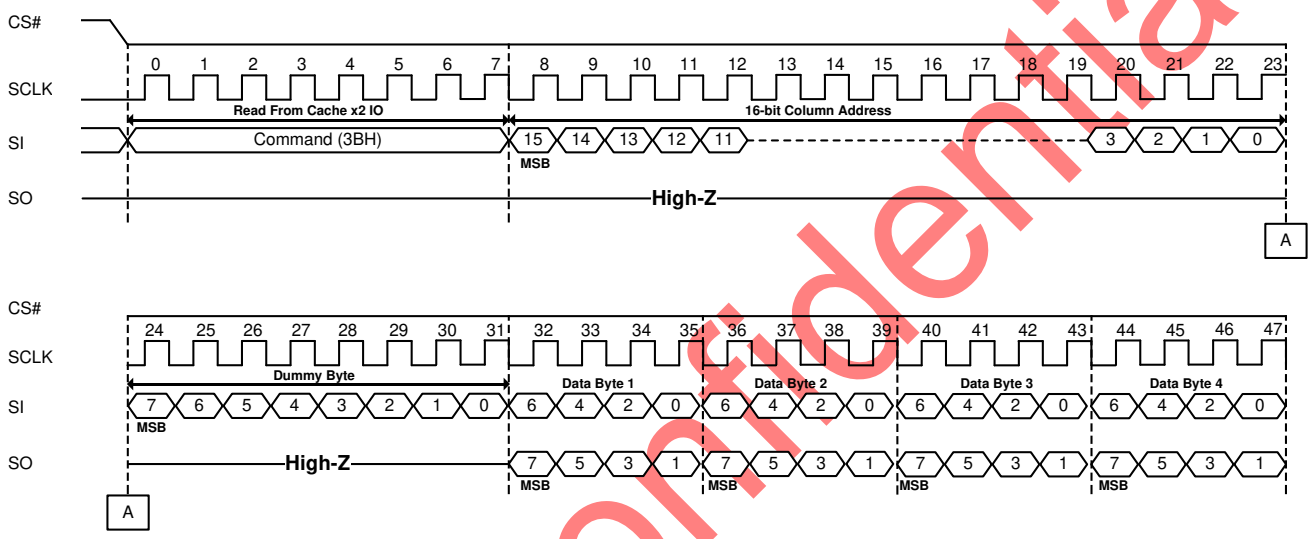


Figure 6-4. Read from Cache x2 IO (3BH) Sequence Diagram

6.5 Read from Cache x4 IO (6BH)

The Read from Cache x4 IO (6BH) command is similar to the Read from Cache x1 IO (03H/0BH) and the Read from Cache x2 IO (3BH) but the command uses four pins to output data. The four pins include the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Read from Cache x4 IO (6BH) sequence diagram is shown as follows:

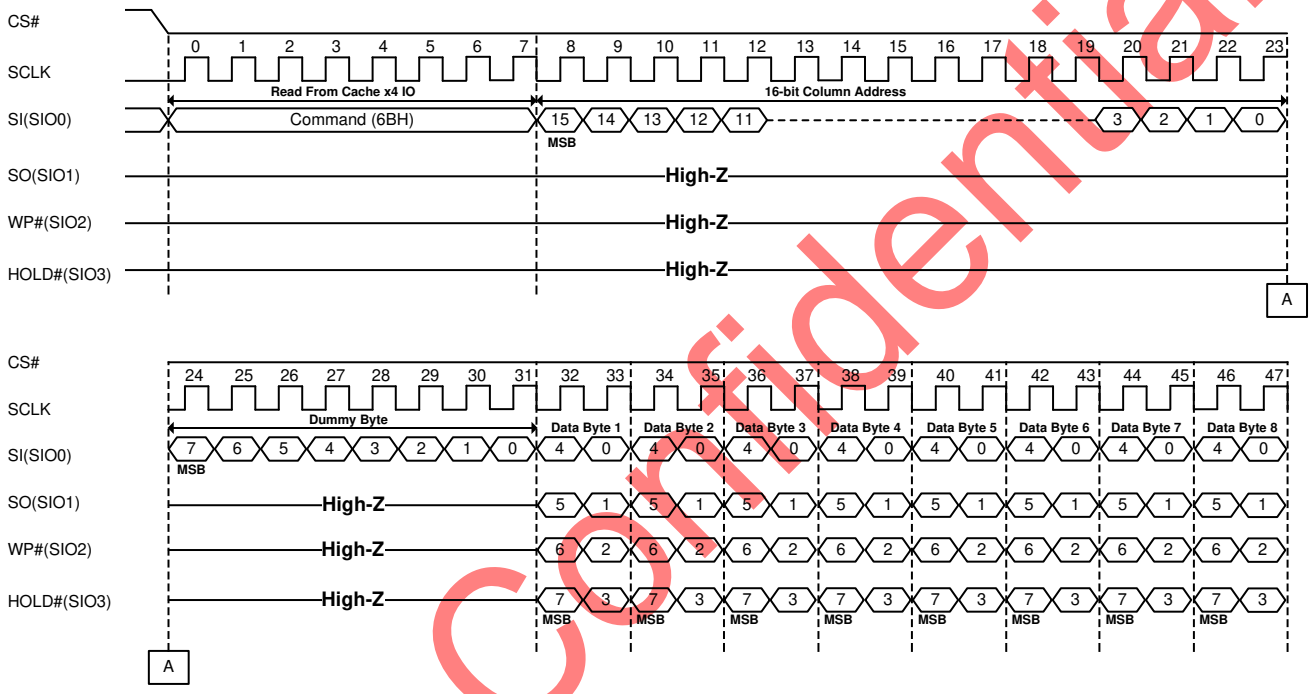


Figure 6-5. Read from Cache x4 IO (6BH) Sequence Diagram

6.6 Read from Cache Dual IO (BBH)

The Read from Cache Dual IO command (BBH) is similar to the Read from Cache x2 IO command (3BH) and uses both of SI (SIO0) and SO (SIO1) as input bin. Each bit in 16-bit column address and the followed dummy byte will be latched in during the falling edge of SCLK, then the cache contents will be shifted out 2-bit in a clock cycle through the SI (SIO0) and the SO (SIO1).

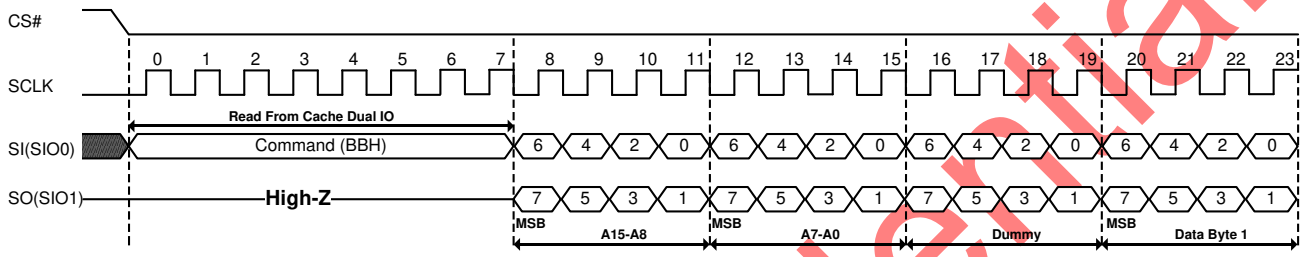


Figure 6-6. Read from Cache Dual IO (BBH) Sequence Diagram

6.7 Read from Cache Quad IO (EBH)

The Read from Cache Quad IO (EBH) command is similar to the Read from Cache x4 IO (6BH) command and has 4 input pins which are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). Each bit in 16-bit column address and the followed dummy byte will be latched in during the raising edge of SCLK through these four input pins, and then the cache contents will be shifted out 4-bit in a clock cycle through SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3) The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the Read from Cache Quad IO (EBH) command .

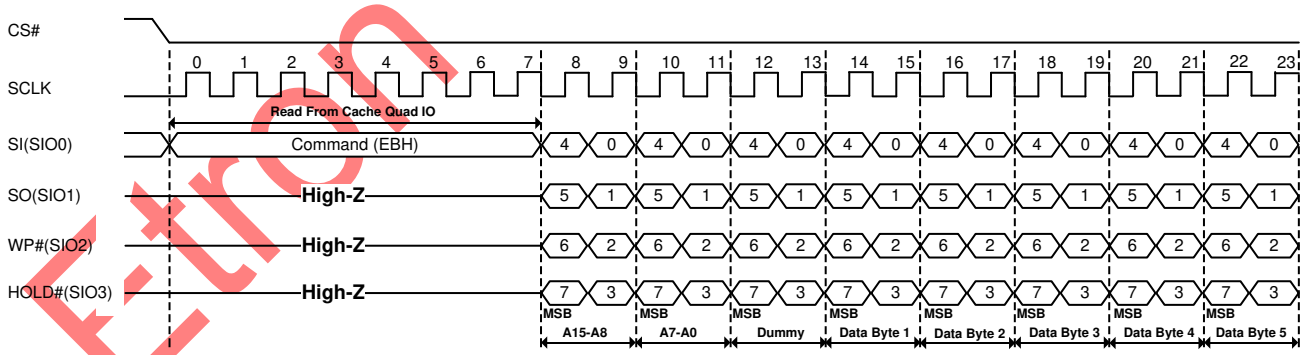


Figure 6-7. Read from Cache Quad (EBH) Sequence Diagram

7 Program Operations

The PAGE PROGRAM sequence transfers the data from the host to NAND flash array through cache memory. The operation sequence programs the first byte to last byte of data within a page. If page size is not enough, those additional bytes will be ignored by the cache memory. The PAGE PROGRAM sequence is as follows:

I. 06H (WRITE ENABLE when WEL bit is 0)
II. PROGRAM LOAD
    - 02H (PROGRAM LOAD) / 32H (PROGRAM LOAD x4)
III. 10H (PROGRAM EXECUTE)
IV. 0FH (GET FEATURE command to read the status)

At first, the WRITE ENABLE (06H) command is used to set the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to issuing a program execute (10h). The PROGRAM LOAD (02H/32H) command is issued then and the PROGRAM LOAD command can only be issued one time in a PAGE PROGRAM sequence. Secondly, the PROGRAM EXECUTE (10H) command is issued to program the data into the page. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE PROGRAM. After finishing the PAGE PROGRAM successfully, the OIP and WEL bit in status register (C0H) will be set to 0.

7.1 Program Load (PL) (02H)

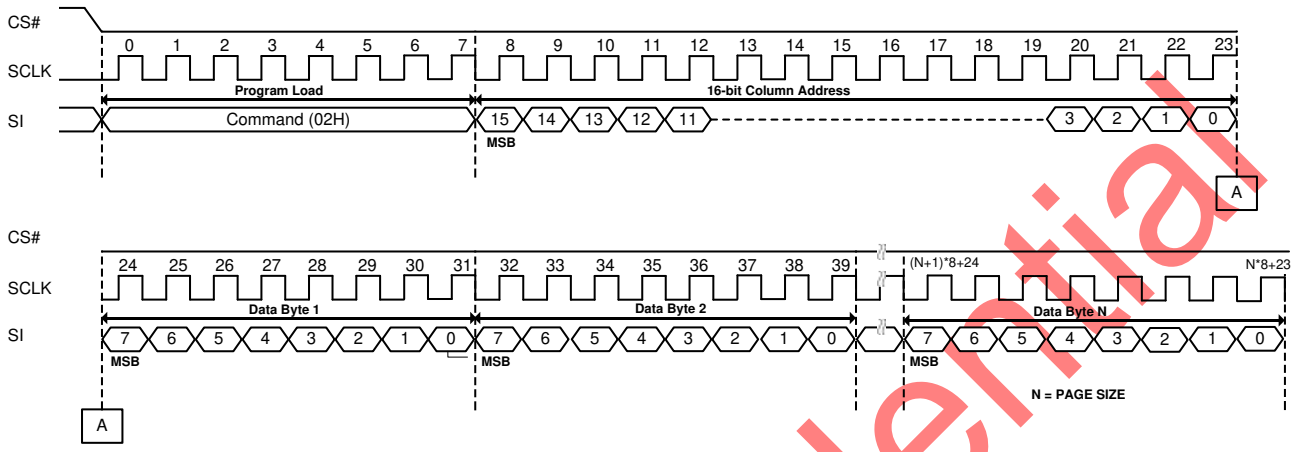


Figure 7-1. Program Load (02H) Sequence Diagram

7.2 Program Load x4 IO (PL x4) (32H)

The PROGRAM LOAD x4 IO (32H) command is similar to the PROGRAM LOAD (02H) command and uses four input pins to transfer data in. The four input pins are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). The Quad Enable bit (QE) of OTP register (B0[0]) must be set to enable the PROGRAM LOAD x4 IO (32H) command. The command sequence is shown as follows:

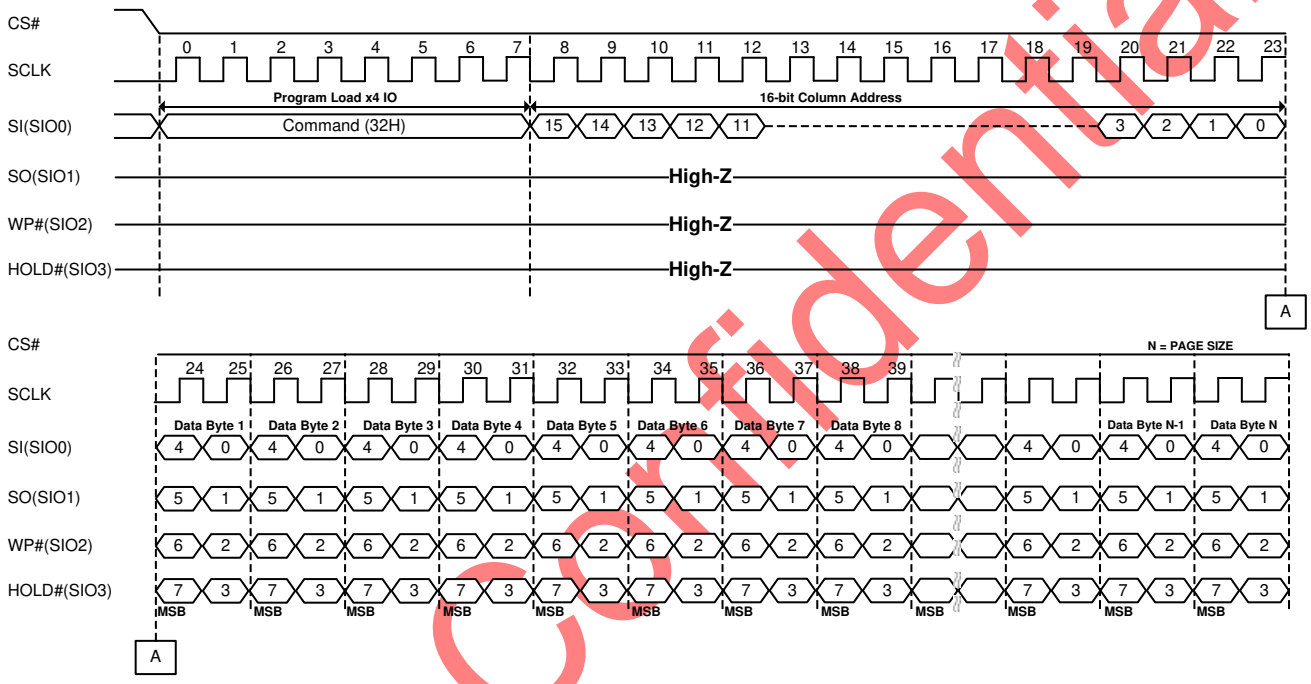


Figure 7-2. Program Load x4 IO (32H) Sequence Diagram

7.3 Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) command must be issued after the data is loaded and the WEL bit is set to HIGH. The PROGRAM EXECUTE (10H) command will transfer data from the cache to the main array. The PROGRAM EXECUTE (10H) consists of an 8-bit Op code, followed by a 24-bit address which including dummy bits and page/block address. This operation needs to wait the busy time. The OIP bit in status register (C0H) will be HIGH until controller finishes the program. The P_FAIL bit in status register (C0H) will be set HIGH if program fail.

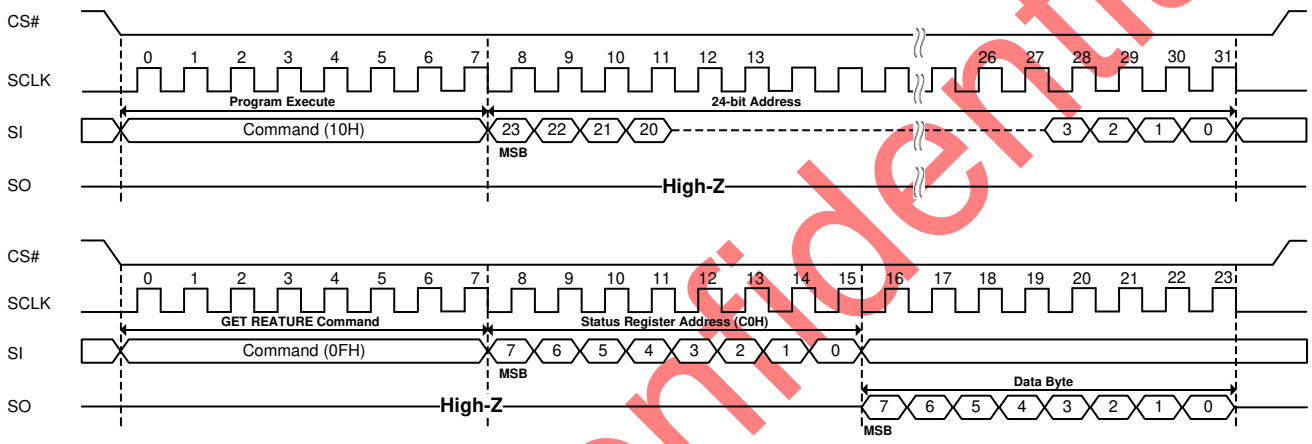


Figure 7-3. Program Execute (10H) Sequence Diagram

8 Internal Data Move

The Internal Data Move sequence programs or replaces data in a page with existing data. The Internal Data Move operation sequence is as follows:

I. 13H (Page Read to cache)
II. 0FH (GET FEATURE command to read the status).
III. Optional 84H/C4H/34H/72H **(PROGRAM LOAD RANDOM DATA. The command of Program load random data can be operated several times in this step.)
IV. 06H (WRITE ENABLE)
V. 10H (PROGRAM EXECUTE)
VI. 0FH (GET FEATURE command to read the status)

- 84H/C4H/34H/72H commands are only available in Internal Data Move operation.

8.1 Program Load Random Data (84H)

Program Load Random Data (84H) command consists of an OP code, followed by 16 bit column address which includes dummy bits and column address bits. This command can only be used in Internal Data Move sequence.

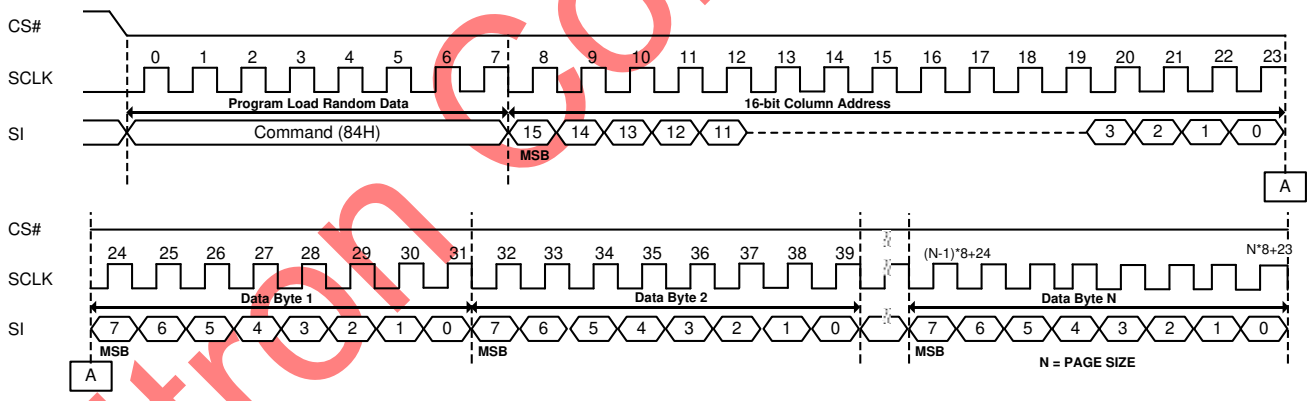


Figure 8-1. Program Load Random Data (84H) Sequence Diagram

8.2 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 (C4H/34H) command is similar to the Program Load Random Data Command (84H) and has four input pins. The four input pins are SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable bit needs to be set before the Program Load Random Data x4 command be used. The command is only available during the Internal Data Move sequence.

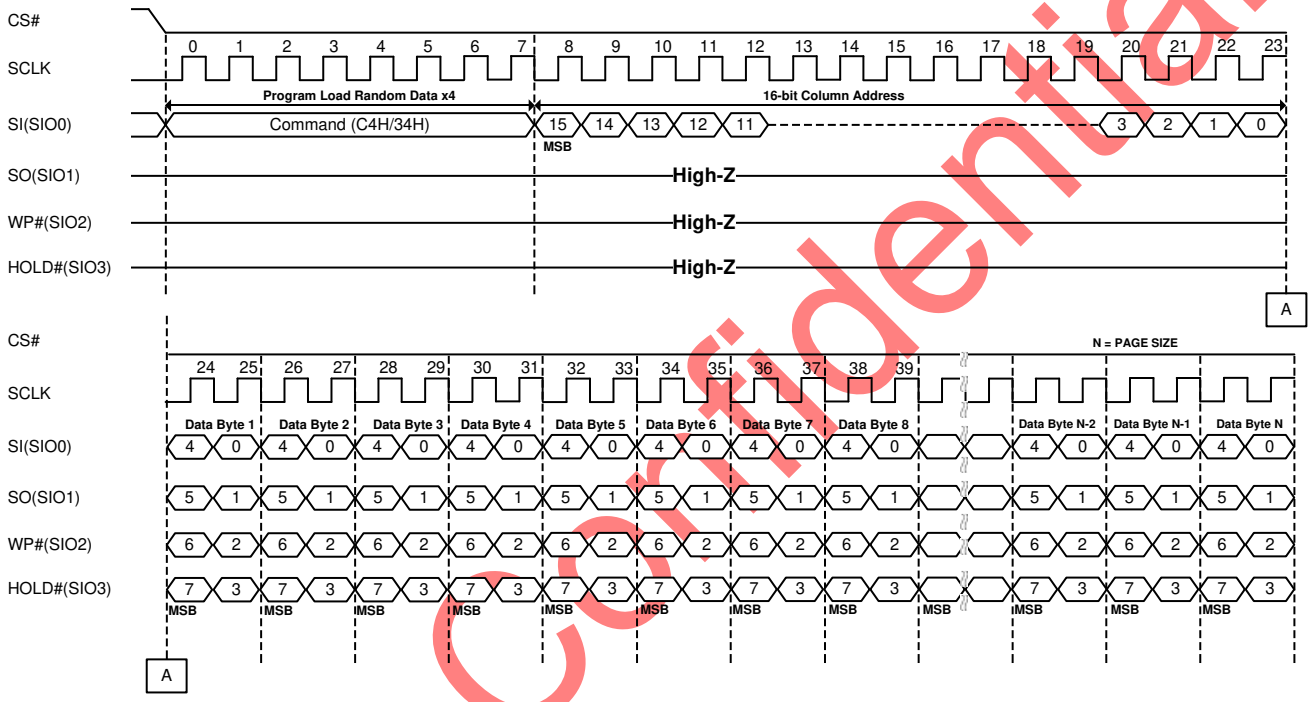


Figure 8-2. Program Load Random Data x4 (C4H/34H) Sequence Diagram

8.3 Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO (72H) is similar to the Program Load Random Data x4 (C4H/34H) command and has 4 input pins: SI(SIO0), SO(SIO1), WP#(SIO2) and HOLD#(SIO3). The Quad Enable (QE) bit in feature register (B0[0]) needs to be set to 1 for the Program Load Random Data Quad IO command. This command is only available during Internal Data Move sequence.

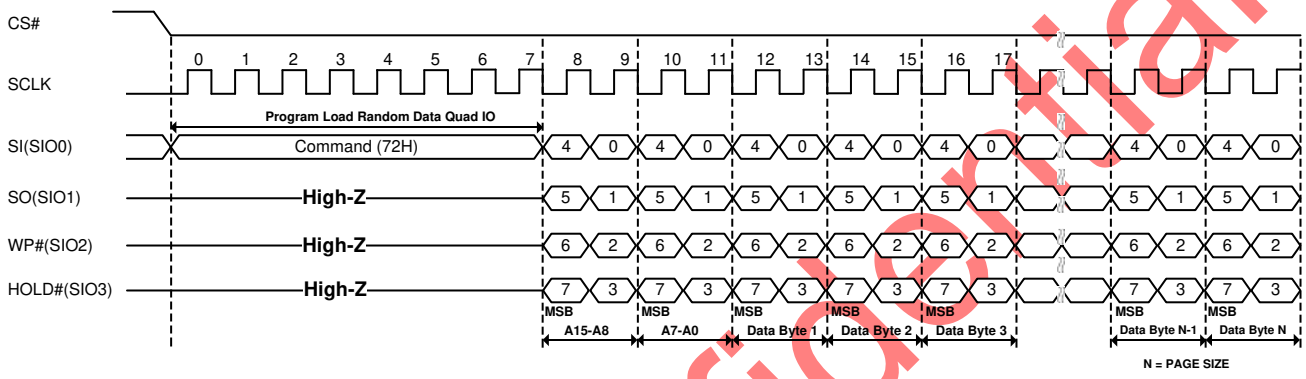


Figure 8-3. Program Load Random Data Quad IO (72H) Sequence Diagram

9 Erase Operation- Block Erase (D8H)

The BLOCK ERASE (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as follows:

I. 06H (WRITE ENABLE command)
II. D8H (BLOCK ERASE command)
III. 0FH (GET FEATURE command to read the status register)

Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically). Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit in status register can reflect whether the block be erased successfully or not.

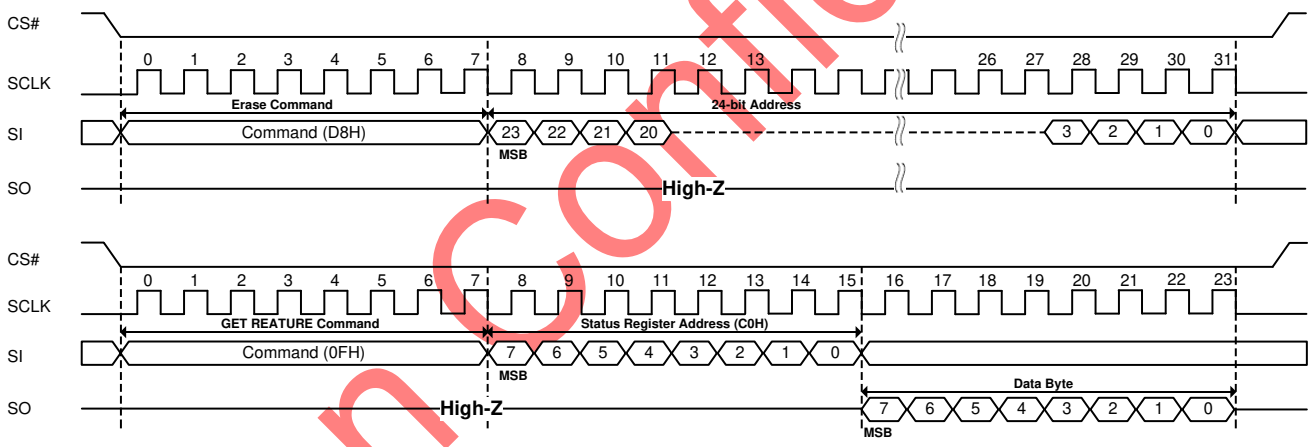


Figure 9-1. Block Erase (D8H) Sequence Diagram

10 Reset Operation - Reset (FFH)

The RESET (FFH) command stops all operations. For example, the RESET command can stop the previous operation and the pending operations during a cache program or a cache read command.

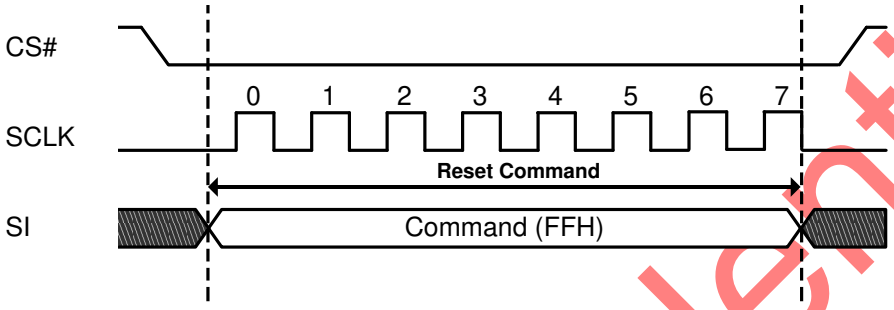


Figure 10-1. Reset (FFH) Sequence Diagram

11 One-Time Programmable (OTP) Function

11.1 OTP Definition

The serial device offers a protected, OTP area. 64 full pages are available on the device. Users can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

Table 11-1. OTP State

OTP_PRT	OTP_EN	State
X	0	Normal operation. Cannot access the OTP region.
0	1	Access OTP region. PAGE READ and PAGE PROGRAM are allowed.
1	1	The OTP_PRT has two situations when the device power on, 1. OTP_PRT is 0 when the device power on: User can use SET FEATURE command to set the OTP_PRT and OTP_EN bit to 1, and then issue PROGRAM EXECUTE (10H) to lock OTP region. Once the OTP region was locked, the OTP_PRT will permanently be 1. 2. OTP_PRT is 1 when the device power on: user can only read the OTP region data.

Table 11-2. OTP Page Definition

Page Address	Page Name	Description	Data Length	Notes
00h	Parameter Page OTP Page [0]	Factory Programmed , Read Only	256 Bytes * 4	
01h ~ 3Fh	OTP Page [1:63]	Read & Program when OTP_PRT=0 Read Only when OTP_PRT=1	2,112 Bytes	

How to access to OTP region:

1. Issue the GET FEATUTE command (0FH).
2. Set Feature bit OTP_EN.
3. Issue the PAGE READ command or PAGE PROGRAM command. The PAGE PROGRAM command can be allowed only when OTP_PRT is 0. The PAGE READ command will automatically be ignored if OTP_PRT is 1.

How to protect OTP region:

Only when the following steps are completed, the OTP_PRT will be set to 1.

1. Issue the SET FEATURE (1FH) command.
2. Set feature bit OTP_EN and OTP_PRT.
3. 06H (WRITE ENABLE)
4. Issue the PROGRAM EXECUTE (10H) command.
5. Issue the GET FEATURE (0FH) command to wait the device goes to ready state from busy.

11.2 Parameter Page Definition

Table 11-3. Parameter Page Data Structure

Parameter Page Data Structure			
Address (DEC)	**Description**	**Display**	**VALUE**
0~3	Parameter page signature	ASCII	4Fh, 4Eh, 46h, 49h
4~5	ONFI Revision number	HEX	00h, 00h
6~7	Features supported	HEX	00h, 00h
8~9	Optional commands supported	HEX	06h, 00h
10~31	Reserved (0)	HEX	ALL 00h
32~43	Device manufacturer (12 Bytes ASCII characters)	ASCII	45h, 74h, 72h, 6Fh, 6Eh, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44~63	Device model (20Bytes ASCII characters)		
	EM73C044VCF-H	ASCII	45h, 4Dh, 37h, 33h, 43h, 30h, 34h, 34h, 56h, 43h, 46h, 2Dh, 48h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	HEX	D5h
65~66	Date code	HEX	00h, 00h
67~79	Reserved (0)	HEX	ALL 00h
80~83	Number of data bytes per page	HEX	00h, 08h, 00h, 00h (Page size = 2048 bytes)
84~85	Number of spare bytes per page	HEX	40h, 00h (Spare 64)
86~89	Number of data bytes per partial page	HEX	00h, 00h, 00h, 00h
90~91	Number of spare bytes per partial page	HEX	00h, 00h
92~95	Number of pages per block	HEX	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit (LUN)	HEX	00h, 04h, 00h, 00h (Block=1024)
100	Number of logical units (LUNs)	HEX	01h
101	Number of address cycles	HEX	00h
102	Number of bits per cell	HEX	01h
103~104	Bad blocks maximum per LUN	HEX	14h, 00h (Bad blocks maximum per LUN = 20)
105~106	Block endurance	HEX	06h, 04h
107	Guaranteed valid blocks at beginning of target	HEX	01h
108~109	Block endurance for guaranteed valid blocks	HEX	00h, 00h
110	Number of programs per page	HEX	01h
111	Partial programming attributes	HEX	00h
112	Number of bits ECC correctability	HEX	04h 08h
113	Number of interleaved address bits	HEX	00h
114	Interleaved operation attributes	HEX	00h
115~127	Reserved (0)	HEX	ALL 00h
128	I/O pin capacitance	HEX	00h
129~130	Timing mode support	HEX	00h, 00h
131~132	Program cache timing mode support	HEX	00h, 00h
133~134	tPROG Maximum page program time (us)	HEX	BCh, 02h
135~136	tBERS Maximum block erase time (us)	HEX	B8h, 0Bh
137~138	tR Maximum page read time (us)	HEX	46h, 00h (Page size = 2048 bytes)
139~140	tCCS Minimum change column setup time (ns)	HEX	00h, 00h
141~163	Reserved (0)	HEX	ALL 00h
164~165	Vendor specific Revision number	HEX	00h, 00h
166~253	Vendor specific	HEX	ALL 00h
254~255	Integrity CRC	HEX	(SEE THE NOTES 1)
256~511	Value of Address 0~255	HEX	Same as address 0~255
512~767	Value of Address 0~255	HEX	Same as address 0~255
768~1023	Value of Address 0~255	HEX	Same as address 0~255
1024+	Additional redundant parameter pages	HEX	ALL FFh

Note 1: (Source：ONFI_1.0_GOLD)

The CRC shall be calculated using the following 16-bit generator polynomial：$G(X) = X^{16} + X^{15} + X^2 + 1$

The CRC calculation covers all of data between byte 0 and byte 253 of the parameter page inclusive.

This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins.

12 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE commands. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1 and BP2 are set to 1, INV, CMP and BRWD are set to 0. Some block operations relating to the block protection are listed as follows:

- SET FEATURE command must be issued to alter the state of protection feature bit.
- When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set.
- When a PROGRAM/ERASE command is issued to a locked block, status bit OIP in status register (C0H) remains 0. The status register (C0H) will return 08H when a PROGRAM command is issued to program a locked block. The status register (C0H) will return 04H when an ERASE command is issued to erase a locked block.
- When WP# is not LOW, user can issue SET FEATURE command and use the protection register (A0H) and the block protect bits table below to alter the protection rows.

Table 12-1. Block Protection Bits Table

CMP	INV	BP2	BP1	BP0	Protect Rows
X	X	0	0	0	All unlocked
0	0	0	0	1	Upper 1/64 locked
0	0	0	1	0	Upper 1/32 locked
0	0	0	1	1	Upper 1/16 locked
0	0	1	0	0	Upper 1/8 locked
0	0	1	0	1	Upper 1/4 locked
0	0	1	1	0	Upper 1/2 locked
X	X	1	1	1	All locked (Default)
0	1	0	0	1	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	0	1	1	Lower 1/16 locked
0	1	1	0	0	Lower 1/8 locked
0	1	1	0	1	Lower 1/4 locked
0	1	1	1	0	Lower 1/2 locked
1	0	0	0	1	Lower 63/64 locked
1	0	0	1	0	Lower 31/32 locked
1	0	0	1	1	Lower 15/16 locked
1	0	1	0	0	Lower 7/8 locked
1	0	1	0	1	Lower 3/4 locked
1	0	1	1	0	Block 0
1	1	0	0	1	Upper 63/64 locked
1	1	0	1	0	Upper 31/32 locked
1	1	0	1	1	Upper 15/16 locked
1	1	1	0	0	Upper 7/8 locked
1	1	1	0	1	Upper 3/4 locked
1	1	1	1	0	Block 0

13 Status Register

The content of status register can be read by issuing the GET FEATURE (0FH) command, followed by the status register address C0H. The meaning of each bit in status register is listed as follows:

Table 13-1. Status Register Bit Description

Bit	Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred. It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command.
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred. It will also be set if the user attempts to erase a locked region. This bit is cleared at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates that the current status of the write enable latch(WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS1, ECCS0	ECC Status	This bit provides ECC status as follows: 00b = No bit errors were detected 01b = bit error was detected and corrected 10b = bit error was detected and not corrected 11b = bit error was detected and corrected, error bit number = ECC max which is according to extended register. ECCS is set to 00b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid operation. After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.

Notes: The ECC status of register C0H will be cleared when ECC is disabled.

14 Block Management

A NAND Flash device is specified to have a minimum number of valid blocks of the total available blocks per die, which means the devices may have blocks that are invalid when shipped from the factory. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark but the first spare area location in each bad block is guaranteed to contain the bad-block mark. System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device.

Table 14-1. Valid Block Information

Total available blocks	1024
Minimum number of valid blocks	1004
The bad block mark	All 00h

15 Power-On Process

When the chip reached the power on level, the internal power on reset signal will be released. The device can response host commands after tPUW (Max 4ms). The host should issue GET FEATURE (0Fh). The device will use the OIP bit in the status register to inform the host that initialization in power-on process is completed. Setting OIP bit to1 indicates that the device is still initializing. Setting the OIP bit to 0 indicates that the power on process is finished. If OIP bit is 1, the host will repeatedly issues GET FEATURE (0Fh) command to monitor the power-on process until the OIP bit is set to 0.

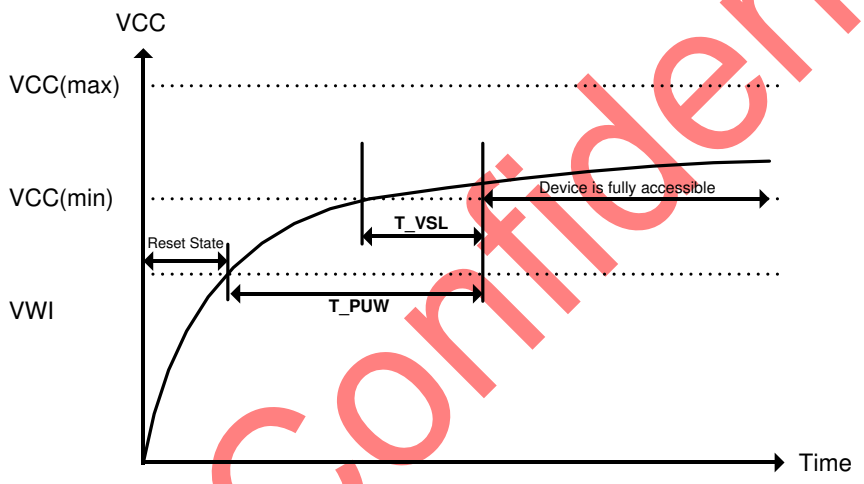


Figure 15-1. Power-On Process

Table 15-1. Power-On Process Parameters

Parameters		Symbol	Min	Typical	Max	Unit
VCC (min) to CS# Low		tVSL	50	-	500	us
Time Delay Before Read/Write Instruction		tPUW	-	3	4	ms
Write Inhibit Threshold Voltage	3.3V	vWI	2.5	-	-	V

16 Electrical Characteristics

Table 16-1. SPI NAND DC Characteristics

Parameters	Symbol	Min	Typical	Max	Unit
SPI Supply Voltage	VCC	3.0	3.3	3.6	V
VCC standby current	ISB	---	---	120	uA
VCC active current (sequential read)	ICC1	---	20	30	mA
VCC active current (Program)	ICC2	---	20	30	mA
VCC active current (Erase)	ICC3	---	25	30	mA
Input low level	V_IL	-0.3	---	0.2 x VCC	V
Input high level	V_IH	0.8 x VCC	---	VCC + 0.3	V
Output High Voltage	V_OH	VCC - 0.2	---	---	V
Output Low Voltage	V_OL	---	---	0.2	V
Input Leakage Current	I_LI	---	---	±10	uA
Output Leakage Current	I_LO	---	---	±10	uA

Table 16-2. Capacitance Characteristics

Parameters	Symbol	Min	Typical	Max	Unit	Condition
Input Capacitance	CIN	-	-	3.5	pF	VIN=0V
Output Capacitance	COUT	-	-	3.5	pF	VOUT=0V
Load Capacitance	CL		10		pF	
Input Rise and Fail time		-	-	5	ns	

Table 16-3. 3.3V AC Time Characteristics (T_A = -40 ~ 85°C, C_L = 10pF)

Parameters	Symbol	Min	Typical	Max	Unit
Clock Frequency	FC	-	-	120	MHz
Page Program Time	tPROG	-	600	700	us
Clock High Time	tCLH	4.16	-	-	ns
Clock Low Time	tCLL	4.16	-	-	ns
Command deselect Time	tSHSL	20			ns
CS# Setup Time	tSLCH	4	-	-	ns
CS# Hold Time	tCHSL	4	-	-	ns
Data In Setup Time	tDVCH	2	-	-	ns
Data In Hold Time	tCHDX	4	-	-	ns
Output Hold time	tCLQX	2.7	-	-	ns
Clock to output Valid	tCLQV	-	-	7.5	ns
CS# High to Output Invalid	tSHQZ	-	-	4	ns
CS# Active Hold time relative to SCLK	tCHSH	4	-	-	ns
CS# Not Active Setup time relative to SCLK	tSHCH	4	-	-	ns
Hold# hold time relative to SCLK	tCH	5	-	-	ns
Hold# non-active hold time relative to SCLK	tCD	5	-	-	ns
Hold# setup time relative to SCLK	tHD	5	-	-	ns
Hold# non-active setup time relative to SCLK	tHC	5	-	-	ns
Hold# to output High-Z	tHZ	-	-	10	ns
Hold# to output Low-Z	tLZ	-	-	10	ns
WP# setup time	tWPS	20	-	-	ns
WP# hold time	tWPH	100	-	-	ns

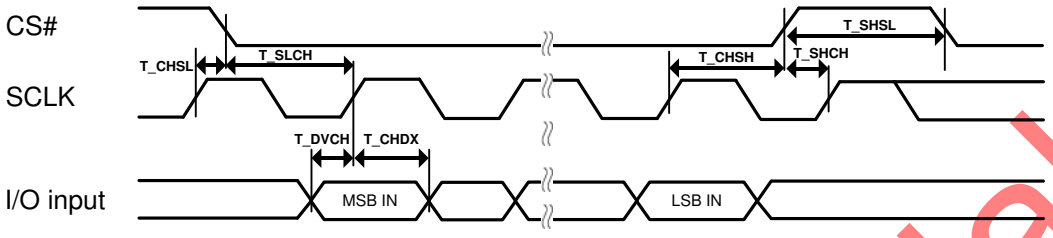


Figure 16-1. Serial Input Timing

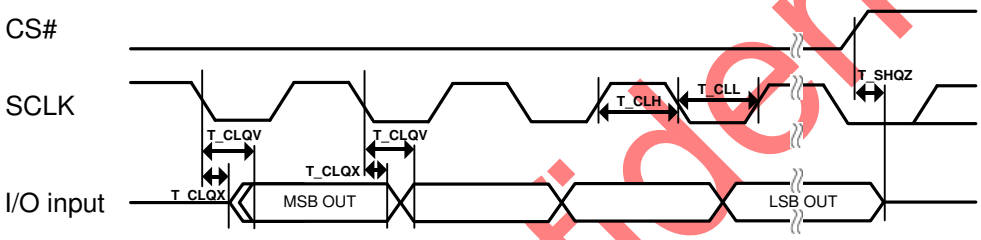


Figure 16-2. Serial Output Timing

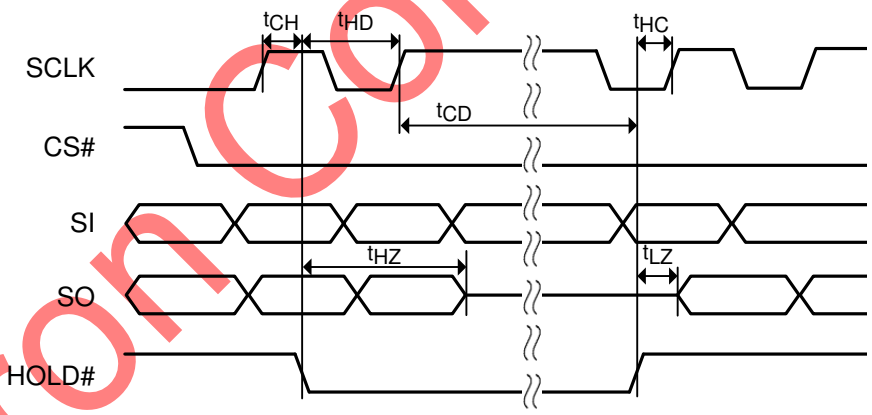


Figure 16-3. Hold# Timing

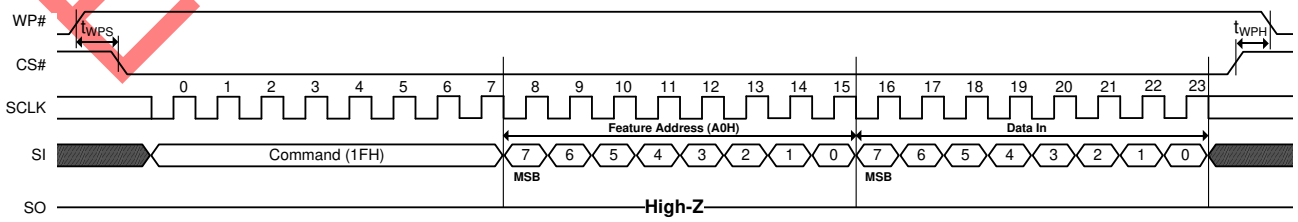


Figure 16-4. WP# Timing

17 Package Outline Information

Table 17-1. LGA (8 x 6 x 0.8mm) Dimension Table

Symbol	Dimension (MM)			Dimension (MIL)		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	27.559	29.528	31.496
(A1)	0.500	0.550	0.600	19.685	21.654	23.622
A2	-	0.210	-	-	8.268	-
b	0.350	0.400	0.480	13.780	15.748	18.898
D	7.900	8.000	8.100	311.023	314.960	318.897
E	5.900	6.000	6.100	232.283	236.220	240.157
e		1.270			50.000	
L	0.450	0.500	0.550	17.717	19.685	21.654

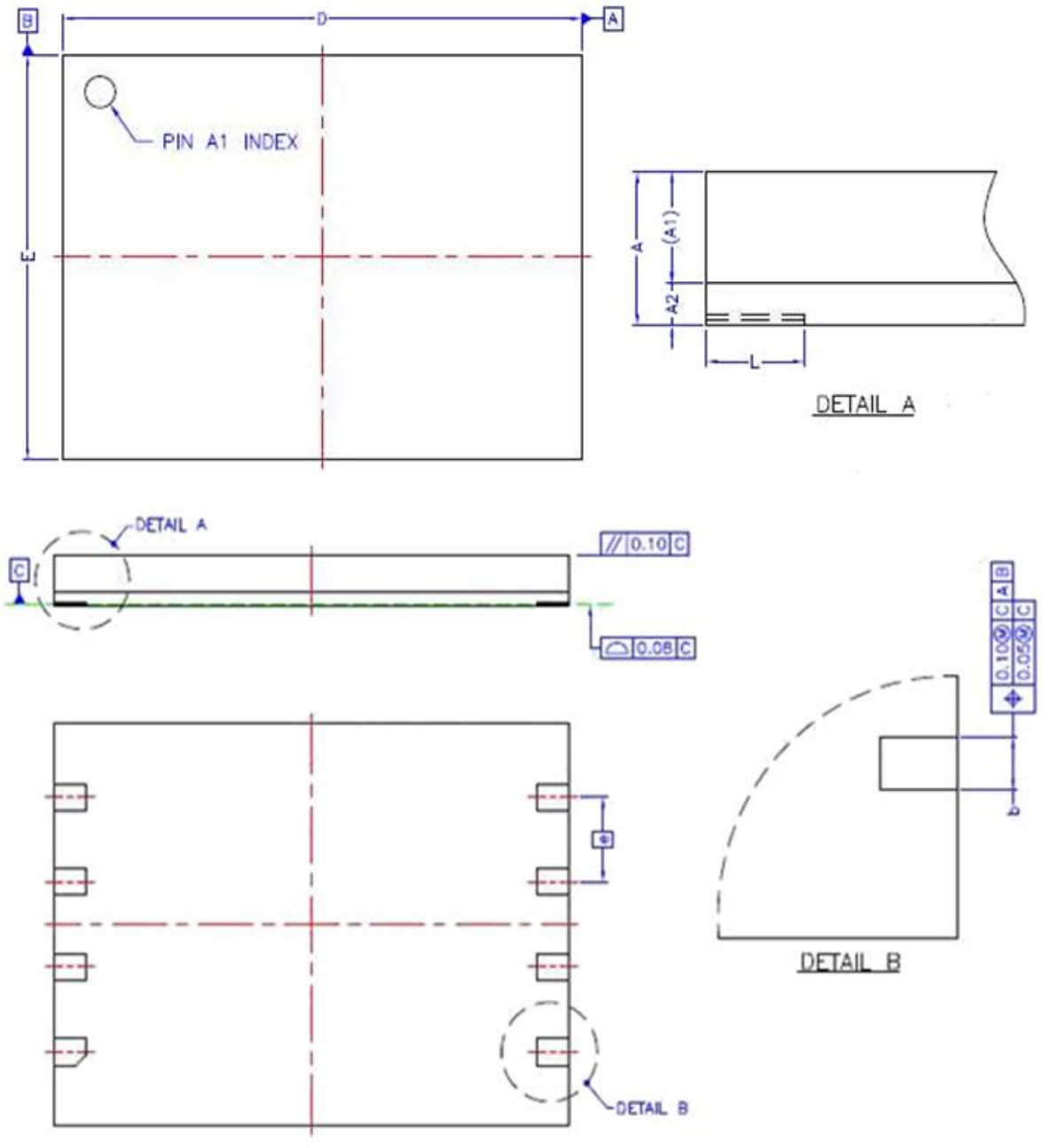


Figure 17-1. LGA (8 x 6 x 0.8mm) Package Outline Drawing Information