8M x 32 Mobile LPDDR2 Synchronous DRAM (SDRAM)

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Features

- JEDEC standard Compliant
- Fast clock rate: 333/400/533 MHz
- Power supplies:
  - V_{DD1} = 1.8V (1.7V~1.95V)
  - V_{DD2} = 1.2V (1.14V~1.3V)
  - V_{DDCA}/V_{DDQ} = 1.2V (1.14V~1.3V)
- Operating Temperature: T_C = -25 ~ 85°C
- Supports JEDEC clock jitter specification
- 4n-bit prefetch architecture
- 4 internal banks for concurrent operation
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- Multiplexed, double data rate, command/address inputs; commands entered on each CK/CK# edge
- Programmable Mode Registers
  - Read and Write latencies (RL/WL)
  - Burst length: 4, 8, or 16
  - Output drive strength (DS)
  - PASR (Partial Array Self Refresh)
- Auto TCSR (Temperature Compensated Self Refresh)
- Auto Refresh and Self Refresh
- Deep power-down
- Clock Stop capability
- 4096 refresh cycles / 32ms
- Interface: HSUL_12
- Package: 168-ball 12 x 12 x 0.9mm (max) FBGA
  - Pb Free and Halogen Free

Overview

The EM6KA32H LPDDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a 4 banks of 2,097,152 words by 32 bits memory device. The devices use double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2 also use double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Table 1. Ordering Information

Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6KA32HVIA-18H	533MHz	1066Mbps/pin	V_{DD1} 1.8V, V_{DDCA}/V_{DDQ}/V_{DD2} 1.2V	FBGA
EM6KA32HVIA-25H	400MHz	800Mbps/pin	V_{DD1} 1.8V, V_{DDCA}/V_{DDQ}/V_{DD2} 1.2V	FBGA
EM6KA32HVIA-3H	333MHz	667Mbps/pin	V_{DD1} 1.8V, V_{DDCA}/V_{DDQ}/V_{DD2} 1.2V	FBGA

VI: indicates 12 x 12 x 0.9mm FBGA Package
A(11^{th} digit): indicates Generation Code
H(Last digit): indicates Pb Free and Halogen Free

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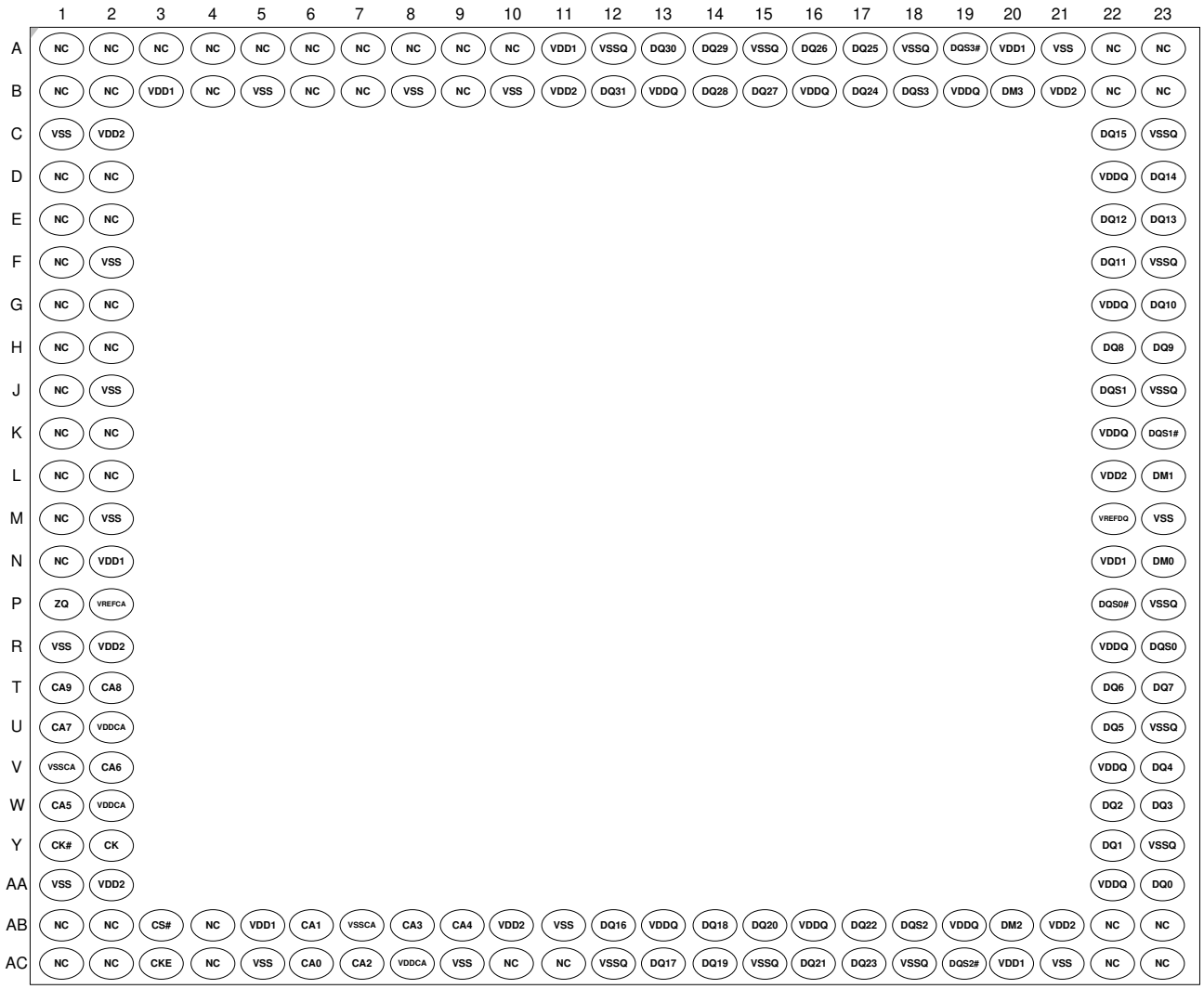
Ball Assignment (FBGA Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3#	VDD1	VSS	NC	NC
B	NC	NC	VDD1	NC	VSS	NC	NC	VSS	NC	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3	VDDQ	DM3	VDD2	NC	NC
C	VSS	VDD2																				DQ15	VSSQ
D	NC	NC																				VDDQ	DQ14
E	NC	NC																				DQ12	DQ13
F	NC	VSS																				DQ11	VSSQ
G	NC	NC																				VDDQ	DQ10
H	NC	NC																				DQ8	DQ9
J	NC	VSS																				DQS1	VSSQ
K	NC	NC																				VDDQ	DQS1#
L	NC	NC																				VDD2	DM1
M	NC	VSS																				VREFDQ	VSS
N	NC	VDD1																				VDD1	DM0
P	ZQ	VREFCA																				DQS0#	VSSQ
R	VSS	VDD2																				VDDQ	DQS0
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK#	CK																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	NC	NC	CS#	NC	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2	VDDQ	DM2	VDD2	NC	NC
AC	NC	NC	CKE	NC	VSS	CA0	CA2	VDDCA	VSS	NC	NC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2#	VDD1	VSS	NC	NC

Figure 1. 168-Ball FBGA Package 12 x 12 x 0.9mm(max)

Functional Block Diagram

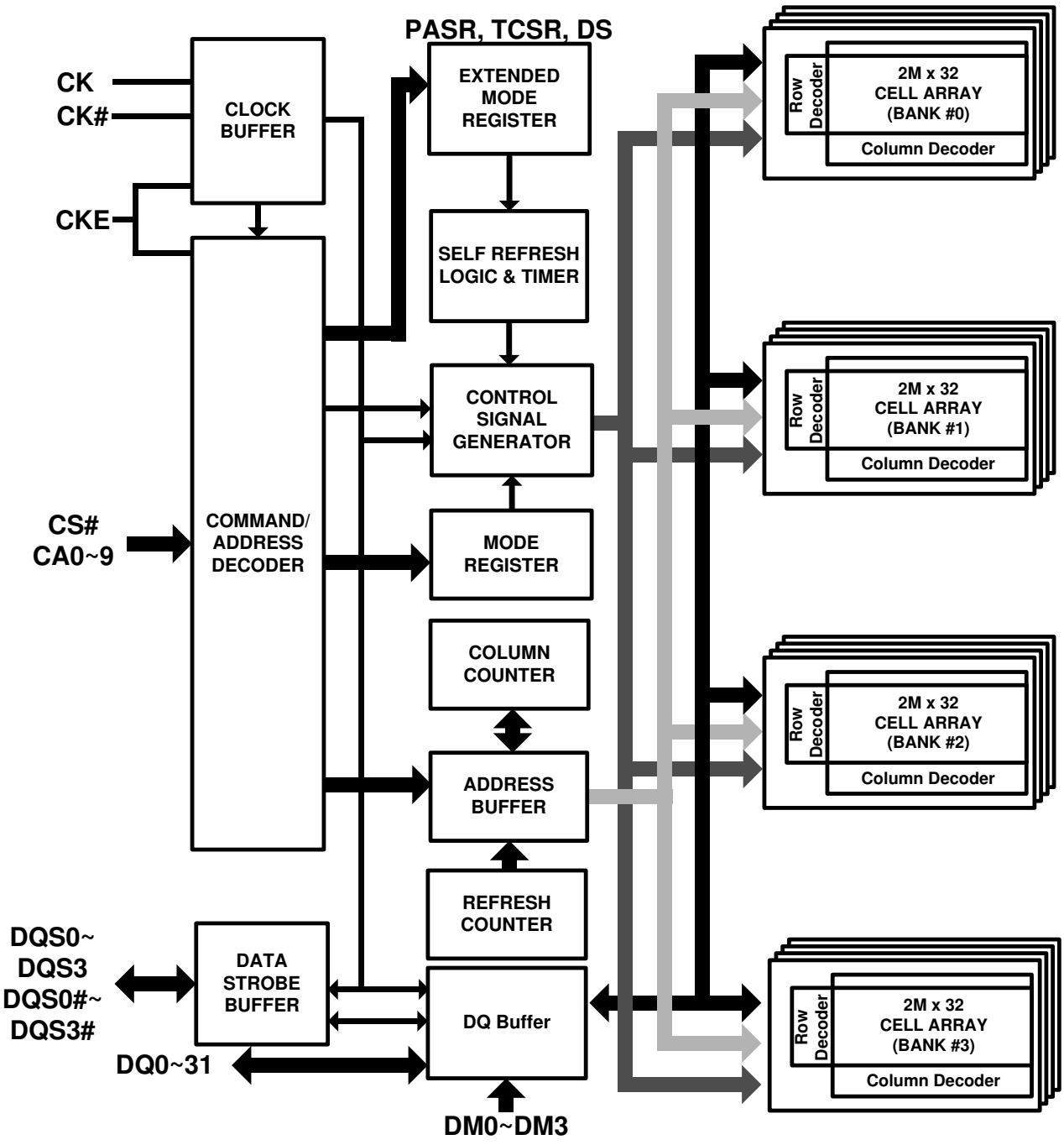
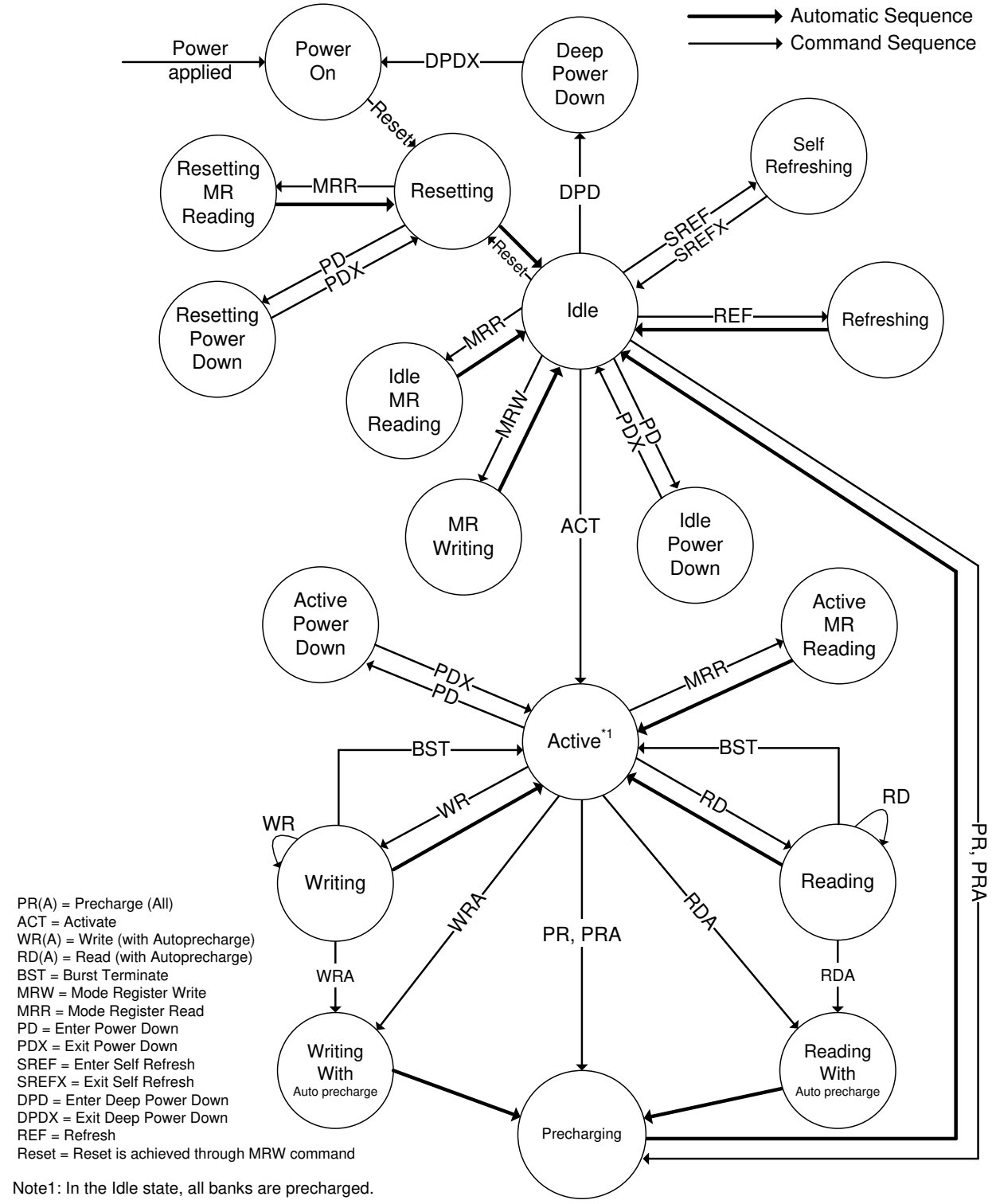


Figure 2. Block Diagram

Simplified State Diagram



Note1: In the Idle state, all banks are precharged.

Figure 3. State Diagram

Pad Descriptions

Table 2. Pad Details

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS# and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS#	Input	**Chip Select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
CA0 – CA9	Input	**Command/Address Inputs:** Provide the command and address inputs according to the command truth table.
DQ0 – DQ31	Input / Output	**Data input/output:** Bidirectional data bus.
DQS0 – DQS3 DQS0# – DQS3#	Input / Output	**Data Strobe:** The data strobe is bi-directional (used for read and write data) and differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. DQS0 and DQS0# correspond to the data on DQ0 - DQ7. DQS1 and DQS1# correspond to the data on DQ8 - DQ15. DQS2 and DQS2# correspond to the data on DQ16 - DQ23. DQS3 and DQS3# correspond to the data on DQ24 - DQ31.
DM0 – DM3	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS#) DM0 is the input data mask signal for the data on DQ0 - 7. DM1 is the input data mask signal for the data on DQ8 - 15. DM2 is the input data mask signal for the data on DQ16 - DQ23. DM3 is the input data mask signal for the data on DQ24 - DQ31.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS#, CK and CK# input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for data input/output buffers.
V_{REFCA}	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS**#**, CK and CK**#** input buffers.
V_{REFDQ}	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{SSQ}	Supply	**I/O Ground:** Ground for data input/output buffers.
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**
NC	-	**No Connect:** Not internal connection.

Truth Tables

Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 3. Command Truth Table

Command	Command Pins			CA Pins										CK Edge
	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_{n-1}	CK_n												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X	X	X	X	X	X	X	X	↓
Refresh (All bank)	H	H	L	L	L	H	H	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter Self Refresh	H	L	L	L	L	H	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	X	↑
			X	R0	R1	R2	R3	R4	R5	R6	R7	X	X	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP[3]	C3	C4	C5	C6	C7	X	X	X	X	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP[3]	C3	C4	C5	C6	C7	X	X	X	X	↓
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
BST	H	H	L	H	H	L	L	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter DPD	H	L	L	H	H	L	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
NOP	H	H	L	H	H	H	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
NOP	H	H	H	X	X	X	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X	X	X	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter Power Down	H	L	H	X	X	X	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
Exit PD, SREF, DPD	L	H	H	X	X	X	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓

Notes:

1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses (BA) determine which bank will be operated upon.
3. AP HIGH during a Read or Write command indicates that an auto precharge will occur to the bank associated with the Read or Write command.
4. “X” indicates a “Don’t Care” state, with a defined logic level, either HIGH “H” or LOW “L”.

5. Self refresh exit and DPD exit are asynchronous.
6. V_{REF} must be between 0 and V_{DDQ} during self refresh and DPD operation.
7. CAxr refers to command/address bit “X” on the rising edge of clock.
8. CAxf refers to command/address bit “X” on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.
11. AB HIGH during a Precharge command indicates that an all-bank precharge will occur. In this case, bank address is "Don't Care".

Table 4. CKE Truth Table

Notes 1 – 2 apply to all parameters and conditions

Current State[*3]	CKEn-1[*4]	CKEn[*4]	CS#[*5]	Command n[*6]	Operation n[*6]	Device Next State	Note
Active Power-Down	L	L	X	X	Maintain Active Power-Down	Active Power-Down	
	L	H	H	NOP	Exit Active Power-Down	Active	7
Idle Power-Down	L	L	X	X	Maintain Idle Power-Down	Idle Power-Down	
	L	H	H	NOP	Exit Idle Power-Down	Idle	7
Resetting Power-Down	L	L	X	X	Maintain Resetting Power-Down	Resetting Power-Down	
	L	H	H	NOP	Exit Resetting Power-Down	Idle or Resetting	7, 10
Deep Power-Down	L	L	X	X	Maintain Deep Power-Down	Deep Power-Down	
	L	H	H	NOP	Exit Deep Power-Down	Power-On	9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank Active	H	L	H	NOP	Enter Active Power-Down	Active Power-Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power-Down	Idle Power-Down	11
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	11
	H	L	L	Deep Power-Down	Enter Deep Power-Down	Deep Power-Down	11
Resetting	H	L	H	NOP	Enter Resetting Power-Down	Resetting Power-Down	
Other States	H	H	Refer to the Command Truth Table				

Notes:

1. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
2. "CS#" is the logic state of CS# at the clock rising edge n;
3. "Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least twice during the t_{XP} period.
10. The clock must toggle at least twice during the t_{XSR} time.
11. 'X' means 'Don't care'.
12. Upon exiting Resetting Power Down, the device will return to the Idle state if t_{INIT5} has expired.

State Truth Tables

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

Table 5. Current State Bank n - Command to Bank n

Notes 1 – 5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	Activate	Select and activate row	Active	
	Refresh (All banks)	Begin to refresh	Refreshing (All banks)	6
	MRW	Load value to Mode Register	MR Writing	6
	MRR	Read value from Mode Register	Idle, MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6,7
	Precharge	Deactivate row(s) in bank or banks	Precharging	8,14
Row Active	Read	Select column and start read burst	Reading	
	Write	Select column and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Reading	Read	Select column and start new read burst	Reading	9,10
	Write	Select column and start write burst	Writing	9,10,11
	BST	Read burst terminate	Active	12
Writing	Write	Select column and start new write burst	Writing	9,10
	Read	Select column and start read burst	Reading	9,10,13
	BST	Write burst terminate	Active	12
Power-on	Reset	Begin Device Auto-Initialization	Resetting	6,8
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: The bank or banks have been precharged, and t_{RP} has been met.
   Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accessesare in progress.
   Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in the following table.
   Precharging: starts with the registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when t_{RFCab} is met. Once t_{RFCab} is met, the device will be in an 'all banks idle' state.
   Idle MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
   MR Writing: starts with the registration of an MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
   Precharging All: starts with the registration of a Precharge-All command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
6. Not bank-specific; requires that all banks are idle and no bursts are in progress.
7. Not bank-specific reset command is achieved through Mode Register Write command.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
10. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
11. A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
12. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
13. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
14. If a Precharge command is issued to a bank in the Idle state, t_{RP} shall still apply.

Table 6. Current State Bank n - Command to Bank m

Notes 1 – 6 apply to all parameters and conditions

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current state of bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active or precharging	Activate	Select and activate row in bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10,12
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	
Reading (Auto precharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Writing (Auto precharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,15
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Reading with Auto precharge	Read	Select column, and start read burst from Bank m	Reading	7,14
	Write	Select column, and start write burst to Bank m	Writing	7,13,14
	Activate	Select and activate row in bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Writing with Auto precharge	Read	Select column, and start read burst from Bank m	Reading	7,14,15
	Write	Select column, and start write burst to Bank m	Writing	7,14
	Activate	Select and activate row in bank m	Active	
	Precharge	Deactivate row(s) in bank or banks	Precharging	8
Power-On	Reset	Begin Device Auto-Initialization	Resetting	11,16
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:
   Idle: The bank has been precharged and t_{RP} has been met.
   Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accessesare in progress.
   Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   Idle MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of an MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
   MR Writing: starts with the registration of an MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
7. t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.)
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active).

14. A Write command may be applied after the completion of the Read burst; otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the precharge and auto-precharge clarification table are followed.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

Table 7. DM Truth Table

Functional Name	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

Power-up, Initialization, and Power-off

The device must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp:

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × V_{DDCA}) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up.

The following conditions apply:
Ta is the point when any power supply first reaches 300mV.

After Ta is reached:
- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins may not exceed 100mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.

Power ramp duration t_{INIT0} (Tb - Ta) must be no greater than 20ms.

Note V_{DD2} is not present in some systems. Rules related to V_{DD2} in those cases do not apply.

2. CKE and clock:

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x t_{CK} prior to the first low to high transition of CKE (Tc). CKE, CS# and CA inputs must observe setup and hold time (t_{IS}, t_{IH}) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 us. (Td).

3. Reset Command

After t_{INIT3} is satisfied, the MRW Reset command must be issued (Td). An optional Precharge all command can be issued prior to the MRW Reset command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands.

4. MRRs and Device Auto Initialization (DAI) Polling

After t_{INIT4} is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification.

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0.

All SDRAM devices will set the DAI-bit no later than t_{INIT5} (10 us) after the Reset command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

5. ZQ Calibration

After t_{INIT5} (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT}.

6. Normal Operation

After t_{ZQINIT} (Tg), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

The LPDDR2 device will now be in idle state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section "Input Clock Stop and Frequency Change".

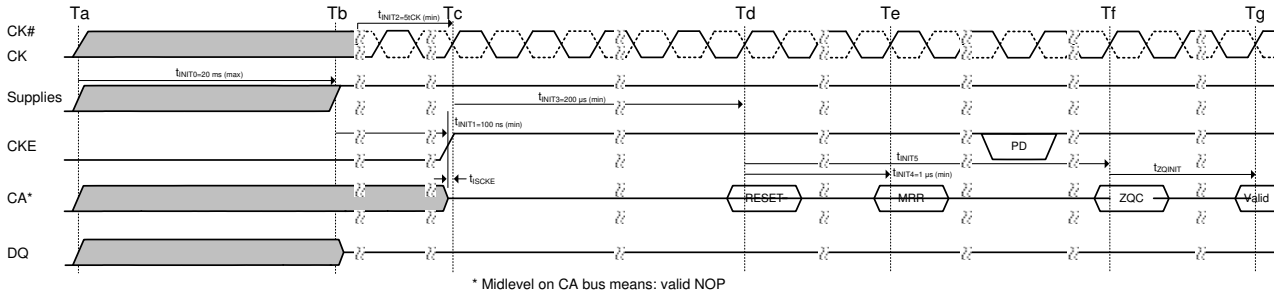


Figure 4. Power Ramp and Initialization Sequence

Table 8. Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage ramp time
t_{INIT1}	100	-	ns	Minimum CKE low time after completion of voltage ramp
t_{INIT2}	5	-	t_{CK}	Minimum stable clock before first CKE high
t_{INIT3}	200	-	us	Minimum idle time after first CKE assertion
t_{INIT4}	1	-	us	Minimum idle time after Reset command
t_{INIT5}	-	10	us	Maximum duration of device auto initialization
t_{ZQINIT}	1	-	us	ZQ initial calibration
t_{CKb}	18	100	ns	Clock cycle time during boot

Initialization after Reset (Without Voltage Ramp)

If the Reset command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

Power-off Sequence

While removing power, CKE shall be held at a logic low level (≤ 0.2 x V_{DDCA}), all other inputs shall be between V_{ILmin} and V_{IHmax}. The device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during power off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition Table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (t_{POFF}) shall be less than 2s.

The following conditions apply:
Between Tx and Tz, V_{DD1} must be greater than V_{DD2} - 200 mV.
Between Tx and Tz, V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200 mV.
Between Tx and Tz, V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200 mV.
Between Tx and Tz, V_{REF} must always be less than all other supply voltages.

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins may not exceed 100 mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Table 9. Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	t_{POFF}	-	2	sec

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off. The time between Tx and Tz (t_{POFF}) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

V_{DD1} and V_{DD2} shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

Mode Register Assignment and Definition

Table below shows the mode registers. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Table 10. Mode Register Assignments

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device Info.	R	RFU			RZQI (optional)		DNVI	DI	DAI
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02h	Device Feature 2	W	RFU					RL & WL		
3	03h	I/O Config-1	W	RFU					DS		
4	04h	Reserved	R	RFU							
5	05h	Basic Config-1	R	Manufacturer ID							
6	06h	Basic Config-2	R	Revision ID1							
7	07h	Basic Config-3	R	Revision ID2							
8	08h	Basic Config-4	R	I/O width			Density				Type
9	09h	Test Mode	W	Vendor-specific test mode							
10	0Ah	I/O Calibration	W	Calibration code							
11-15	0Bh-0Fh	Reserved		RFU							
16	10h	PASR_Bank	W	Bank mask							
17	11h	Reserved	W	RFU							
18-31	12h-1Fh	Reserved		RFU							
32	20h	DQ Calibration Pattern A	R	See “DQ Calibration”							
33-39	21h-27h	Do Not Use									
40	28h	DQ Calibration Pattern B	R	See “DQ Calibration”							
41-47	29h-2Fh	Do Not Use									
48-62	30h-3Eh	Reserved		RFU							
63	3Fh	Reset	W	X							
64-255	40h-FFh	Reserved		RFU							

Notes:

1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, DQS# shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

Table 11. MR0 Device Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI (Optional)[*3]		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP[0]	0b: DAI complete 1b: DAI still in progress
DI (Device Information)	Read-only	OP[1]	0b: S4 SDRAM
DNVI (Data Not Valid Information)	Read-only	OP[2]	0b: DNV not supported
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	00b: RZQ self test not supported 01b: ZQ-pin may connect to V_{DDCA} or float 10b: ZQ-pin may short to GND 11b: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DDCA} or float nor short to GND)

Notes:

1. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10, as defined above), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-ohm ±1%).

Table 12. MR1 Device Feature 1

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)*[1]			WC	BT	BL		

BL	Write-only	OP[2:0]	010b: BL4 (default) 011b: BL8 100b: BL16 All others: reserved
BT	Write-only	OP[3]	0b: Sequential (default) 1b: Interleaved
WC	Write-only	OP[4]	0b: Wrap (default) 1b: No wrap
nWR	Write-only	OP[7:5]	001b: nWR=3 (default) 010b: nWR=4 011b: nWR=5 100b: nWR=6 101b: nWR=7 110b: nWR=8 All others: reserved

Notes:
1. The programmed value in nWR register is the number of clock cycles that determines when to start internal precharge operation for a Write burst with AP enabled. It is determined by RU (t_{WR}/t_{CK}).

Table 13. Burst Sequence by BL, BT, and WC

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
4	Any	X	X	0b	0b	W	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
	Any	X	X	X	0b	NW	y	y+1	y+2	y+3												
8	Seq	X	0b	0b	0b	W	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	Any	X	X	X	0b	NW	Illegal (not supported)															
16	Seq	0b	0b	0b	0b	W	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b		Illegal (not supported)															
	Any	X	X	X	0b	NW	Illegal (not supported)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL = 4, the burst address represents C[1:0].
3. For BL = 8, the burst address represents C[2:0].
4. For BL = 16, the burst address represents C[3:0].
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable y can start at any address with C0 equal to 0, but must not start at any address shown in the following table.
6. “W” means Wrap, “NW” means No Wrap, “Any” means Sequential and interleaved.”Seq” means sequential and “Int” means interleaved.

Table 14. Non Wrap Restrictions

Width	256Mb
Not across full page boundary	
X32	FE, FF, 00, 01
Not across sub page boundary	
X32	None

Notes: Non-wrap BL = 4 data orders shown above are prohibited.

Table 15. MR2 Device Feature 2

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL & WL			

RL & WL	Write-only	OP[3:0]	0001b: RL = 3 / WL = 1 (default) 0010b: RL = 4 / WL = 2 0011b: RL = 5 / WL = 2 0100b: RL = 6 / WL = 3 0101b: RL = 7 / WL = 4 0110b: RL = 8 / WL = 4 All others: reserved

Table 16. MR3 I/O Configuration 1

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

DS	Write-only	OP[3:0]	0000b: reserved 0001b: 34.3Ω typical 0010b: 40Ω typical (default) 0011b: 48Ω typical 0100b: 60Ω typical 0101b: reserved for 68.6Ω typical 0110b: 80Ω typical 0111b: 120Ω typical (optional) All others: reserved

Table 17. MR5 Basic Configuration 1

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Manufacturer ID	Read-only	OP[7:0]	0000 0100b: Etron

Table 18. MR8 Basic Configuration 4

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	00b: S4 SDRAM All others: reserved
Density	Read-only	OP[5:2]	0010b: 256Mb All others: reserved
I/O width	Read-only	OP[7:6]	00b: x32 All others: reserved

Table 19. MR10 Calibration

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write Only	OP[7:0]	1111 1111b: Calibration command after initialization 1010 1011b: Long Calibration 0101 0110b: Short Calibration 1100 0011b: ZQ Reset All others: reserved

Notes:
1. Host processor shall not write MR10 with "Reserved" values.
2. The device ignores calibration commands when a reserved value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to V_{SSCA} through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command) or default calibration (through the ZQ Reset command) is supported. If ZQ is connected to $_{VDDCA}$, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. Devices that do not support calibration shall ignore the ZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

Table 20. MR16 PASR Bank Mask

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Bank Mask			

Bank Mask	Write-only	OP[3:0]	0b: refresh enable to the bank (= unmasked, default) 1b: refresh blocked (= masked)

OP	Bank Mask	4-Bank
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3

Command Definitions

Activate Command

The Activate command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA1 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The device can accept a Read or Write command at t_{RCD} after the Activate command is issued. After a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD}.

Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, Reads can be interrupted by Reads and Writes can be interrupted by Writes, provided that the interrupt occurs on a 4-bit boundary and that t_{CCD} is met.

Burst Read Operation

The burst Read command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r–CA6r and CA1f–CA9f determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the Read command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid data is available RL × t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock when the Read command is issued. The data strobe output is driven LOW t_{RPRE} before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

Reads interrupted by a read

A burst read can be interrupted by another read on even clock cycles after the Read command, provided that t_{CCD} is met.

Burst Write Operation

The burst Write command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the Write command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid data must be driven WL × t_{CK} + t_{DQSS} from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW t_{WPRE} prior to the data input. The data bits of the burst cycle must be applied to the DQ pins t_{DS} prior to the respective edge of the DQS, DQS# and held valid until t_{DH} after that edge. The burst data are sampled on successive edges of the DQS, DQS# until the burst length is completed, which is 4, 8, or 16 bit burst. t_{WR} must be satisfied before a precharge command to the same bank may be issued after a burst write operation. Input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Writes interrupted by a write

A burst write can only be interrupted by another write on even clock cycles after the Write command, provided that $t_{CCD(min)}$ is met.

Burst Terminate Command

The Burst Terminate (BST) command is initiated by having CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Terminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL × t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst WL × t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

The 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

Write Data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

Precharge Operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access t_{RPab} after an All-Bank Precharge command is issued and t_{RPpb} after a Single-Bank Precharge command is issued.

For 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge (t_{RPab}) is equal to the Row Precharge time for a Single-Bank Precharge (t_{RPpb}).

Activate to Precharge timing is shown in Activate Command.

Table 21. Bank selection for Precharge by address bits

AB (CA4r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s)
0	0	0	Bank 0 only
0	0	1	Bank 1 only
0	1	0	Bank 2 only
0	1	1	Bank 3 only
1	Don't Care	Don't Care	All Banks

Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (t_{RP}). A precharge command cannot be issued until after t_{RAS} is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called t_{RTP} (Read to Precharge).

For LPDDR2-S4 devices, t_{RTP} begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when t_{RTP} begins. For LPDDR2 Read-to-Precharge timings, see the Precharge and Auto Precharge Clarification table.

Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the t_{WR} delay.

LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time (t_{WR}) starts at different boundaries.

For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(t_{WR}/t_{CK}) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

For LPDDR2 Write-to-Precharge timings, see the Precharge and Auto Precharge Clarification table.

Auto Precharge operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

Burst Read with Auto-Precharge:

If AP (CA0f) is HIGH when a Read command is issued, the Read with auto-precharge function is engaged.

The devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU (t_{RTP}/t_{CK}) clock cycles later than the Read with auto precharge command, whichever is greater. For LPDDR2 auto-precharge calculations, see the Precharge and Auto Precharge Clarification table.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

a) The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto- precharge begins.
b) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Burst write with Auto-Precharge:

If AP (CA0f) is HIGH when a Write command is issued, the Write with auto precharge function is engaged. The device starts an auto precharge on the rising edge t_{WR} cycles after the completion of the burst Write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

a) The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto-precharge begins.
b) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Table 22. Precharge and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between "From Command" to "To Command"	Unit	Note
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU (t_{RTP}/t_{CK})) - 2	t_{CK}	1
	Precharge All	BL/2 + max(2, RU (t_{RTP}/t_{CK})) - 2	t_{CK}	1
BST (for Read)	Precharge (to same Bank as Read)	1	t_{CK}	1
	Precharge All	1	t_{CK}	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU (t_{RTP}/t_{CK})) - 2	t_{CK}	1,2
	Precharge All	BL/2 + max(2, RU (t_{RTP}/t_{CK})) - 2	t_{CK}	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU (t_{RTP}/t_{CK})) - 2 + RU (t_{RPpb}/t_{CK})	t_{CK}	1
	Write or Write w/AP (same bank)	Illegal	t_{CK}	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU ($t_{DQSCKmax}/t_{CK}$) - WL + 1	t_{CK}	3
	Read or Read w/AP (same bank)	Illegal	t_{CK}	3
	Read or Read w/AP (different bank)	BL/2	t_{CK}	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
	Precharge All	WL + BL/2 + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
BST (for Write)	Precharge (to same Bank as Write)	WL + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
	Precharge All	WL + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
	Precharge All	WL + BL/2 + RU (t_{WR}/t_{CK}) + 1	t_{CK}	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU (t_{WR}/t_{CK}) + 1 + RU (t_{RPpb}/t_{CK})	t_{CK}	1
	Write or Write w/AP (same bank)	Illegal	t_{CK}	3
	Write or Write w/AP (different bank)	BL/2	t_{CK}	3
	Read or Read w/AP (same bank)	Illegal	t_{CK}	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU (t_{WTR}/t_{CK}) +1	t_{CK}	3
Precharge	Precharge (to same Bank as Precharge)	1	t_{CK}	1
	Precharge All	1	t_{CK}	1
Precharge All	Precharge	1	t_{CK}	1
	Precharge All	1	t_{CK}	1

Notes:

1. For a given bank, the Precharge period should be counted from the latest Precharge command, which will be either a one-bank Precharge command or a Precharge All command, issued to that bank. The Precharge period is satisfied after t_{RP}, depending on the latest Precharge command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After a Read with auto precharge command, seamless Read operations to different banks are supported. After a Write with auto precharge command, seamless Write operations to different banks are supported. Read with auto precharge and Write with auto precharge commands must not be interrupted or truncated.

Refresh command

The Refresh command is initiated with CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. All-bank Refresh is initiated with CA3 HIGH at the rising edge of the clock.

An all-bank Refresh command (REFab) issues a Refresh command to all banks. All banks must be idle when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- t_{RFCab} has been satisfied following the prior REFab command
- t_{RP} has been satisfied following the prior Precharge commands.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- t_{RFCab} latency must be satisfied before issuing an Activate command
- t_{RFCab} latency must be satisfied before issuing a REFab command.

Table 23. Command Scheduling Separations related to Refresh

Symbol	Minimum Delay From…	To…
t_{RFCab}	REFab	REFab
		Activate command to any bank
t_{RRD}	Activate	Activate command to different bank than prior Activate

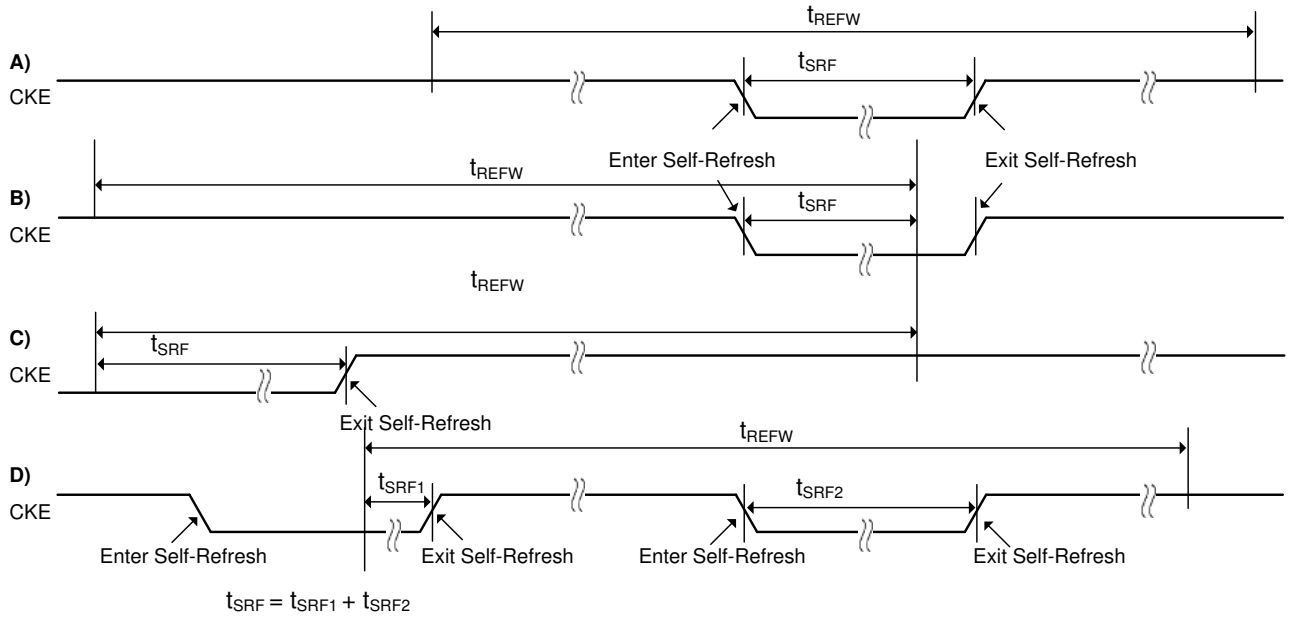
Refresh Requirements

a) Minimum number of Refresh commands:
LPDDR2 requires a minimum number, R, of Refresh (REFab) commands within any rolling refresh window (t_{REFW} = 32 ms @ MR4[2:0] = 011 or $T_C \leq 85°C$). For t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings.

b) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling t_{REFBW} (t_{REFBW} = 4 x 8 x t_{RFCab}).

c) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

$$R' = RU\left\{\frac{tSRF}{tREFI}\right\} = R - RU\left\{R \times \frac{tSRF}{tREFW}\right\}$$; where RU stands for the round-up function.



Notes:
Several examples on how to t_{SRF} is calculated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (tREFW),
B: at Self-Refresh entry
C: at Self-Refresh exit
D: with several different intervals spent in Self Refresh during one tREFW interval

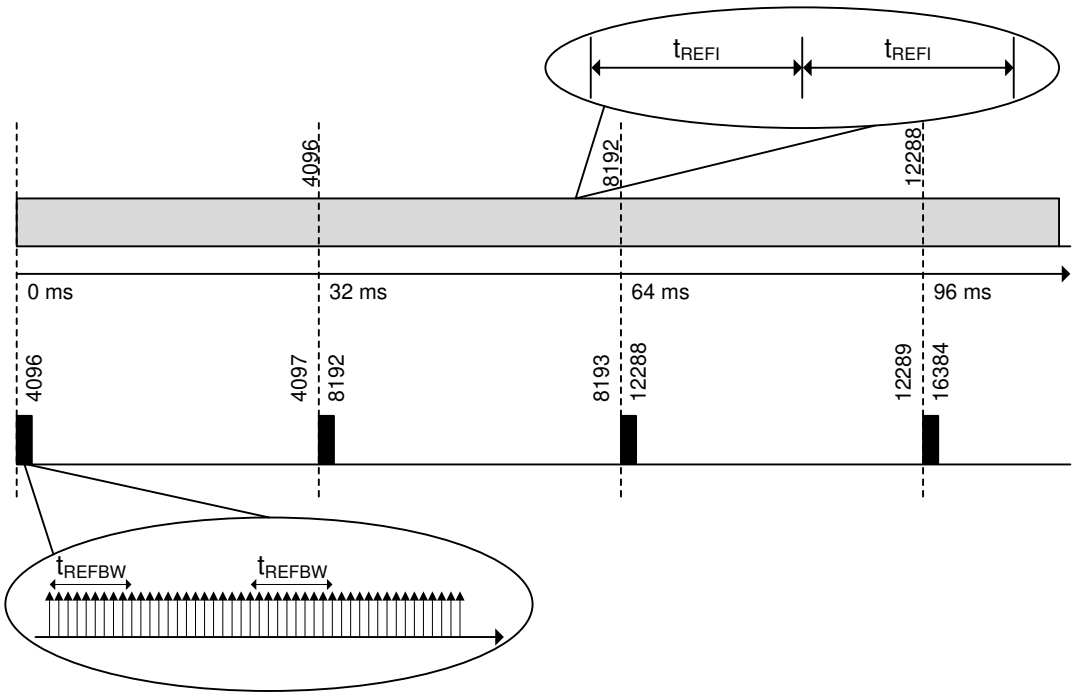
Figure 5. t_{SRF} Definition

Mobile LPDDR2 devices allow significant flexibility in scheduling refresh commends, as long as the boundary conditions above are met.

In the most straight forward case a refresh command should be scheduled every t_{REFI}. In this case Self-Refresh may be entered at any time.

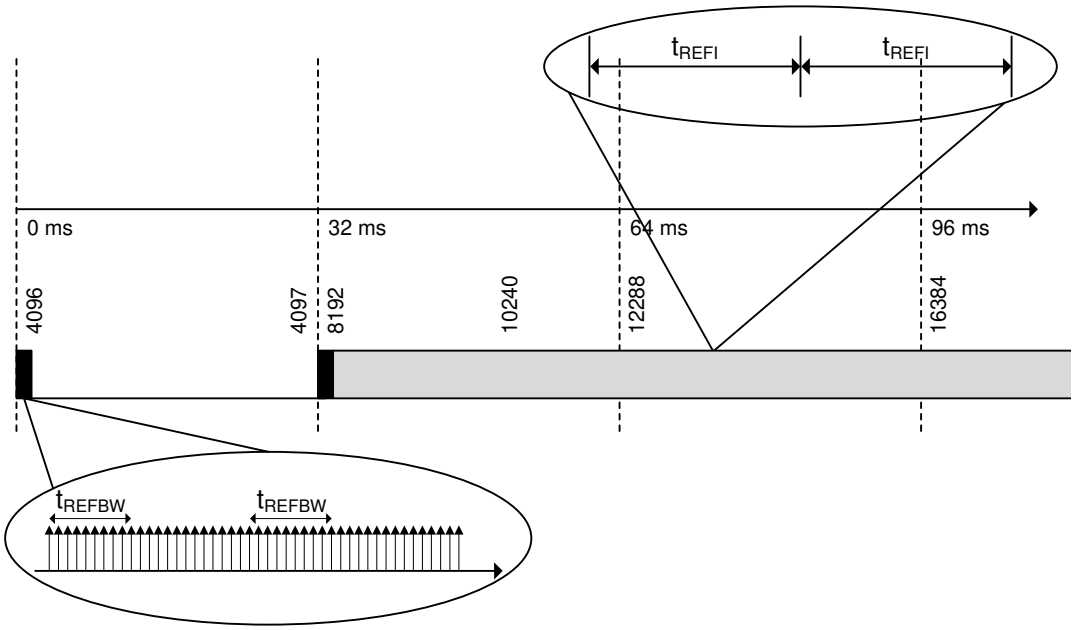
The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., 256Mb LPDDR2) the user may choose to issue a refresh burst of 4096 refresh commands with the maximum allowable rate (limited by t_{REFBW}) followed by a long time without any refresh commands, until the refresh window is complete, then repeating this sequence. The maximum supported time without refresh commands is calculated as follows: t_{REFW} - (R / 8) x t_{REFBW} = t_{REFW} - R x 4 x t_{RFCab}. (e.g., for a LPDDR2 256Mb device @ $T_C \leq 85°C$ this can be up to 32 ms - 4096 x 4 x 90 ns ≈ 30 ms).

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition. Figure 7 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling t_{REFW} intervals will have at least the required number of refresh commands. Figure 8 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling t_{REFW} intervals the minimmun number of refresh commands is not satisfied. The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure 9 and begin with the burst phase upon exit from Self-Refresh.



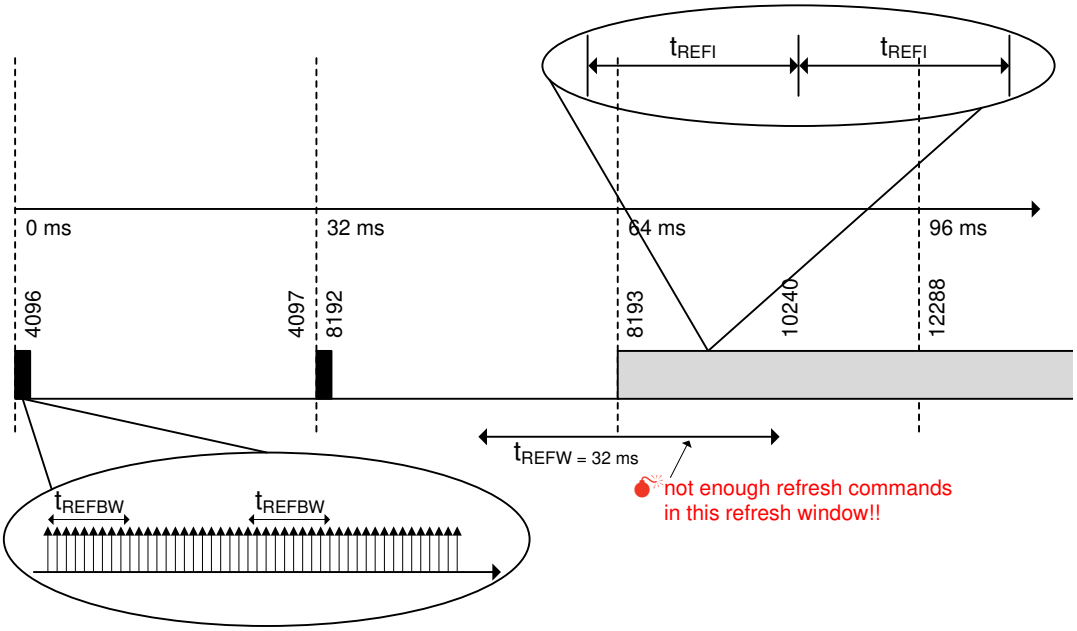
Notes:
1. Compared to repetitive burst Refresh with subsequent Refresh pause.
2. As an example, in a 256Mb LPDDR2 device at $T_{CASE} \leq 85°C$, the distributed refresh pattern would have one refresh command per 7.8 µs; the burst refresh pattern would have an average of one refresh command per 0.36 µs followed by ≈ 30 ms without any refresh command.

Figure 6. Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause



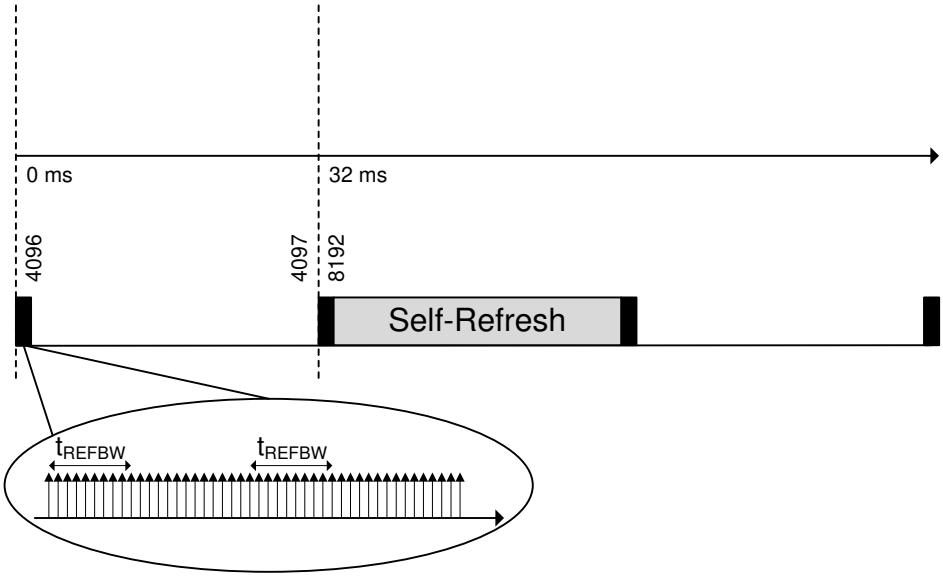
Notes:
1. Shown with subsequent Refresh pause to regular distributed Refresh pattern.
2. As an example, in a 256Mb LPDDR2 device at $T_{CASE} \leq 85°C$, the distributed refresh pattern would have one refresh command per 7.8 µs; the burst refresh pattern would have an average of one refresh command per 0.36 µs followed by ≈ 30 ms without any refresh command.

Figure 7. Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



Notes:
1. Shown with subsequent refresh pause to regular distributed refresh pattern.
2. Only ~2048 refresh commands (<R which is 4096) in the indicated t_{REFW} windows.

Figure 8. Not Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



Note: 1. In conjunction with a burst/pause refresh pattern.

Figure 9. Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns

Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in self refresh mode.

LPDDR2 SDRAM devices can operate in Self Refresh in both the standard or extended temperature ranges. These devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (V_{DD1}, V_{DD2}, and V_{DDCA}) must be at valid levels. V_{DDQ} may be turned off during Self-Refresh. Prior to exiting Self-Refresh, V_{DDQ} must be within specified limits. V_{REFDQ} and V_{REFCA} may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self-Refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (see Recommended DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is t_{CKESR}. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 t_{CK} prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSR}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (one all-bank) is issued before entry into a subsequent Self Refresh.

Partial Array Self-Refresh (PASR) -- PASR Bank Masking

The LPDDR2 SDRAM has eight banks. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 4 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 4 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, the corresponding bank mask bit must be programmed as “unmasked”.

Mode Register Read (MRR) Command

The Mode Register Read (MRR) command is used to read configuration and status data from mode registers. The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ [7:0] after RL × t_{CK} + t_{DQSCK} + t_{DQSQ} following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are toggled for the duration of the mode register read burst.

The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS, DQS# shall be toggled.

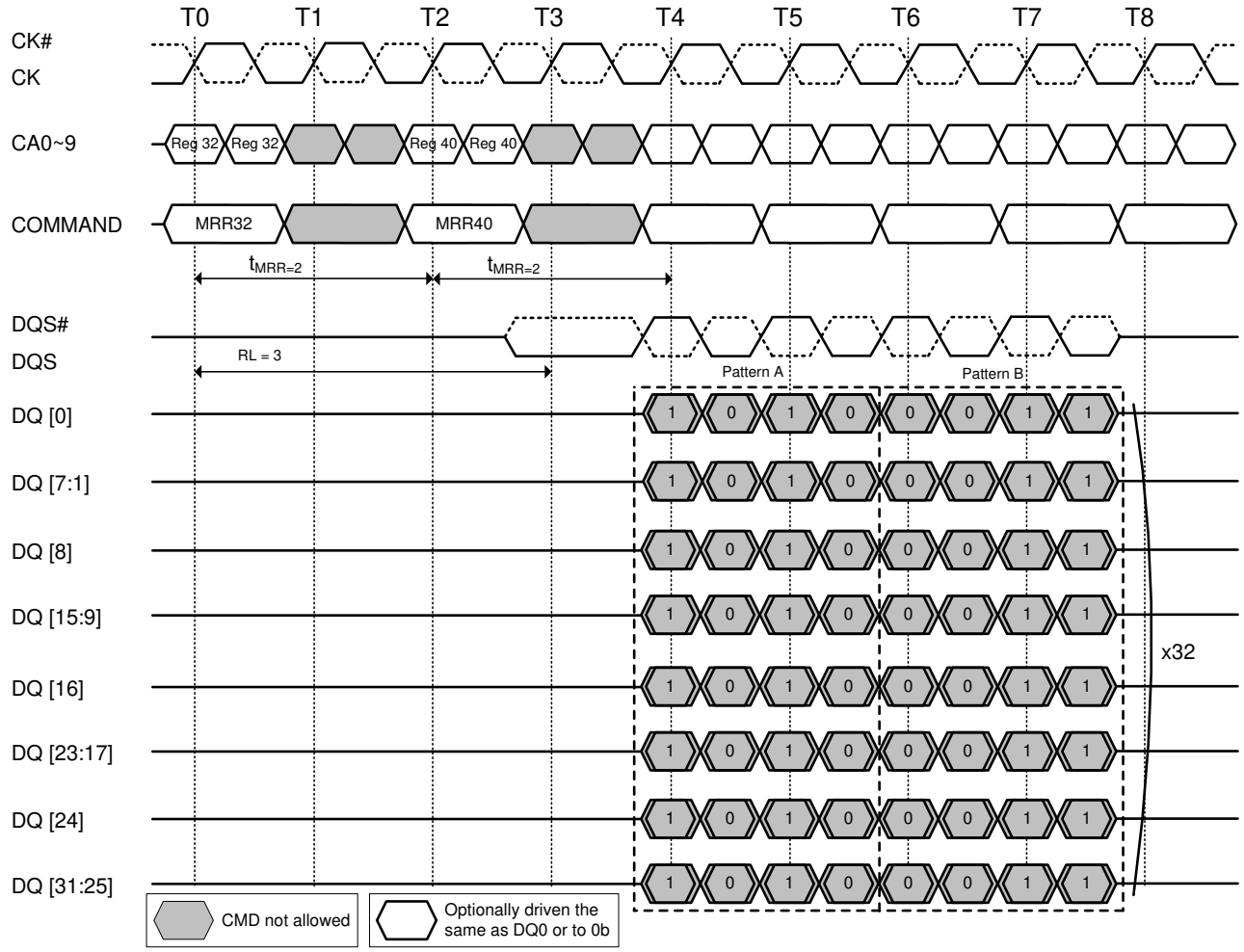
The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(t_{WTR}/t_{CK}) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL”.

DQ Calibration

LPDDR2 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern "A") or MR40 (Pattern "B") will return the specified pattern on DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Table 24. Data Calibration Pattern Description

Pattern	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern "A" (MR32)	1	0	1	0
Pattern "B" (MR40)	0	0	1	1



Notes:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst.
   For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
4. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
5. The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

Figure 10. MR32 and MR40 DQ Calibration timing example: RL = 3, t_{MRR} = 2

Mode Register Write (MRW) Command

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode register writes to read-only registers have no impact on the functionality of the device.

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a Precharge-All command.

Table 25. Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	
	MRW (Reset)	Resetting, device auto initialization	
Bank(s) active	MRR	Reading mode register, bank(s) active	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (Reset)	Not allowed	Not allowed

MRW Reset

The MRW Reset command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence (see the Voltage Ramp and Device Initialization section). The MRW Reset command can be issued from the idle state. This command resets all mode registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period (t_{INIT4}). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW Reset command.

For MRW Reset timing, see the Voltage Ramp and Initialization Sequence figure.

Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 output drivers (RON) over process, temperature, and voltage. LPDDR2 devices support ZQ Calibration.
There are four ZQ calibration commands and related timings: t_{ZQINIT}, $t_{ZQRESET}$, t_{ZQCL}, and t_{ZQCS}. t_{ZQINIT} is for initialization calibration; $t_{ZQRESET}$ for resetting ZQ setting to default; t_{ZQCL} is for long calibration(s); and t_{ZQCS} is for short calibration(s). See Mode Register 10 (MR10) for description on the command codes for the different ZQ Calibration commands.

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR2. ZQINIT provides an output impedance accuracy of ±15 %. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 %. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system. The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQCorrection) of output impedance errors within t_{ZQCS} for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR2 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

Where T_{sens} = max ($dR_{ON}dT$) and V_{sens} = max ($dR_{ON}dV$) define temperature and voltage sensitivities.

For example, if T_{sens} = 0.75%/°C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1°C/sec and
$V_{driftrate}$ = 15mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4\text{s}$$

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus and the data bus shall be un-terminated during calibration periods (t_{ZQINIT}, t_{ZQCL}, or t_{ZQCS}). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent t_{ZQINIT}, t_{ZQCS}, and t_{ZQCL} overlap between the devices. ZQ Reset overlap is acceptable. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to V_{DDCA}. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See Output Driver DC Electrical Characteristics without ZQ Calibration table)

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240Ω ±1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

Power-down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS# HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, preactive, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until t_{CKE} has been satisfied. V_{REF} must be maintained at a valid level during power down.

V_{DDQ} may be turned off during power down. If V_{DDQ} is turned off, then V_{REFDQ} must also be turned off. Prior to exiting power down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (See Recommended DC Operating Conditions table).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section LPDDR2 SDRAM Refresh Requirements, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with power-down exit latency, t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.

All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power Down, CKE must be held LOW.

In Deep Power Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the device. All power supplies must be within specified limits prior to exiting Deep Power Down. V_{REFDQ} and V_{REFCA} may be at any level within minimum and maximum levels (see Absolute Maximum Ratings). However prior to exiting Deep Power Down, V_{REF} must be within specified limits (See Recommended DC Operating Conditions).

The contents of the device will be lost upon entry into Deep Power Down mode.

The Deep Power Down state is exited when CKE is registered HIGH, while meeting t_{ISCKE} with a stable clock input. The device must be fully re-initialized as described in the power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

Input clock stop and frequency change

The device support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab commands may be executing;
- Any Activate, Preactive or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

The devices support clock stop during CKE LOW under the following conditions:

- CK is held LOW and CK# is held HIGH during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab commands may be executing;
- Any Activate, Preactive or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

The devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- CS# shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK is held LOW and CK# is held HIGH during clock stop;
- CS# shall be held HIGH during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab commands may be executing;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.

No Operation command

The purpose of the No Operation command (NOP) is to prevent the device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS# HIGH at the clock rising edge N.
2. CS# LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Table 26. Absolute Maximum Rating

Symbol	Parameter	Values	Unit	Note
V_{DD1}	V_{DD1} supply voltage relative to V_{SS}	-0.4~2.3	V	2
V_{DD2}	V_{DD2} supply voltage relative to V_{SS}	-0.4~1.6	V	2
V_{DDCA}	V_{DDCA} supply voltage relative to V_{SSCA}	-0.4~1.6	V	2,4
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SSQ}	-0.4~1.6	V	2,3
V_{IN}, V_{OUT}	Voltage on any I/O relative to V_{SS}	-0.4~1.6	V	
T_{STG}	Storage Temperature	-55~125	°C	5

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See "Power-Ramp" in section "Power-Up and Initialization" for relationships between power supplies.
3. $V_{REFDQ} \leq 0.6 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.
4. $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$ provided that $V_{REFDCA} \leq 300mV$.
5. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

Table 27. Operating Temperature Condition

Symbol	Parameter	Values	Unit	Note
T_{OPER}	Operating Temperature Range	-25~85	°C	

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device.
2. Either the device case temperature rating can be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature.

Table 28. Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$V_{DD1\ (DC)}$	Core power 1	1.7	1.8	1.95	V	1
$V_{DD2\ (DC)}$	Core power 2	1.14	1.2	1.3	V	1
$V_{DDCA\ (DC)}$	Input buffer power	1.14	1.2	1.3	V	1
$V_{DDQ\ (DC)}$	I/O buffer power	1.14	1.2	1.3	V	1
I_L	Input leakage current	-2	-	2	μA	2,5
I_{VREF}	V_{REF} supply leakage current	-1	-	1	μA	3,4

Notes:
1. V_{DD1} uses significantly less power than V_{DD2}.
2. For CA, CKE, CS#, CK, CK#. Any input $0V \leq V_{IN} \leq V_{DDCA}$ (All other pins not under test = 0V)
3. $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$ (All other pins not under test = 0V)
4. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.
5. Although DM is for input only, the DM leakage shall match the DQ and DQS/DQS# output leakage specification.

AC and DC Logic Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

Table 29. Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min.	Max.		
$V_{IHCA\ (AC)}$	AC input logic HIGH	V_{REF} + 0.220	-	V	1,2
$V_{ILCA\ (AC)}$	AC input logic LOW	-	V_{REF} - 0.220	V	1,2
$V_{IHCA\ (DC)}$	DC input logic HIGH	V_{REF} + 0.130	V_{DDCA}	V	1
$V_{ILCA\ (DC)}$	DC input logic LOW	V_{SSCA}	V_{REF} - 0.130	V	1
$V_{REFCA\ (DC)}$	Reference voltage for CA/CS# inputs	0.49 x V_{DDCA}	0.51 x V_{DDCA}	V	3,4

Notes:
1. For CA and CS# input only pins. $V_{REF\ =\ VREFCA\ (DC)}$.
2. See “Overshoot and Undershoot Specifications”.
3. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA\ (DC)}$ by more than ±1% V_{DDCA} (for reference: approx. ±12 mV).
4. For reference: approx. V_{DDCA}/2 ±12 mV.

Table 30. Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IHCKE}	CKE Input High Level	0.8 x V_{DDCA}	-	V	1
V_{ILCKE}	CKE Input Low Level	-	0.2 x V_{DDCA}	V	1

Notes:
1. See “Overshoot and Undershoot Specifications”.

Table 31. Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min.	Max.		
$V_{IHDQ(AC)}$	AC input logic high	V_{REF} + 0.220	-	V	1,2
$V_{ILDQ(AC)}$	AC input logic low	-	V_{REF} - 0.220	V	1,2
$V_{IHDQ(DC)}$	DC input logic high	V_{REF} + 0.130	V_{DDQ}	V	1
$V_{ILDQ(DC)}$	DC input logic low	V_{SSQ}	V_{REF} - 0.130	V	1
$V_{REFDQ(DC)}$	Reference Voltage for DQ/DM inputs	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	3,4

Notes:
1. For DQ input only pins. V_{REF} = $V_{REFDQ\ (DC)}$.
2. See “Overshoot and Undershoot Specifications”.
3. The AC peak noise on V_{REFDQ} may not allow V_{REFDQ} to deviate from $V_{REFDQ\ (DC)}$ by more than ±1% V_{DDQ} (for reference: approx. ±12 mV).
4. For reference: approx. V_{DDQ}/2 ±12 mV.

AC and DC Logic Input Levels for Differential Signals

Differential swing requirements for clock (CK – CK#) and strobe (DQS – DQS#)

Table 32. Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min.	Max.		
$V_{IHdiff\ (DC)}$	Differential input HIGH	2 x ($V_{IH(DC)}$ - V_{REF})	-	V	1
$V_{ILdiff\ (DC)}$	Differential input LOW	-	2 x ($V_{IL(DC)}$ - V_{REF})	V	1
$V_{IHdiff\ (AC)}$	Differential input HIGH AC	2 x ($V_{IH(AC)}$ - V_{REF})	-	V	2
$V_{ILdiff\ (AC)}$	Differential input LOW AC	-	2 x ($V_{IL(AC)}$ - V_{REF})	V	2

Notes:

1. Used to define a differential signal slew-rate. For CK - CK# use $V_{IH}/V_{IL(DC)}$ of CA and V_{REFCA}; for DQS - DQS#, use $V_{IH}/V_{IL(DC)}$ of DQs and V_{REFDQ}; if a reduced DC-high or DC-low level is used for a signal group, then the reduced level applies also here.
2. For CK - CK# use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS - DQS#, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# need to be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”.
4. For CK and CK#, $V_{REF} = V_{REFCA(DC)}$; For DQS and DQS#, $V_{REF} = V_{REFDQ(DC)}$.

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, CK#, or DQS#) has also to comply with certain requirements for single-ended signals.

CK and CK# shall meet $V_{SEH(AC)min}$/$V_{SEL(AC)max}$ in every half-cycle.
DQS, DQS# shall meet $V_{SEH(AC)min}$/$V_{SEL(AC)max}$ in every half-cycle preceding and following a valid transition.
The applicable AC-levels for CA and DQ's are different per speed-bin.

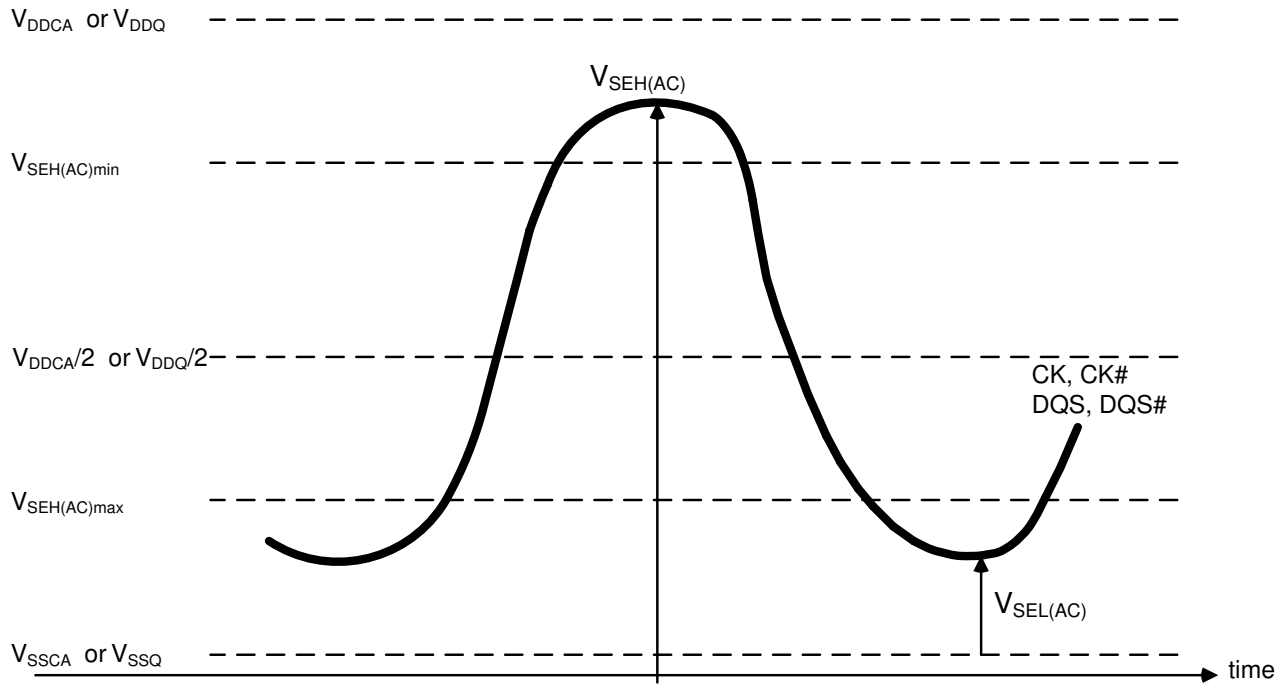


Figure 11. Single-ended requirement for differential signals

Note that while CA and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS, DQS# and $V_{DDCA}/2$ for CK, CK#; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)max}$, $V_{SEH(AC)min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.
The signal ended requirements for CK, CK#, DQS, and DQS# are found in Table 29 and Table 31, respectively.

Table 33. Single-Ended Levels for CK, CK#, DQS, DQS#

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min.	Max.		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	$(V_{DDQ}/2) + 0.220$	-	V	1,2
	Single-ended HIGH level for CK, CK#	$(V_{DDCA}/2) + 0.220$	-	V	1,2
$V_{SEL(AC)}$	Single-ended LOW level for strobes	-	$(V_{DDQ}/2) - 0.220$	V	1,2
	Single-ended LOW level for CK, CK#	-	$(V_{DDCA}/2) - 0.220$	V	1,2

Notes:
1. For CK and CK#, use V_{SEH}/$V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and DQS#[3:0]), use V_{IH}/$V_{IL(AC)}$ of DQ.
2. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS[3:0] and DQS#[3:0] need to be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications".

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the specifications in the table above. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

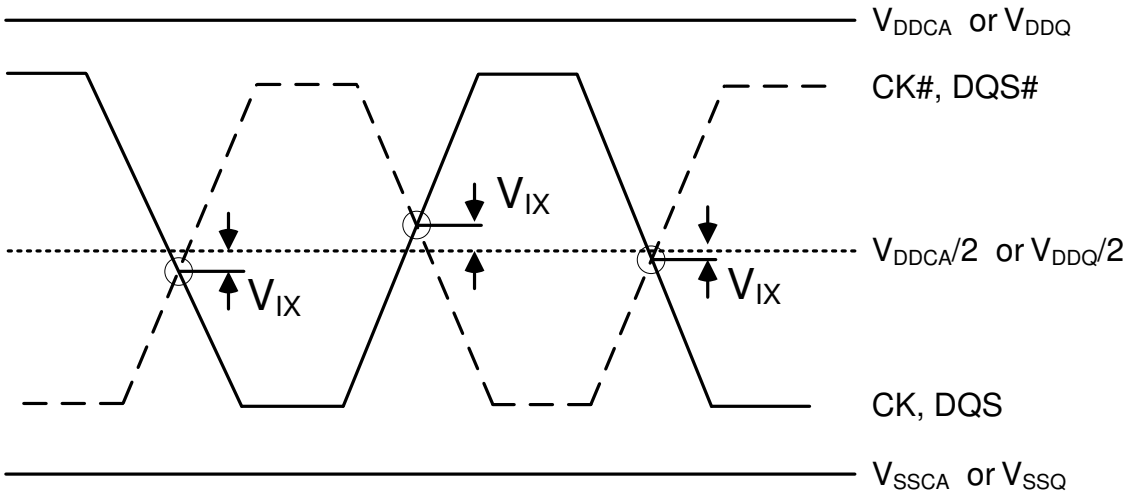


Figure 12. V_{IX} Definition

Table 34. Crosspoint Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	Values		Unit	Note
		Min.	Max.		
V_{IXCA}	Differential input crosspoint voltage relative to V_{DDCA}/2 for CK and CK#	-120	120	mV	1,2
V_{IXDQ}	Differential input crosspoint voltage relative to V_{DDQ}/2 for DQS and DQS#	-120	120	mV	1,2

Notes:

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK and CK#, V_{REF} = $V_{REFCA(DC)}$. For DQS and DQS#, V_{REF} = $V_{REFDQ(DC)}$.

Input Slew Rate

Table 35. Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$

Notes:
1. The differential signal (CK/CK# and DQS/DQS#) must be linear between these thresholds.

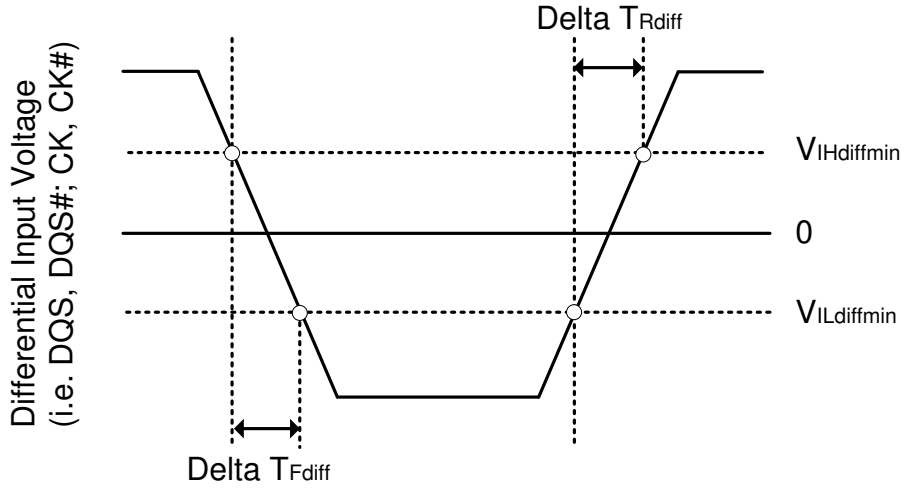


Figure 13. Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

AC and DC Output Measurement Levels

Table 36. Single-ended AC and DC Output Levels

Symbol	Parameter		Values	Unit	Note
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, DQS#) (DQ, DQS, DQS# are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta R_{ON} between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

Notes:
1. I_{OH} = -0.1mA.
2. I_{OL} = 0.1mA.

Table 37. Differential AC and DC Output Levels

Symbol	Parameter	Values	Unit	Note
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level (for output SR)	+0.2 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output LOW measurement level (for output SR)	-0.2 x V_{DDQ}	V	2

Notes:
1. I_{OH} = -0.1mA.
2. I_{OL} = 0.1mA.

Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals.

Table 38. Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

Notes:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

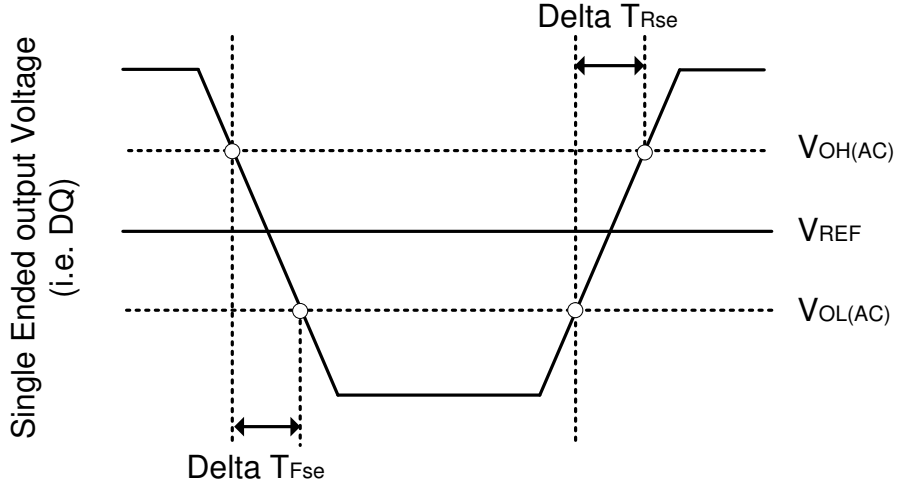


Figure 14. Single Ended Output Slew Rate Definition

Table 39. Output Slew Rate (single-ended)

Symbol	Parameter	Values		Unit
		Min	Max	
SRQ_{SE}	Single-ended output slew rate (R_{ON} = 40Ω ±30%)	1.5	3.5	V/ns
	Single-ended output slew rate (R_{ON} = 60Ω ±30%)	1.0	2.5	V/ns
	Output slew-rate-matching ratio (pull-up to pull-down)	0.7	1.4	

Definitions:
SR: Slew rate;
Q: Query Output (like in DQ, which stands for Data-in, Query-Output);
SE: Single-ended signals.

Notes:
1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under normal simultaneous switching output (SSO) conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ for differential signals.

Table 40. Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TF_{diff}$

Notes:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

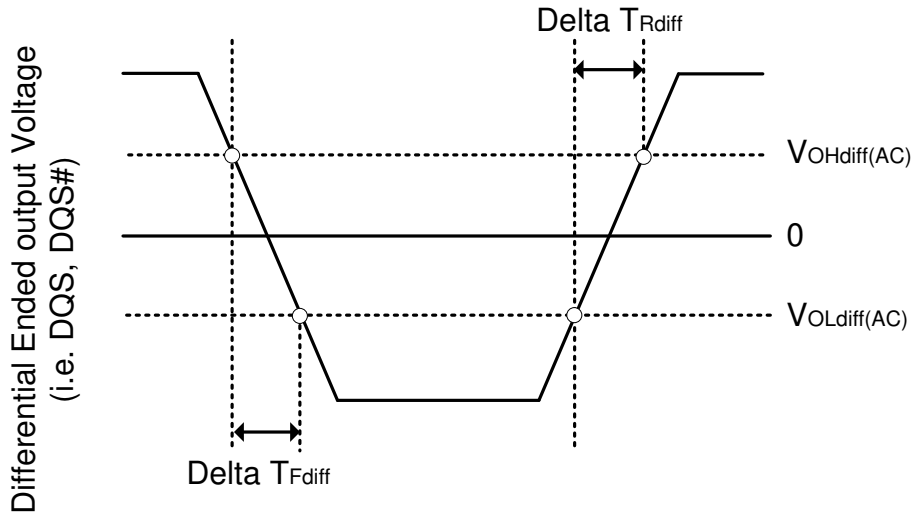


Figure 15. Differential Output Slew Rate Definition

Table 41. Differential Output Slew Rate

Symbol	Parameter	Values		Unit
		Min	Max	
SRQ_{diff}	Differential output slew rate (R_{ON} = 40Ω ±30%)	3.0	7.0	V/ns
	Differential output slew rate (R_{ON} = 60Ω ±30%)	2.0	5.0	V/ns

Definitions:
SR: Slew rate;
Q: Query Output (like in DQ, which stands for Data-in, Query-Output);
diff: Differential signals

Notes:
1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
3. Slew rates are measured under normal simultaneous switching output (SSO) conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Overshoot/Undershoot Specification

Table 42. AC Overshoot/Undershoot Specification

Parameter	1066	800	667	Unit
	Max			
Maximum peak amplitude allowed for overshoot area	0.35	0.35	0.35	V
Maximum peak amplitude allowed for undershoot area	0.35	0.35	0.35	V
Maximum area above V_{DD}	0.15	0.20	0.24	V/ns
Maximum area below V_{SS}	0.15	0.20	0.24	V/ns

Notes:
1. For CA[9:0], CK, CK#, CS#, and CKE, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.
2. For CA[9:0], CK, CK#, CS#, and CKE, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.
3. V_{SS} stands for V_{SSCA} for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, ODT, DQS, and DQS#.
4. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
5. Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

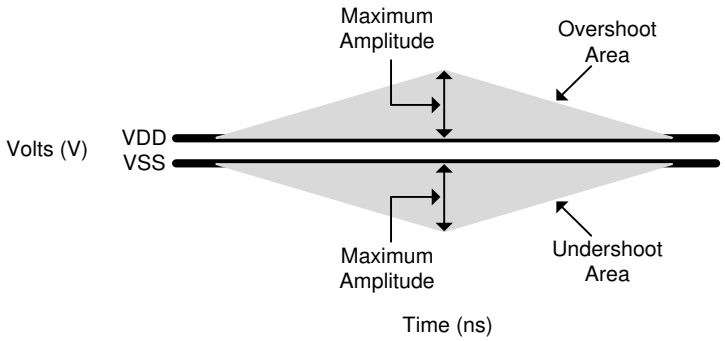


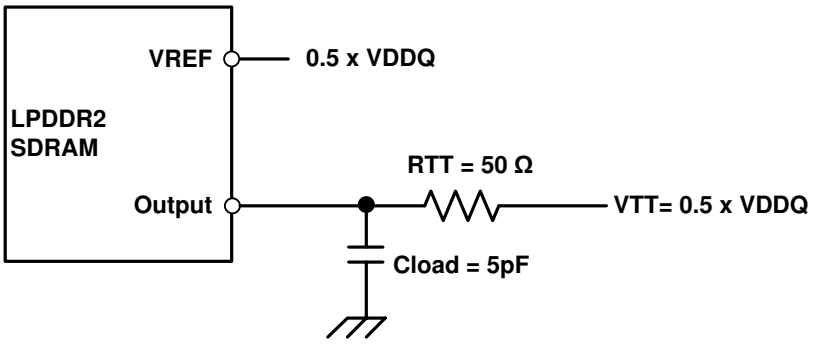
Figure 16. Overshoot and Undershoot Definition

Notes:
1. For CA[9:0], CK, CK#, CS#, and CKE, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.
2. For CA[9:0], CK, CK#, CS#, and CKE, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.
3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4. Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

Output buffer characteristics

HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Notes:

1. All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Figure 17. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

RONPU and RONPD Resistor Definition

$$R_{ONPU} = \frac{(V_{DDQ} - V_{out})}{ABS\ (Iout)}$$

Note1: This is under the condition that R_{ONPD} is turned off

$$R_{ONPD} = \frac{(V_{out})}{ABS\ (Iout)}$$

Note1: This is under the condition that R_{ONPU} is turned off

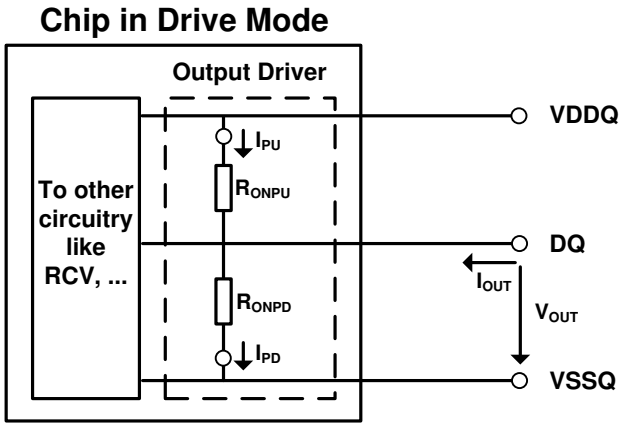


Figure 18. Output Driver: Definition of Voltages and Currents

R_{ONPU} and R_{ONPD} Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ}. Nominal R_{ZQ} is 240Ω.

Table 43. Output Driver DC Electrical Characteristics without ZQ Calibration

R_{ONNOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	R_{ON34PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1-4
	R_{ON34PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1-4
40.0Ω	R_{ON40PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1-4
	R_{ON40PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1-4
48.0Ω	R_{ON48PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1-4
	R_{ON48PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1-4
60.0Ω	R_{ON60PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	1-4
	R_{ON60PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	1-4
80.0Ω	R_{ON80PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	1-4
	R_{ON80PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	1-4
120.0Ω (optional)	$R_{ON120PD}$	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	1-4
	$R_{ON120PU}$	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	1-4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1-5

Notes:
1. Across entire operating temperature range, after calibration.
2. R_{ZQ} = 240 Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}.
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure R_{ONPU} and R_{ONPD}, both at 0.5 x V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

For example, with $MM_{PUPD(max)}$ = 15% and R_{ONPD} = 0.85, R_{ONPU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 44. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Note
R_{ONPD} R_{ONPU}	0.5 x V_{DDQ}	85 – ($dR_{ON}dT \times |\Delta T|$) – ($dR_{ON}dV \times |\Delta V|$)	115 + ($dR_{ON}dT \times |\Delta T|$) + ($dR_{ON}dV \times |\Delta V|$)	%	1-2

Notes:
1. ΔT = T – T (@ calibration), ΔV = V – V (@ calibration)
2. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table 45. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	%/°C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	%/mV

R_{ONPU} and R_{ONPD} Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by design and characterization as default setting.

Table 46. Output Driver DC Electrical Characteristics without ZQ Calibration

R_{ONNOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	R_{ON34PD}	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
	R_{ON34PU}	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
40.0Ω	R_{ON40PD}	0.5 x V_{DDQ}	28	40	52	Ω	1
	R_{ON40PU}	0.5 x V_{DDQ}	28	40	52	Ω	1
48.0Ω	R_{ON48PD}	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
	R_{ON48PU}	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
60.0Ω	R_{ON60PD}	0.5 x V_{DDQ}	42	60	78	Ω	1
	R_{ON60PU}	0.5 x V_{DDQ}	42	60	78	Ω	1
80.0Ω	R_{ON80PD}	0.5 x V_{DDQ}	56	80	104	Ω	1
	R_{ON80PU}	0.5 x V_{DDQ}	56	80	104	Ω	1
120.0Ω (optional)	$R_{ON120PD}$	0.5 x V_{DDQ}	84	120	156	Ω	1
	$R_{ON120PU}$	0.5 x V_{DDQ}	84	120	156	Ω	1

Notes:
1. Across entire operating temperature range, without calibration.

Input/Output Capacitance

Table 47. Capacitance (Notes 1, 2 apply for all values)

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

Symbol	Parameter	Min.	Max.	Unit	Note
C_{CK}	Input Capacitance (CK, CK#)	1.0	2.0	pF	
C_{DCK}	Input capacitance delta (CK, CK#)	0	0.2	pF	3
C_I	Input capacitance (all other input only pins)	1.0	2.0	pF	4
C_{DI}	Input capacitance delta (all other input only pins)	-0.40	0.40	pF	5
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#)	1.25	2.5	pF	6~7
C_{DDQS}	Input/output capacitance delta (DQS, DQS#)	0	0.25	pF	7~8
C_{DIO}	Input/output capacitance delta (DQ, DM)	-0.5	0.5	pF	7, 9
C_{ZQ}	Input/output capacitance ZQ Pin	0	2.5	pF	

Notes:

1. This parameter applies to monolithic devices only.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA)) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, V_{SSQ} applied and all other pins floating.
3. Absolute value of C_{CK} - $C_{CK\#}$.
4. C_I applies to CS#, CKE and CA[9:0].
5. $C_{DI} = C_I - 0.5 \times (C_{CK} + C_{CK\#})$.
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).
8. Absolute value of C_{DQS} and $C_{DQS\#}$.
9. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS} + C_{DQS\#})$ in byte-lane.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: $V_{IN} \leq V_{IL\ (DC)\ MAX}$
HIGH: $V_{IN} \geq V_{IH\ (DC)\ MIN}$
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See the following three tables

Table 48. Switching for CA Input Signals

CK/ CK#	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising
Cycle	N		N+1		N+2		N+3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:
1. CS# must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require Switching on the CA bus.

Table 49. Switching for I_{DD4R}

Clock	CKE	CS#	Cycle	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	HLHLLHL	L
Rising	H	L	N+2	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N+2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The above pattern (N, N+1...) is used continuously during IDD measurement for I_{DD4R}.

Table 50. Switching for I_{DD4W}

Clock	CKE	CS#	Cycle	Command	CA[0:2]	CA[3:9]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	HLHLLHL	L
Rising	H	L	N+2	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N+2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for I_{DD4W}.

Table 51. IDD Specification Parameters and Operating Conditions

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V) (Notes 1-3 apply to all parameters)

Parameter & Test Condition	Symbol	Power Supply	1066	800	667	Unit	Note
			Max.				
Operating one bank active-precharge current: $t_{RC}=t_{RC(min)}$; $t_{CK}=t_{CK(min)}$; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	$IDD0_1$	V_{DD1}	16	16	16	mA	
	$IDD0_2$	V_{DD2}	26	21	16	mA	
	$IDD0_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
Idle power-down standby current: $t_{CK}=t_{CK(min)}$; CKE is LOW; CS# is HIGH; All banks idle; CA bus inputs are switching; Data bus inputs are stable	$IDD2P_1$	V_{DD1}	0.4	0.4	0.4	mA	
	$IDD2P_2$	V_{DD2}	1	1	1	mA	
	$IDD2P_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	$IDD2PS_1$	V_{DD1}	0.4	0.4	0.4	mA	
	$IDD2PS_2$	V_{DD2}	1	1	1	mA	
	$IDD2PS_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	
Idle non-power-down standby current: $t_{CK}=t_{CK(min)}$; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	$IDD2N_1$	V_{DD1}	0.6	0.6	0.6	mA	
	$IDD2N_2$	V_{DD2}	15	15	15	mA	
	$IDD2N_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
Idle non-power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	$IDD2NS_1$	V_{DD1}	0.6	0.6	0.6	mA	
	$IDD2NS_2$	V_{DD2}	10	8	8	mA	
	$IDD2NS_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
Active power-down standby current: $t_{CK}=t_{CK(min)}$; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	$IDD3P_1$	V_{DD1}	1	1	1	mA	
	$IDD3P_2$	V_{DD2}	8	8	8	mA	
	$IDD3P_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	$IDD3PS_1$	V_{DD1}	1	1	1	mA	
	$IDD3PS_2$	V_{DD2}	8	8	8	mA	
	$IDD3PS_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	
Active non-power-down standby current: $t_{CK}=t_{CK(min)}$; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	$IDD3N_1$	V_{DD1}	1.5	1.5	1.5	mA	
	$IDD3N_2$	V_{DD2}	20	20	20	mA	
	$IDD3N_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
Active non-power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	$IDD3NS_1$	V_{DD1}	1.5	1.5	1.5	mA	
	$IDD3NS_2$	V_{DD2}	15	15	15	mA	
	$IDD3NS_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
Operating burst Read current: $t_{CK}=t_{CK(min)}$; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = $RL_{(min)}$; CA bus inputs are switching; 50% data change each burst transfer	$IDD4R_1$	V_{DD1}	2	2	2	mA	
	$IDD4R_2$	V_{DD2}	155	140	125	mA	
	$IDD4R_{IN}$	V_{DDCA}	6.5	6.5	6.5	mA	
Operating burst Write current: $t_{CK}=t_{CK(min)}$; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = $WL_{(min)}$; CA bus inputs are switching; 50% data change each burst transfer	$IDD4W_1$	V_{DD1}	2	2	2	mA	
	$IDD4W_2$	V_{DD2}	150	140	130	mA	
	$IDD4W_{IN}$	V_{DDCA}, V_{DDQ}	30	30	30	mA	
All-bank Refresh burst current: $t_{CK}=t_{CK(min)}$; CKE is HIGH between valid commands; t_{RC} = $t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	$IDD5_1$	V_{DD1}	38	34	30	mA	
	$IDD5_2$	V_{DD2}	38	34	30	mA	
	$IDD5_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	
All-bank Refresh average current: $t_{CK}=t_{CK(min)}$; CKE is HIGH between valid commands; t_{RC} = t_{REFI}; CA bus inputs are switching; Data bus inputs are stable	$IDD5AB_1$	V_{DD1}	2	2	2	mA	
	$IDD5AB_2$	V_{DD2}	16	16	16	mA	
	$IDD5AB_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	

Self refresh current (-25°C to +85°C)**:** CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	$IDD6_1$	V_{DD1}	0.6	0.6	0.6	mA	4,5
	$IDD6_2$	V_{DD2}	1.5	1.5	1.5	mA	4,5
	$IDD6_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	4,5
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	$IDD8_1$	V_{DD1}	30	30	30	uA	
	$IDD8_2$	V_{DD2}	30	30	30	uA	
	$IDD8_{IN}$	V_{DDCA}, V_{DDQ}	100	100	100	uA	

Notes:
1. IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of V_{DDQ} and V_{DDCA}.
4. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
5. This is the general definition that applies to full-array self refresh.

Table 52. IDD6 Partial Array Self-Refresh Current

Parameter	PASR	Power Supply	-25°C to +85°C	Unit
			Max.	
IDD6 Partial Array Self-Refresh Current	Full array	V_{DD1}	600	uA
		V_{DD2}	1500	uA
		V_{DDCA}, V_{DDQ}	300	uA
	1/2 array	V_{DD1}	550	uA
		V_{DD2}	1300	uA
		V_{DDCA}, V_{DDQ}	300	uA
	1/4 array	V_{DD1}	530	uA
		V_{DD2}	1200	uA
		V_{DDCA}, V_{DDQ}	300	uA

Notes:
1. The IDD6 currents are measured using bank-masking only.
2. IDD values published are the maximum of the distribution of the arithmetic mean.

Electrical Characteristics and AC Timing

Table 53. AC Timing (Notes 4, 6, 10 apply to all parameters and conditions)

(T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, V_{DD2} = 1.14-1.3V)

Symbol	Parameter	Min. t_{CK}	Data Rate						Unit
			1066		800		667		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CK}	Maximum clock frequency		533		400		333		MHz
Clock Timing									
$t_{CK(avg)}$	Average clock period		1.875	100	2.5	100	3	100	ns
$t_{CH(avg)}$	Average HIGH pulse width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
$t_{CL(avg)}$	Average LOW pulse width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
$t_{CK(abs)}$	Absolute clock period		**Min:** $t_{CK(avg)min} + t_{JIT(per),min}$						ns
$t_{CH(abs)}$, allowed	Absolute clock HIGH pulse width (with allowed jitter)		0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}
$t_{CL(abs)}$, allowed	Absolute clock LOW pulse width (with allowed jitter)		0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}
$t_{JIT(per)}$, allowed	Clock period jitter (with allowed jitter)		-90	90	-100	100	-110	110	ps
$t_{JIT(cc)}$, allowed	Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)		-	180	-	200	-	220	ps
$t_{JIT(duty)}$, allowed	Duty cycle jitter (with allowed jitter)		**Min:** min(($t_{CH(abs),min}$ - $t_{CH(avg),min}$), ($t_{CL(abs),min}$ - $t_{CL(avg),min}$)) × $t_{CK(avg)}$ **Max:** max(($t_{CH(abs),max}$ - $t_{CH(avg),max}$), ($t_{CL(abs),max}$ - $t_{CL(avg),max}$)) × $t_{CK(avg)}$						ps
$t_{ERR(2per)}$, allowed	Cumulative errors across 2 cycles		-132	132	-147	147	-162	162	ps
$t_{ERR(3per)}$, allowed	Cumulative errors across 3 cycles		-157	157	-175	175	-192	192	ps
$t_{ERR(4per)}$, allowed	Cumulative errors across 4 cycles		-175	175	-194	194	-214	214	ps
$t_{ERR(5per)}$, allowed	Cumulative errors across 5 cycles		-188	188	-209	209	-230	230	ps
$t_{ERR(6per)}$, allowed	Cumulative errors across 6 cycles		-200	200	-222	222	-244	244	ps
$t_{ERR(7per)}$, allowed	Cumulative errors across 7 cycles		-209	209	-232	232	-256	256	ps
$t_{ERR(8per)}$, allowed	Cumulative errors across 8 cycles		-217	217	-241	241	-266	266	ps
$t_{ERR(9per)}$, allowed	Cumulative errors across 9 cycles		-224	224	-249	249	-274	274	ps
$t_{ERR(10per)}$, allowed	Cumulative errors across 10 cycles		-231	231	-257	257	-282	282	ps
$t_{ERR(11per)}$, allowed	Cumulative errors across 11 cycles		-237	237	-263	263	-289	289	ps
$t_{ERR(12per)}$, allowed	Cumulative errors across 12 cycles		-242	242	-269	269	-296	296	ps
$t_{ERR(nper)}$, allowed	Cumulative errors across n = 13, 14, 15…, 49, 50 cycles		**Min:** $t_{ERR(nper)}$,allowed, min = (1 + 0.68ln(n)) x $t_{JIT(per)}$, allowed, min **Max:** $t_{ERR\ (nper)}$, allowed, max = (1 + 0.68ln(n)) x $t_{JIT(per)}$, allowed, max						ps
ZQ Calibration Parameters									
t_{ZQINIT}	Initialization calibration time		1	-	1	-	1	-	µs
t_{ZQCL}	Long calibration time	6	360	-	360	-	360	-	ns
t_{ZQCS}	Short calibration time	6	90	-	90	-	90	-	ns
$t_{ZQRESET}$	Calibration Reset time	3	50	-	50	-	50	-	ns

Read Parameters [11]									
t_{DQSCK}	DQS output access time from CK/CK#		2500	5500	2500	5500	2500	5500	ps
$t_{DQSCKDS}$	DQSCK delta short [15]		-	330	-	450	-	540	ps
$t_{DQSCKDM}$	DQSCK delta medium [16]		-	680	-	900	-	1050	ps
$t_{DQSCKDL}$	DQSCK delta long [17]		-	920	-	1200	-	1400	ps
t_{DQSQ}	DQS-DQ skew		-	200	-	240	-	280	ps
t_{QHS}	Data hold skew factor		-	230	-	280	-	340	ps
t_{QSH}	DQS output HIGH pulse width		**Min:** $t_{CH(abs)}$ - 0.05						t_{CK}
t_{QSL}	DQS output LOW pulse width		**Min:** $t_{CL(abs)}$ - 0.05						t_{CK}
t_{QHP}	Data half period		**Min:** $(t_{QSH}, t_{QSL})_{min}$						t_{CK}
t_{QH}	DQ/DQS output hold time from DQS		**Min:** t_{QHP} - t_{QHS}						ps
t_{RPRE}	READ preamble [12, 13]		**Min:** 0.9						t_{CK}
t_{RPST}	READ postamble [12, 14]		**Min:** $t_{CL(abs)}$ - 0.05						t_{CK}
$t_{LZ(DQS)}$	DQS Low-Z from clock [12]		**Min:** $t_{DQSCKmin}$ - 300						ps
$t_{LZ(DQ)}$	DQ Low-Z from clock [12]		**Min:** $t_{DQSCKmin}$ - 300						ps
$t_{HZ(DQS)}$	DQS High-Z from clock [12]		**Max:** $t_{DQSCKmax}$ - 100						ps
$t_{HZ(DQ)}$	DQ High-Z from clock [12]		**Max:** $t_{DQSCKmax}$ + (1.4 x $t_{DQSQmax}$)						ps
Write Parameters [11]									
t_{DH}	DQ and DM input hold time (V_{REF} based)		210	-	270	-	350	-	ps
t_{DS}	DQ and DM input setup time (V_{REF} based)		210	-	270	-	350	-	ps
t_{DIPW}	DQ and DM input pulse width		0.35	-	0.35	-	0.35	-	t_{CK}
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}
t_{DQSH}	DQS input high-level width		0.4	-	0.4	-	0.4	-	t_{CK}
t_{DQSL}	DQS input low-level width		0.4	-	0.4	-	0.4	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time		0.2	-	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK		0.2	-	0.2	-	0.2	-	t_{CK}
t_{WPST}	Write postamble		0.4	-	0.4	-	0.4	-	t_{CK}
t_{WPRE}	Write preamble		0.35	-	0.35	-	0.35	-	t_{CK}
CKE Input Parameters									
t_{CKE}	CKE minimum pulse width (HIGH and LOW pulse width)	3	3	-	3	-	3	-	t_{CK}
t_{ISCKE} [2]	CKE input setup time		0.25	-	0.25	-	0.25	-	t_{CK}
t_{IHCKE} [3]	CKE input hold time		0.25	-	0.25	-	0.25	-	t_{CK}
Command Address Input Parameters [11]									
t_{IS} [1]	Address and control input setup time (V_{REF} based)		220	-	290	-	370	-	ps
t_{IH} [1]	Address and control input hold time (V_{REF} based)		220	-	290	-	370	-	ps
t_{IPW}	Address and control input pulse width		0.4	-	0.4	-	0.4	-	t_{CK}

Boot Parameters (10 MHz–55 MHz) [5, 7, 8]									
t_{CKb}	Clock cycle time		18	100	18	100	18	100	ns
t_{ISCKEb}	CKE input setup time		2.5	-	2.5	-	2.5	-	ns
t_{IHCKEb}	CKE input hold time		2.5	-	2.5	-	2.5	-	ns
t_{ISb}	Address and control input setup time		1150	-	1150	-	1150	-	ps
t_{IHb}	Address and control input hold time		1150	-	1150	-	1150	-	ps
t_{DQSCKb}	DQS output data access time from CK/CK#		2	10	2	10	2	10	ns
t_{DQSQb}	Data strobe edge to output data edge $t_{DQSQb\ -\ 1.2}$		-	1.2	-	1.2	-	1.2	ns
t_{QHSb}	Data hold skew factor		-	1.2	-	1.2	-	1.2	ns
Mode Register Parameters									
t_{MRW}	Mode Register Write command period	5	5	-	5	-	5	-	t_{CK}
t_{MRR}	Mode Register Read command period	2	2	-	2	-	2	-	t_{CK}
Core Parameters [9]									
RL	Read latency	3	8	-	6	-	5	-	t_{CK}
WL	Write latency	1	4	-	3	-	2	-	t_{CK}
t_{RC}	Activate to Activate command period		**Min:** t_{RAS} + t_{RPab} (with all-bank precharge) t_{RAS} + t_{RPpb} (with per-bank precharge)						ns
t_{CKESR}	CKE minimum pulse width during Self Refresh (low pulse width during Self Refresh)	3	15	-	15	-	15	-	ns
t_{XSR}	Self Refresh exit to next valid command delay	2	**Min:** t_{RFCab} + 10						ns
t_{XP}	Exit power- down to next valid command delay	2	7.5	-	7.5	-	7.5	-	ns
t_{CCD}	CAS to CAS delay	2	2	-	2	-	2	-	t_{CK}
t_{RTP}	Internal Read to Precharge command delay	2	7.5	-	7.5	-	7.5	-	ns
$t_{RCD\ (fast)}$	RAS to CAS delay	3	15	-	15	-	15	-	ns
$t_{RCD\ (typ)}$		3	18	-	18	-	18	-	ns
$t_{RCD\ (slow)}$		3	24	-	24	-	24	-	ns
$t_{RPpb\ (fast)}$	Row precharge time (single bank)	3	15	-	15	-	15	-	ns
$t_{RPpb\ (typ)}$		3	18	-	18	-	18	-	ns
$t_{RPpb\ (slow)}$		3	24	-	24	-	24	-	ns
$t_{RPab\ (fast)}$	Row precharge time (all banks)	3	18	-	18	-	18	-	ns
$t_{RPab\ (typ)}$		3	21	-	21	-	21	-	ns
$t_{RPab\ (slow)}$		3	27	-	27	-	27	-	ns
t_{RAS}	Row active time	3	42	-	42	-	42	-	ns
		-	-	70	-	70	-	70	µs
t_{WR}	Write recovery time	3	15	-	15	-	15	-	ns
t_{WTR}	Internal Write to Read command delay	2	7.5	-	7.5	-	7.5	-	ns
t_{RRD}	Active bank A to Active bank B	2	10	-	10	-	10	-	ns
t_{FAW}	Four-bank Activate window	8	50	-	50	-	50	-	ns
t_{DPD}	Minimum deep power- down time	-	500	-	500	-	500	-	µs

Refresh Requirement Parameters										
t_{REFW}	Refresh Window (Tcase ≤ 85°C)		32	-	32	-	32	-	ms
t_{REFI}	Average time between Refresh commands (for reference only)	REFab (Tcase ≤ 85°C)	7.8	-	7.8	-	7.8	-	µs
t_{RFCab}	Refresh Cycle time		90	-	90	-	90	-	ns
t_{REFBW}	Burst Refresh Window = 4 x 8 x t_{RFCab}		2.88	-	2.88	-	2.88	-	µs
Temperature Derating									
t_{DQSCK} (derated)	Core Timings Temperature De-Rating		-	5620	-	6000	-	6000	ps
t_{RCD} (derated)			**Min:** t_{RCD} + 1.875						ns
t_{RC} (derated)			**Min:** t_{RC} + 1.875						ns
t_{RAS} (derated)			**Min:** t_{RAS} + 1.875						ns
t_{RP} (derated)			**Min:** t_{RP} + 1.875						ns
t_{RRD} (derated)			**Min:** t_{RRD} + 1.875						ns

Notes:

1. Input setup/hold time for signal(CA0 ~ 9, CS#).
2. CKE input setup time is measured from CKE reaching high/low voltage level to CK/CK# crossing.
3. CKE input hold time is measured from CK/CK# crossing to CKE reaching high/low voltage level.
4. Frequency values are for reference only. Clock cycle time (t_{CK}) shall be used to determine device capabilities.
5. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, t_{CK} during boot is t_{CKb}).
6. Frequency values are for reference only. Clock cycle time (t_{CK} or t_{CKb}) shall be used to determine device capabilities.
7. Mobile LPDDR2 devices set some mode register default values upon receiving a Reset (MRW) command, as specified in Mode Register Definition.
8. The output skew parameters are measured with default output impedance settings using the reference load.
9. The minimum t_{CK} column applies only when t_{CK} is greater than 6ns.
10. All AC timings assume an input slew rate of 1V/ns.
11. Read, Write, and Input Setup and Hold values are referenced to V_{REF}.
12. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses V_{TT}. t_{HZ} and t_{LZ} transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for t_{RPST}, $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$), or begins driving (for t_{RPRE}, $t_{LZ(DQS)}$, $t_{LZ(DQ)}$). The figure below shows a method to calculate the point when device is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$ by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as single-ended. The timing parameters t_{RPRE} and t_{RPST} are determined from the differential signal DQS-DQS#.

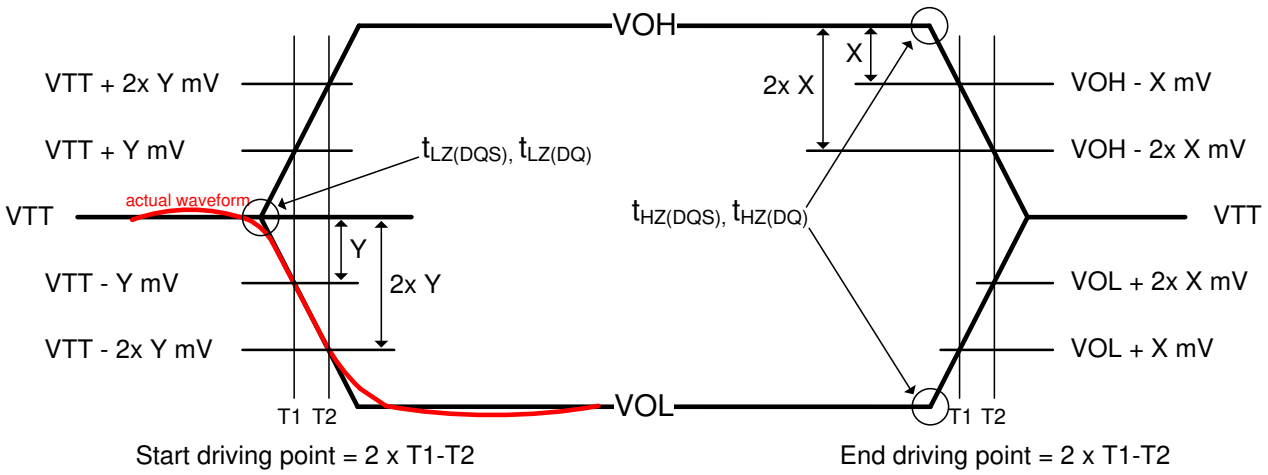


Figure 19. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

13. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.
14. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal. $t_{DQSCKDS}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. $t_{DQSCKDS}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
15. $t_{DQSCKDM}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 1.6µs rolling window. $t_{DQSCKDM}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
16. $t_{DQSCKDL}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 32ms rolling window. $t_{DQSCKDL}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
17. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: t_{RCD}, t_{RC}, t_{RAS}, t_{RP}, and t_{RRD}. The t_{DQSCK} parameter must be derated as specified in the AC Timing table. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the device.

Definitions for $t_{CK(avg)}$ and nCK:

$t_{CK(avg)}$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

Where N=200

Unit '$t_{CK(avg)}$' represents the actual clock average $t_{CK(avg)}$) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
$t_{CK(avg)}$ may change by up to ±1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

Definitions for $t_{CK(abs)}$:

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $t_{CK(abs)}$ is not subject to production test.

Definitions for $t_{CH(avg)}$ and $t_{CL(avg)}$:

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / \left(N \times tCK(avg) \right)$$

Where N=200

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / \left(N \times tCK(avg) \right)$$

Where N=200

Definitions for $t_{JIT(per)}$:

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.
$t_{JIT(per)}$ = Min/max of {t_{CKi} - $t_{CK(avg)}$ where i = 1 to 200}.
$t_{JIT(per),act}$ is the actual clock jitter for a given system.
$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

Definitions for $t_{JIT(cc)}$:

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$t_{JIT(cc)}$ = Max of |{t_{CKi+1} - t_{CKi}}|.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

Definitions for $t_{ERR(nper)}$:

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.
$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.
$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.
$t_{ERR(nper)}$ is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+N-1} tCK_j \right) - n \times tCK(avg)$$

$t_{ERR(nper),min}$ can be calculated by the formula:

$$t_{ERR(nper),\,min} = (1 + 0.68LN(n)) \times t_{JIT(per),\,min}$$

$t_{ERR(nper),max}$ can be calculated by the formula:

$$t_{ERR(nper),\,max} = (1 + 0.68LN(n)) \times t_{JIT(per),\,max}$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

Definitions for duty cycle jitter $t_{JIT(duty)}$:

$t_{JIT(duty)}$ is defined with absolute and average specification of t_{CH} / t_{CL}.

$t_{JIT(duty),\,min} = MIN((t_{CH(abs),\,min} - t_{CH(avg),\,min}), (t_{CL(abs),\,min} - t_{CL(avg),\,min})) \times t_{CK(avg)}$

$t_{JIT(duty),\,max} = MAX((t_{CH(abs),\,max} - t_{CH(avg),\,max}), (t_{CL(abs),\,max} - t_{CL(avg),\,max})) \times t_{CK(avg)}$

Definitions for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$:

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 54. Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

Symbol	Parameter	Min	Unit
$t_{CK(abs)}$	Absolute clock period	$t_{CK(avg),min} + t_{JIT(per),min}$	ps
$t_{CH(abs)}$	Absolute clock HIGH pulse width	$t_{CH(avg),min} + t_{JIT(duty),min}$ / $t_{CK(avg)min}$	t_{CK}
$t_{CL(abs)}$	Absolute clock LOW pulse width	$t_{CL(avg),min} + t_{JIT(duty),min}$ / $t_{CK(avg)min}$	t_{CK}

Notes:
1. $t_{CK(avg),min}$ is expressed is ps for this table.
2. $t_{JIT(duty),min}$ is a negative value.

Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter ($t_{JIT(per)}$) in excess of the values found in the AC Timing table and how to determine cycle time de-rating and clock cycle de-rating.

Clock period jitter effects on core timing parameters (t_{RCD}, t_{RP}, t_{RTP}, t_{WR}, t_{WRA}, t_{WTR}, t_{RC}, t_{RAS}, t_{RRD}, t_{FAW})

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support t_{nPARAM} = RU {t_{PARAM} / $t_{CK(avg)}$}.

When the device is operated with clock jitter outside specification limits, the number of clocks or $t_{CK(avg)}$ may need to be increased based on the values for each core timing parameter.

Cycle time de-rating for core timing parameters

For a given number of clocks (t_{nPARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR(tnPARAM),act}$) in excess of the allowed cumulative period error ($t_{ERR(tnPARAM),allowed}$), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{\text{tPARAM} + \text{tERR(tnPARAM),act} - \text{tERR(tnPARAM),allowed}}{\text{tnPARAM}}\right) - \text{tCK(avg)}, 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle de-rating for core timing parameters

For a given number of clocks (t_{nPARAM}) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter ($t_{JIT(per)}$).

For a given number of clocks (t_{nPARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR(tnPARAM),act}$) in excess of the allowed cumulative period error ($t_{ERR(tnPARAM),allowed}$), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{\text{tPARAM} + \text{tERR(tnPARAM),act} - \text{tERR(tnPARAM),allowed}}{\text{tCK(avg)}}\right\} - \text{tnPARAM}$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters (t_{IS}, t_{IH}, t_{ISCKE}, t_{IHCKE}, t_{ISb}, t_{IHb}, t_{ISCKEb}, t_{IHCKEb})

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/ address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters
t_{RPRE} Parameter

When the device is operated with input clock jitter, t_{RPRE} needs to be de-rated by the actual period jitter ($t_{JIT(per),act,max}$) of the input clock in excess of the allowed period jitter ($t_{JIT(per),allowed,max}$). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}\right)$$

For example,
if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)}$ = 2500 ps, $t_{JIT(per),act,min}$ = -172 ps, and $t_{JIT(per),act,max}$ = + 193 ps, then
$t_{RPRE,min,derated}$ = 0.9 - ($t_{JIT(per),act,max}$ - $t_{JIT(per),allowed,max}$)/$t_{CK(avg)}$ = 0.9 - (193 - 100)/2500 = 0.8628 $t_{CK(avg)}$.

$t_{LZ(DQ)}$, $t_{HZ(DQ)}$, t_{DQSCK}, $t_{LZ(DQS)}$, $t_{HZ(DQS)}$ Parameter

These parameters are measured from a specific clock edge to a data signal (DMn or DQm, Where: n=0,1,2,3; m= DQ[31:0]) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$).

t_{QSH}, t_{QSL} Parameter

These parameters are affected by duty cycle jitter which is represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$.
$t_{QSH(abs)min}$ = $t_{CH(abs)min}$ - 0.05
$t_{QSL(abs)min}$ = $t_{CL(abs)min}$ - 0.05
These parameters determine absolute Data-Valid Window (DVW) at the device pin. Absolute minimum DVW at the device pin = min {($t_{QSH(abs)min}$ × $t_{CK(avg)min}$ - $t_{DQSQmax}$ - t_{QHSmax}), ($t_{QSL(abs)min}$ × $t_{CK(avg)min}$ - $t_{DQSQmax}$ - t_{QHSmax})}. This minimum DVW shall be met at the target frequency regardless of clock jitter.

t_{RPST} Parameter

t_{RPST} is affected by duty cycle jitter which is represented by $t_{CL(abs)}$. Therefore $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$.
$t_{RPST(abs)min}$ = $t_{CL(abs)min}$ - 0.05 = $t_{QSL(abs)min}$.

Clock jitter effects on Write timing parameters
t_{DS}, t_{DH} Parameter

These parameters are measured from a data signal (DMn or DQm, Where n=0,1,2,3; m= DQ[31:0]) transition edge to its respective data strobe signal (DQSn, DQSn# : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

t_{DSS}, t_{DSH} Parameter

These parameters are measured from a data strobe signal (DQSx, DQSx#) crossing to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

t_{DQSS} Parameter

This parameter is measured from a data strobe signal (DQSx, DQSx#) crossing to the subsequent clock signal (CK/CK#) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter $t_{JIT(per),act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per),allowed}$.

$$tDQSS(min, derated) = 0.75 - \left(\frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK(avg)}\right)$$

$$tDQSS(max, derated) = 1.25 - \left(\frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}\right)$$

For example, if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)}$= 2500 ps, $t_{JIT(per),act,min}$= -172 ps and $t_{JIT(per),act,max}$= + 193 ps, then
$t_{DQSS,(min,derated)}$ = 0.75 - ($t_{JIT(per),act,min}$ - $t_{JIT(per),allowed,min}$)/$t_{CK(avg)}$) = 0.75 - (-172 + 100)/2500 = 0.7788 $t_{CK(avg)}$ and
$t_{DQSS,(max,derated)}$ = 1.25 - ($t_{JIT(per),act,max}$ - $t_{JIT(per),allowed,max}$)/$t_{CK(avg)}$) = 1.25 - (193 - 100) /1250 = 1.2128 $t_{CK(avg)}$.

CA and CS# Setup, Hold, and Derating

For all input signals (CA and CS#) the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the data sheet $t_{IS(base)}$ and $t_{IH(base)}$ value to the Δt_{IS} and Δt_{IH} derating value respectively.
Example: t_{IS} (total setup time) = $t_{IS(base)}$ + Δt_{IS}.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between shaded $V_{REF(DC)}$ to AC region, use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded $V_{REF(DC)}$ to AC region, the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded DC to $V_{REF(DC)}$ region, use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded DC to $V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value.

For a valid transition the input signal has to remain above/below $V_{IH}/V_{IL(AC)}$ for some time t_{VAC}.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates in between the values listed in derating table, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 55. CA and CS# Setup and Hold Base - Values for 1V/ns

Symbol	Reference	Data Rate			Unit
		1066	800	667	
$t_{IS(base)}$	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$	0	70	150	**ps**
$t_{IH(base)}$	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$	90	160	240	**ps**

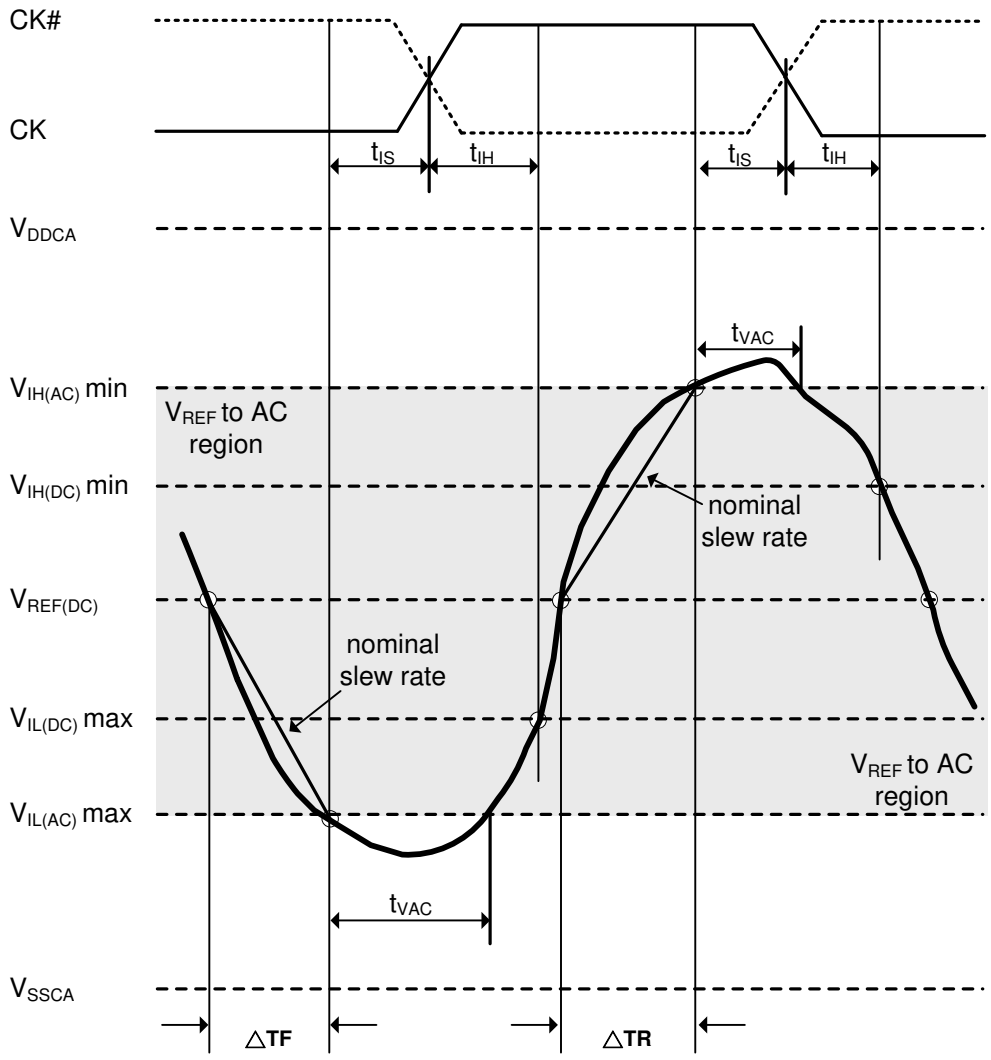
Notes: AC/DC referenced for 1V/ns CA and CS# slew rate, and 2V/ns differential CK/CK# slew rate.

Table 56. Derating Values for AC/DC-Based tIS/tIH (AC220)

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)}=V_{REF(DC)}+220mV$, $V_{IL(AC)}=V_{REF(DC)}-220mV$ DC130 Threshold -> $V_{IH(DC)}=V_{REF(DC)}+130mV$, $V_{IL(DC)})=V_{REF(DC)}-130mV$																	
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS# slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	**0**	**0**	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Table 57. Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition

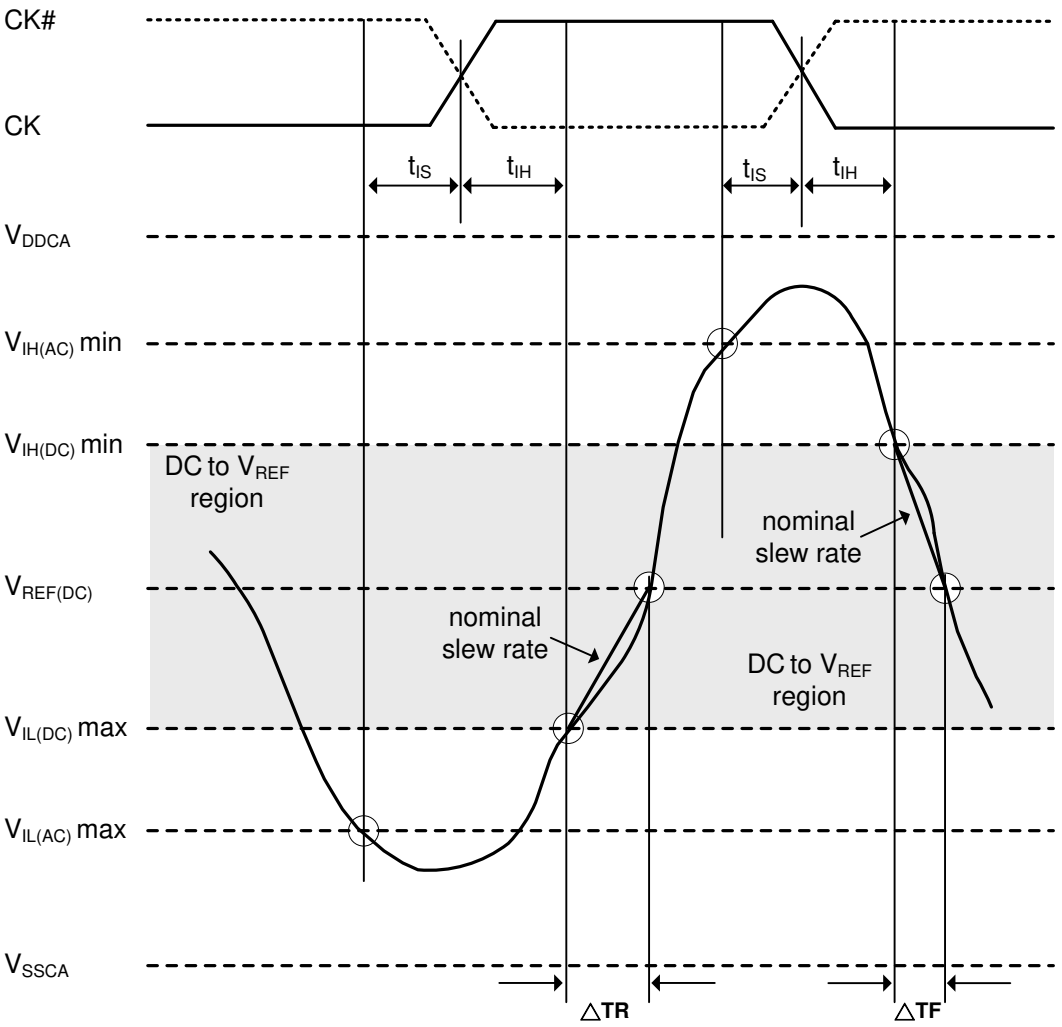
Slew Rate [V/ns]	tVAC @ 220mV [ps]	
	min	max
>2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
<0.5	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{VREF(DC) - VIL(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{VIH(AC)min - VREF(DC)}{\Delta TR}$$

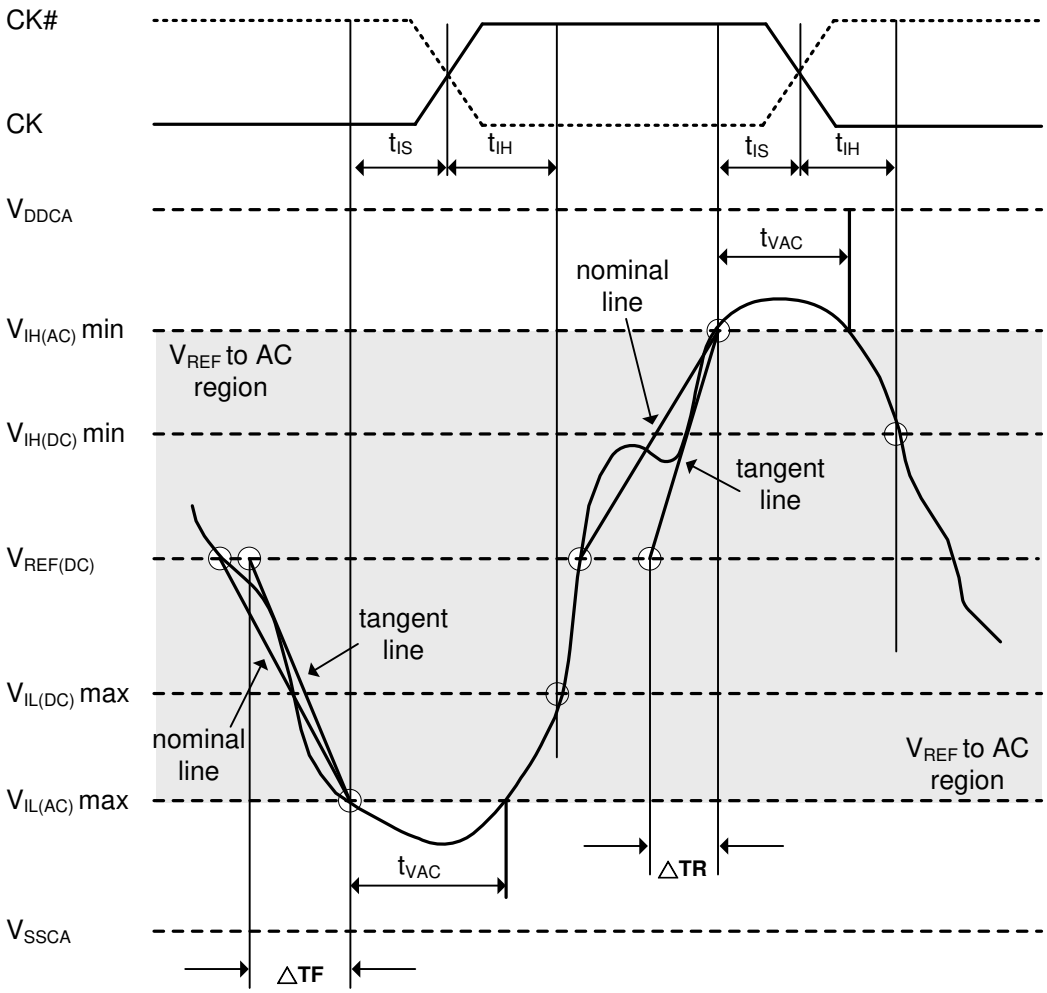
Figure 20. Illustration of nominal slew rate and tVAC for setup time tIS for CA and CS# with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{VREF(DC)} - \text{VIL(DC)max}}{\Delta\text{TR}}$$

$$\text{Hold Slew Rate Fallsing Signal} = \frac{\text{VIH(DC)min} - \text{VREF(DC)}}{\Delta\text{TF}}$$

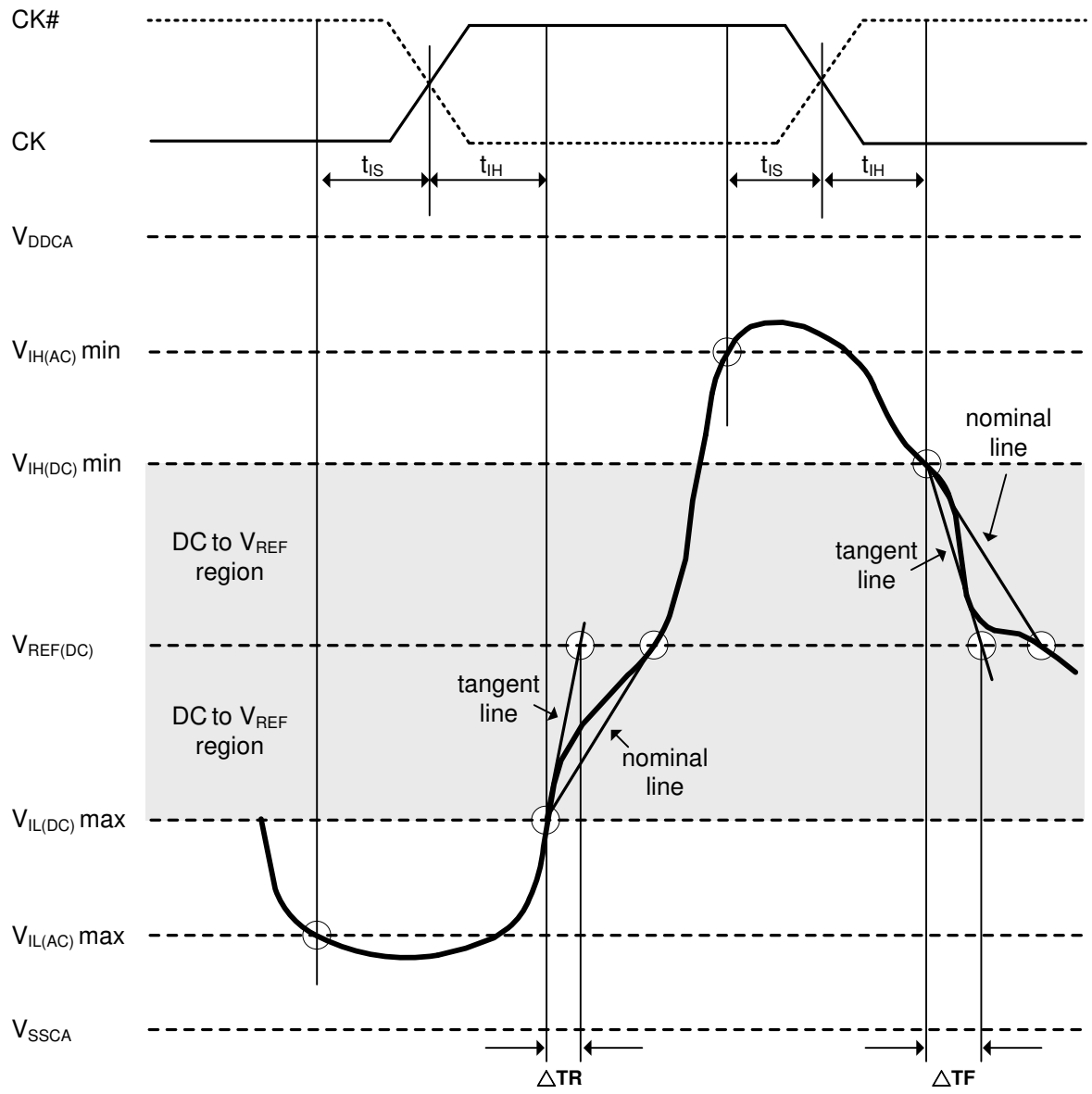
Figure 21. Illustration of nominal slew rate for hold time t_{IH} for CA and CS# with respect to clock



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[VIH(AC)\text{min} - VREF(DC)]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[VREF(DC) - VIH(AC)\text{max}]}{\Delta TF}$$

Figure 22. Illustration of tangent line for setup time t_{IS} for CA and CS# with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line[VREF(DC)} - \text{VIL(DC)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line[VIH(DC)min} - \text{VREF(DC)]}}{\Delta TF}$$

Figure 23. Illustration of tangent line for hold time t_{IH} for CA and CS# with respect to clock

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet $t_{DS(base)}$ and $t_{DH(base)}$ value to the Δt_{DS} and Δt_{DH} derating value respectively.
Example: t_{DS} (total setup time) = $t_{DS(base)}$ + Δt_{DS}.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between shaded $V_{REF(DC)}$ to AC region, use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded $V_{REF(DC)}$ to AC region, the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded DC level to $V_{REF(DC)}$ region, use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded DC to $V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value.

For a valid transition the input signal has to remain above/below $V_{IH}/V_{IL(AC)}$ for some time t_{VAC}.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table 58. Data Setup and Hold Base Values

Symbol	Reference	Data Rate			Unit
		1066	800	667	
$t_{DS(base)}$	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±220mV	-10	50	130	**ps**
$t_{DH(base)}$	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±130mV	80	140	220	**ps**

Notes: AC/DC referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS/DQS# slew rate.

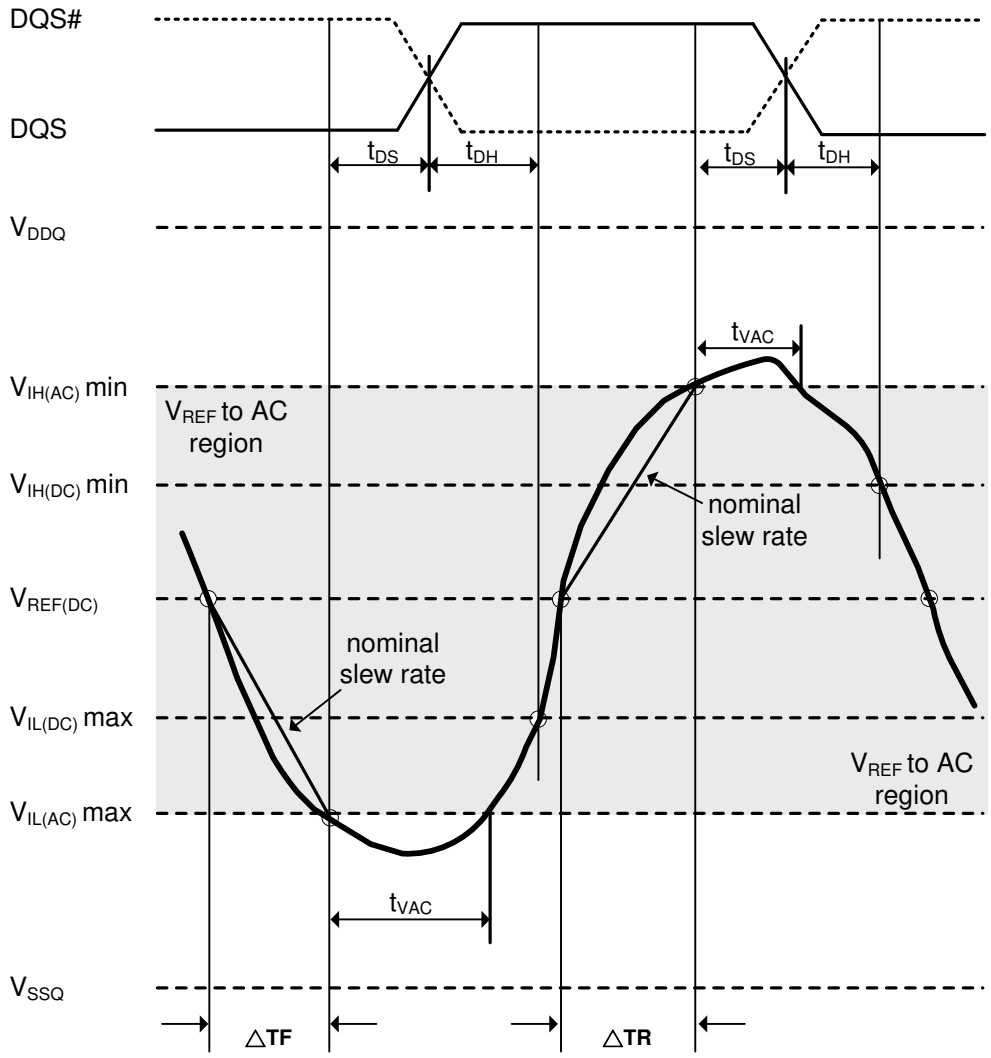
Table 59. Derating Values for AC/DC-Based tDS/tDH (AC220)

Δt_{DS}, Δt_{DH} derating in [ps] AC/DC based
AC220 Threshold -> $V_{IH(AC)}=V_{REF(DC)}$+220mV, $V_{IL(AC)}=V_{REF(DC)}$-220mV
DC130 Threshold -> $V_{IH(DC)}=V_{REF(DC)}$+130mV, $V_{IL(DC)}=V_{REF(DC)}$-130mV

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	**0**	**0**	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Table 60. Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition

Slew Rate [V/ns]	tVAC @ 220mV [ps]	
	min	max
>2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
<0.5	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{VREF(DC) - VIL(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{VIH(AC)min - VREF(DC)}{\Delta TR}$$

Figure 24. Illustration of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe

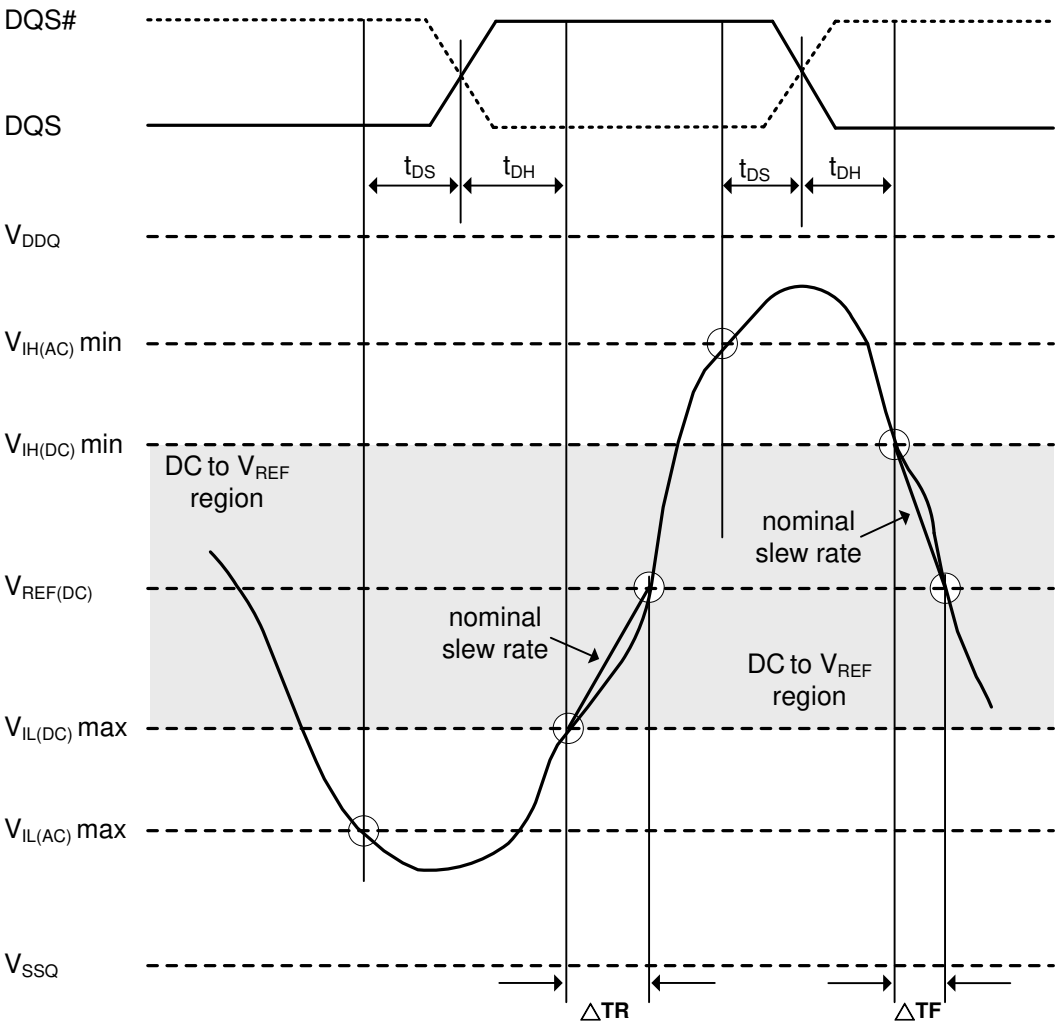
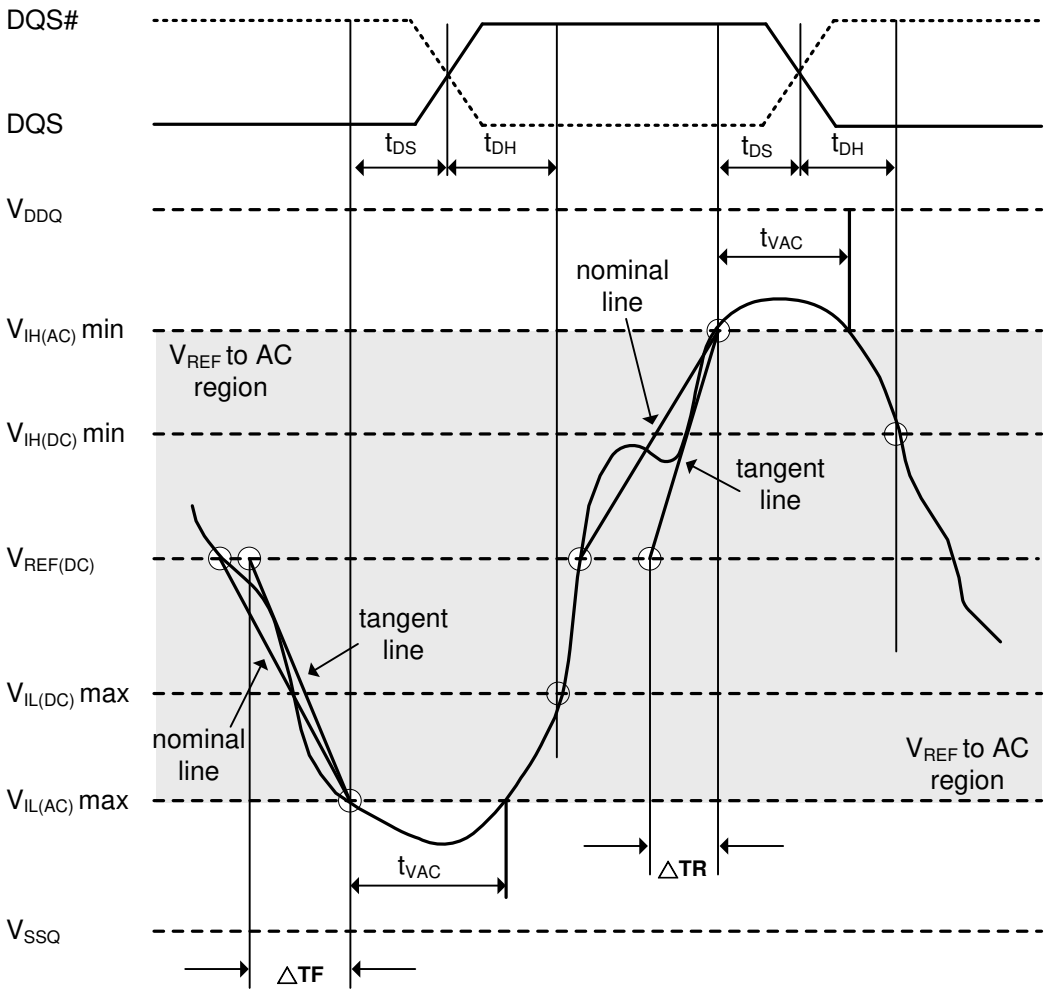


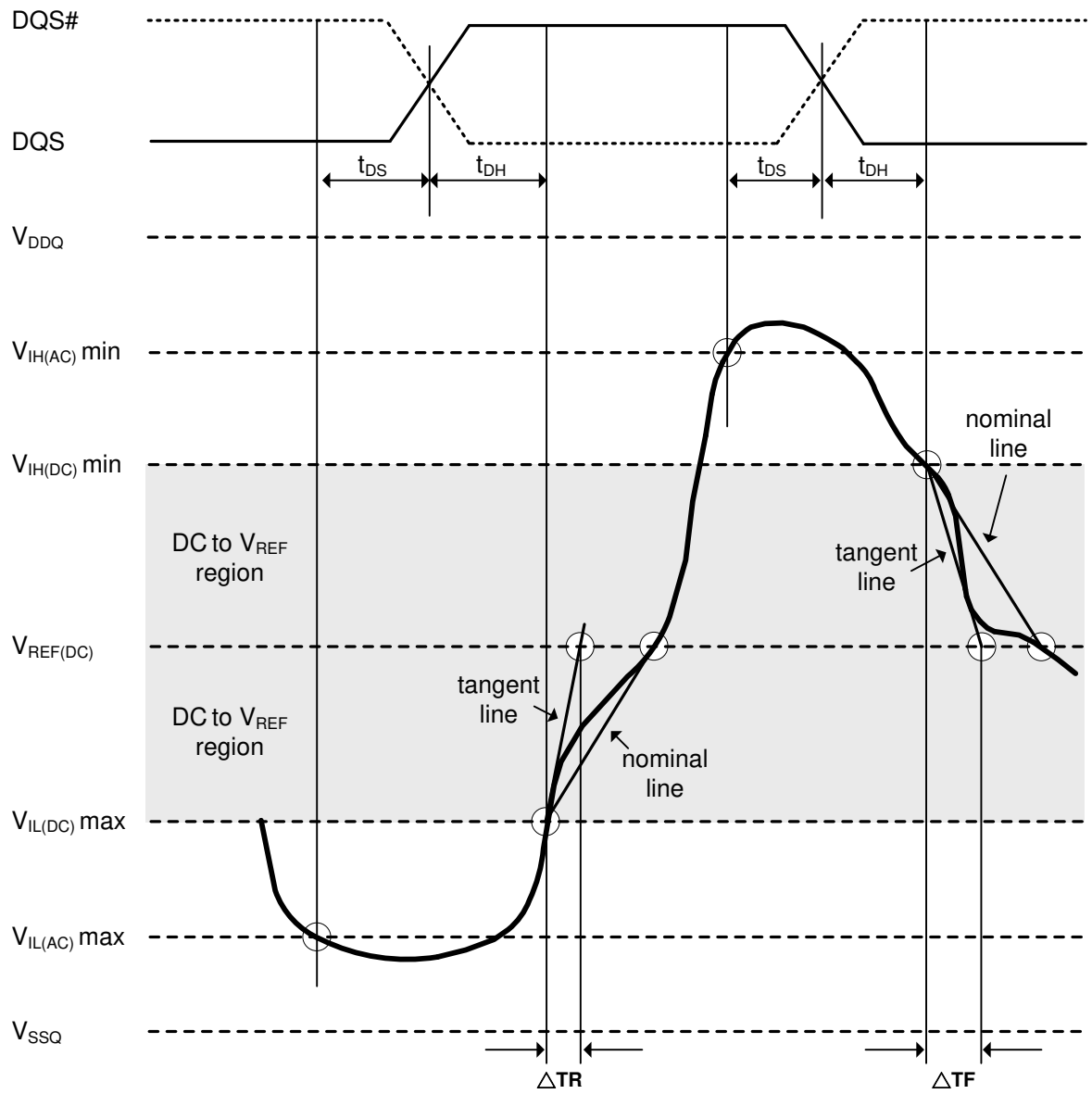
Figure 25. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[VIH(AC)\text{min} - VREF(DC)]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[VREF(DC) - VIH(AC)\text{max}]}{\Delta TF}$$

Figure 26. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

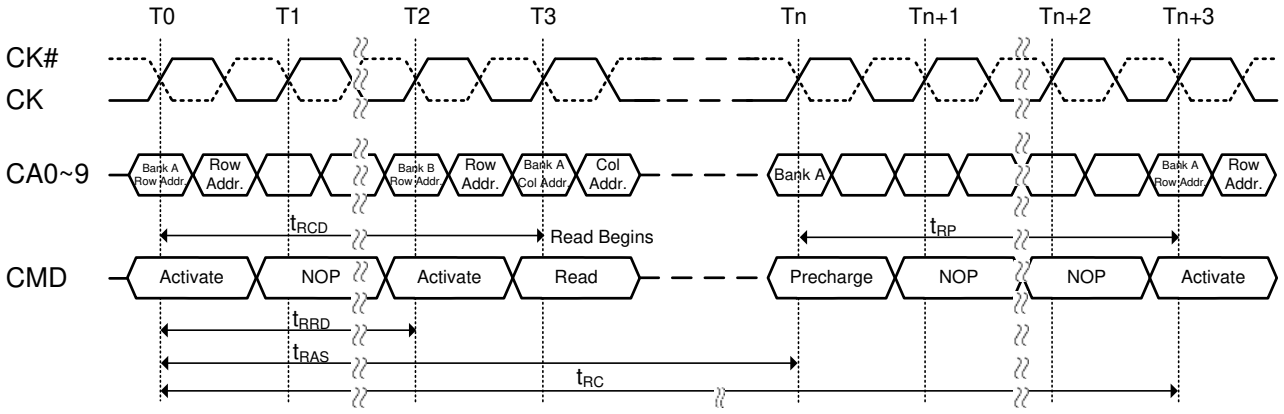


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line[VREF(DC)} - \text{VIL(DC)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line[VIH(DC)min} - \text{VREF(DC]}}{\Delta TF}$$

Figure 27. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

Timing Waveforms



Note:
A Precharge-all command uses tRPab timing, while a single-bank Precharge command uses tRPpb timing.
In this figure, tRP is used to denote either an all-bank Precharge or a single-bank Precharge.

Figure 28. Activate command cycle: t_{RCD} = 3, t_{RP} = 3, t_{RRD} = 2

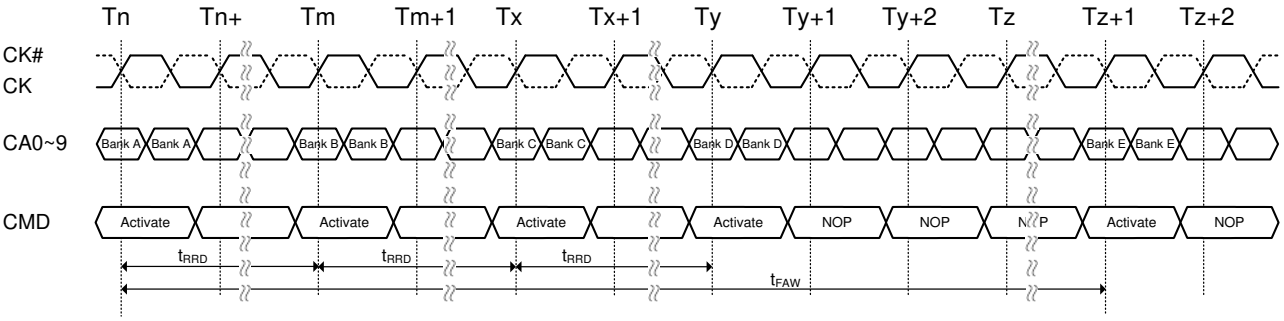
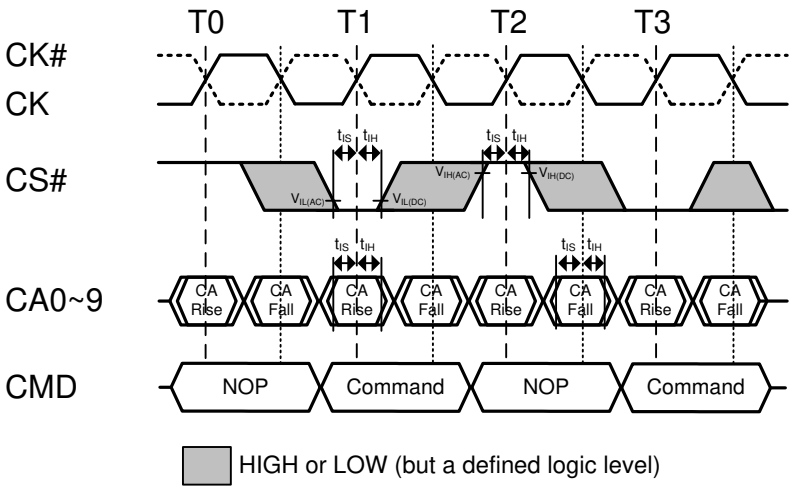
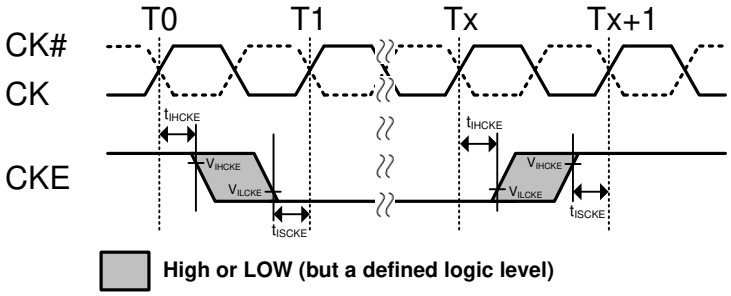


Figure 29. t_{FAW} Timing



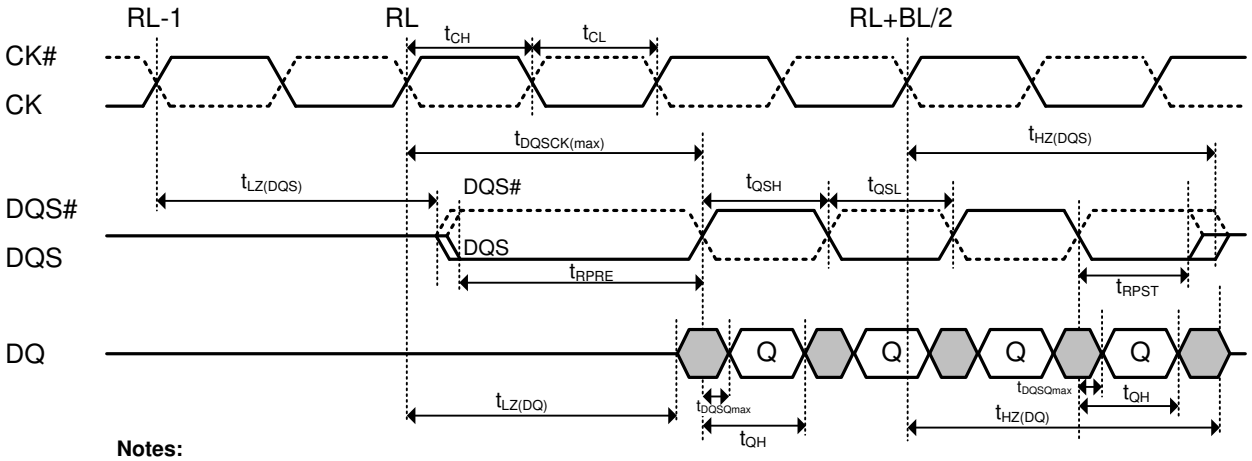
Notes:
Setup and hold conditions also apply to the CKE pin.
See section related to power down for timing diagrams related to the CKE pin.

Figure 30. Command Input Setup and Hold Timing



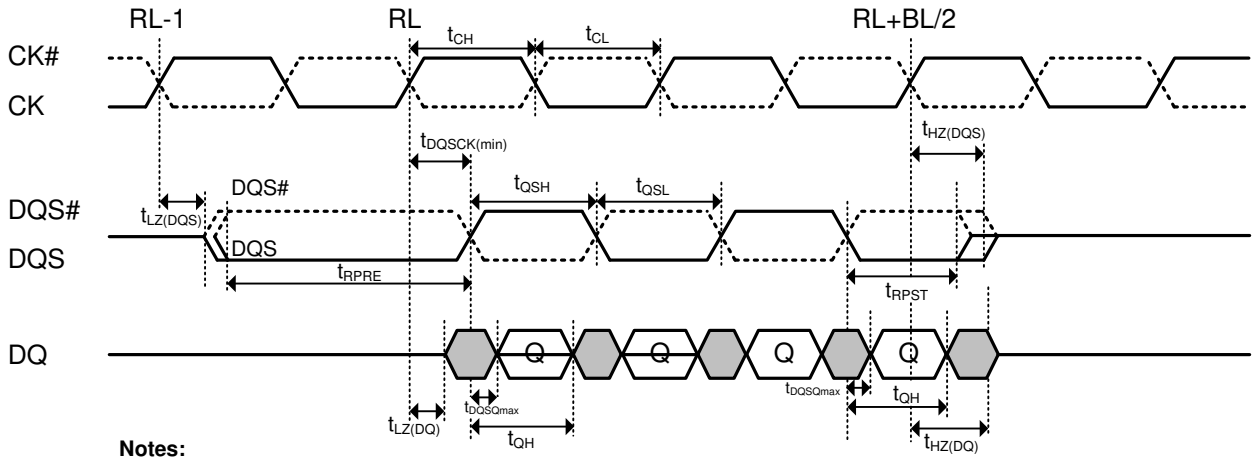
Notes:
1. After CKE is registered LOW, CKE signal level shall be maintained below V_{ILCKE} for t_{CKE} specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above V_{IHCKE} for t_{CKE} specification (HIGH pulse width).

Figure 31. CKE Input Setup and Hold Timing



Notes:
1. tDQSCK may span multiple clock periods.
2. An effective Burst Length of 4 is shown.

Figure 32. Data output (Read) timing ($t_{DQSCKmax}$)



Notes:
1. An effective Burst Length of 4 is shown.

Figure 33. Data output (Read) timing ($t_{DQSCKmin}$)

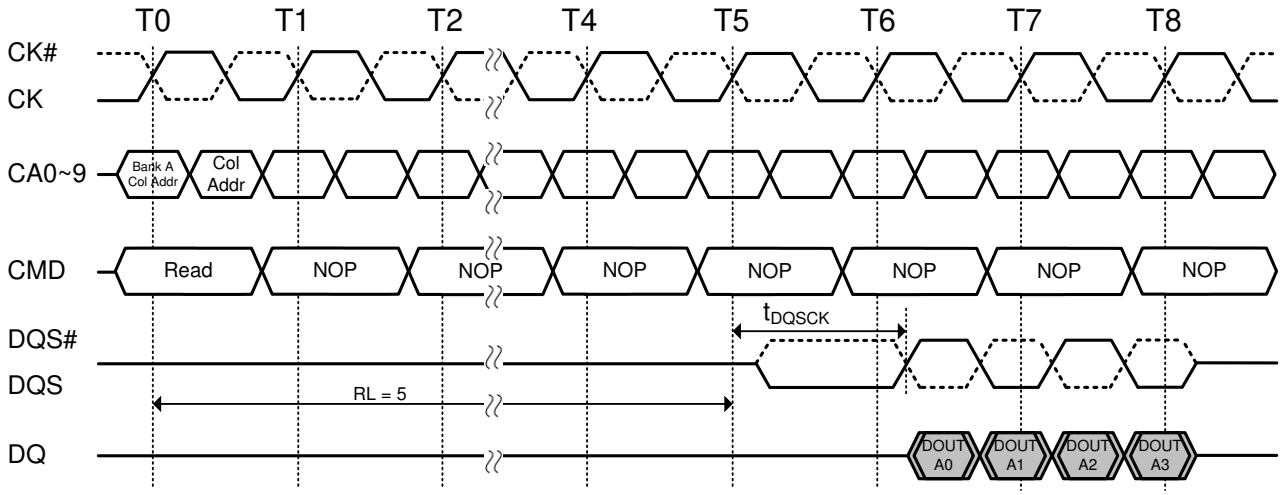


Figure 34. Burst Read: RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$

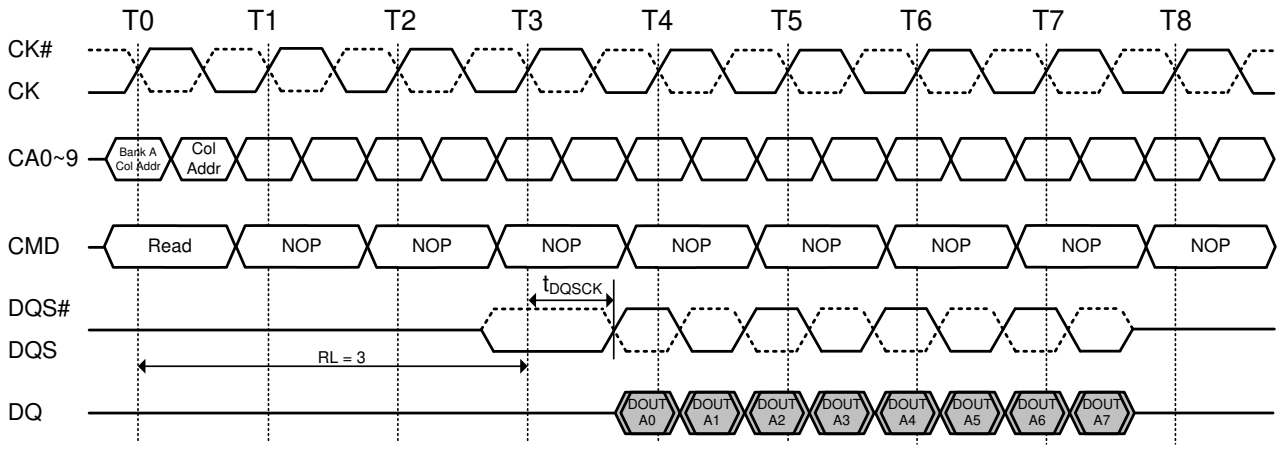
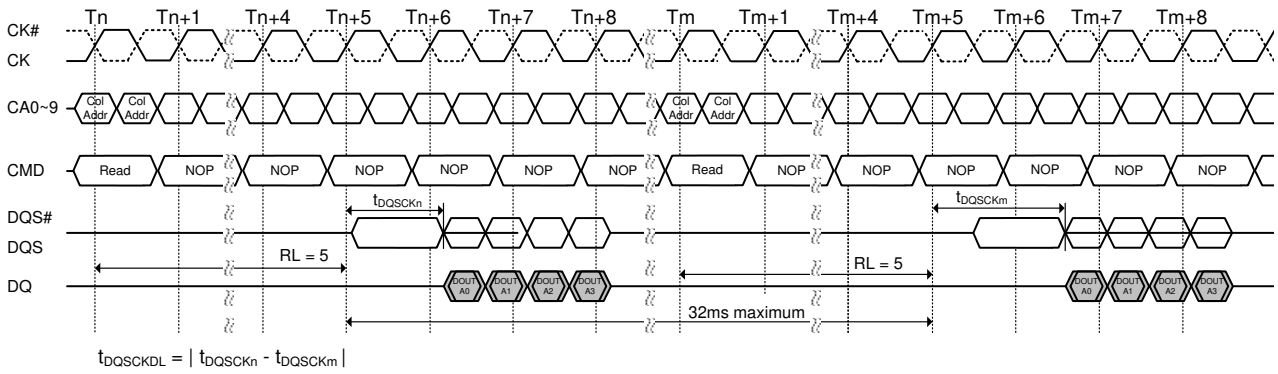
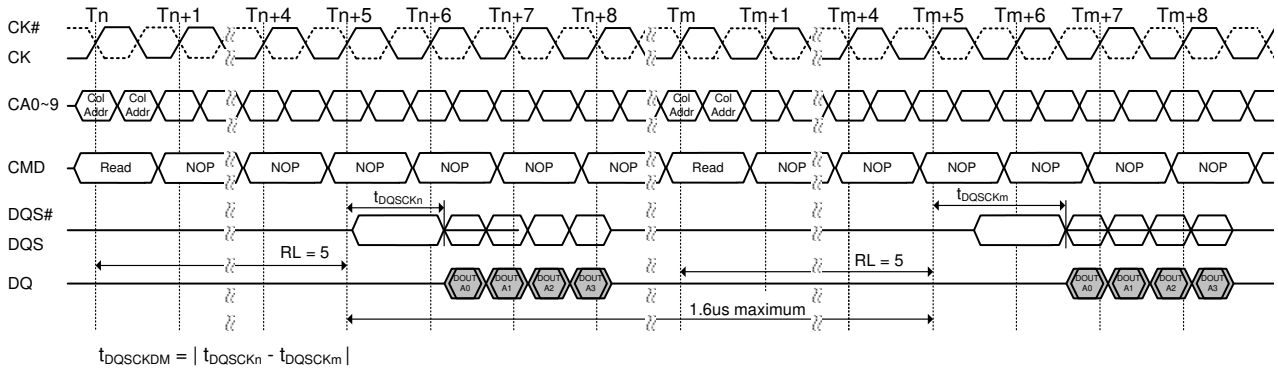


Figure 35. Burst Read: RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$



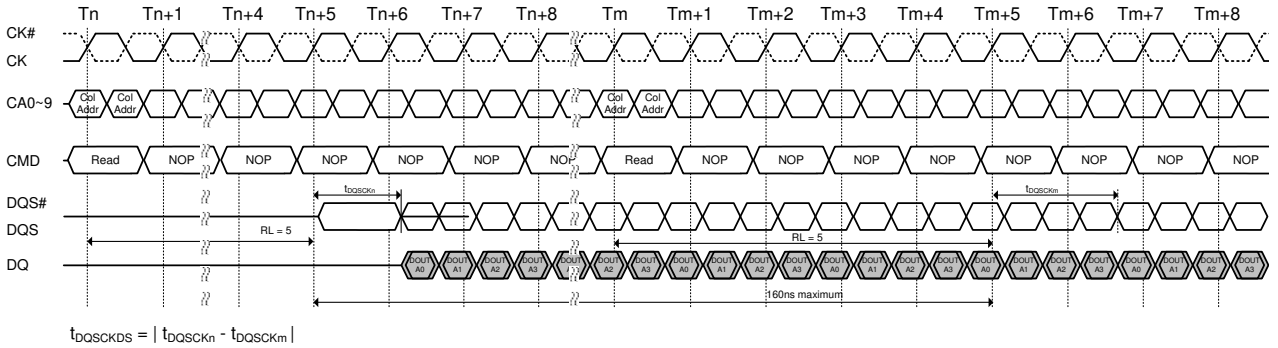
Notes:
1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn, tDQSCKm} pair within any 32ms rolling window.

Figure 36. $t_{DQSCKDL}$ timing



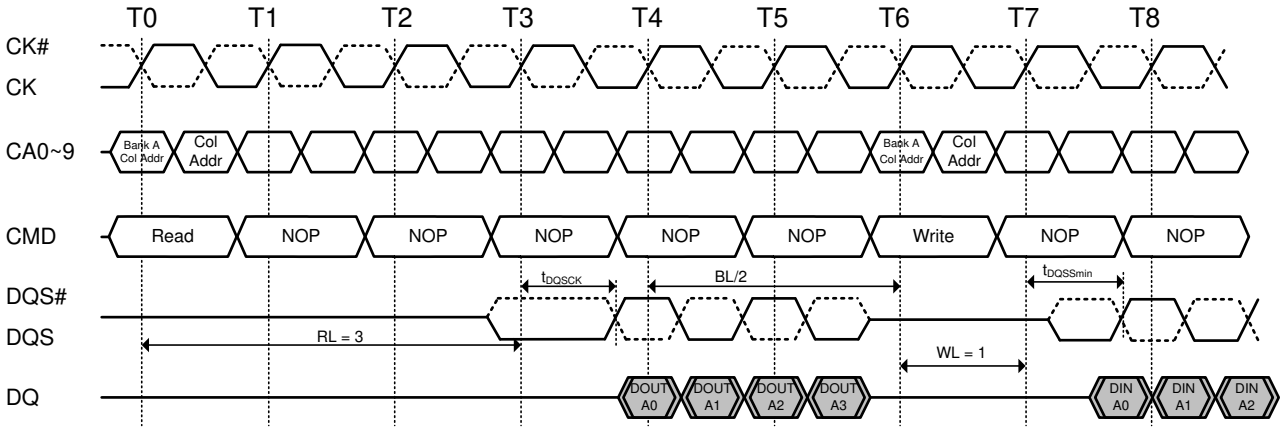
Notes:
1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn, tDQSCKm} pair within any 1.6us rolling window.

Figure 37. $t_{DQSCKDM}$ timing



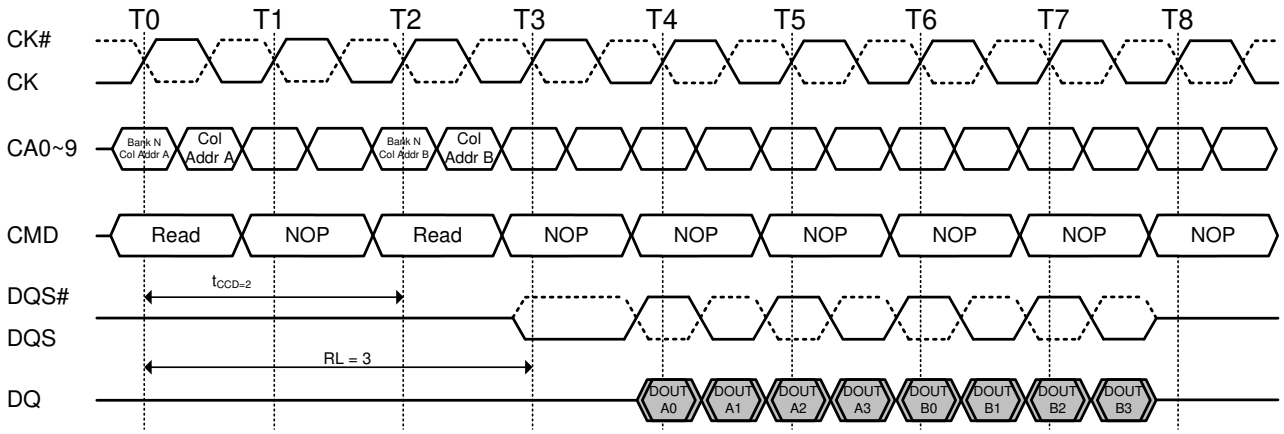
Notes:
1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn, tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.

Figure 38. $t_{DQSCKDS}$ timing



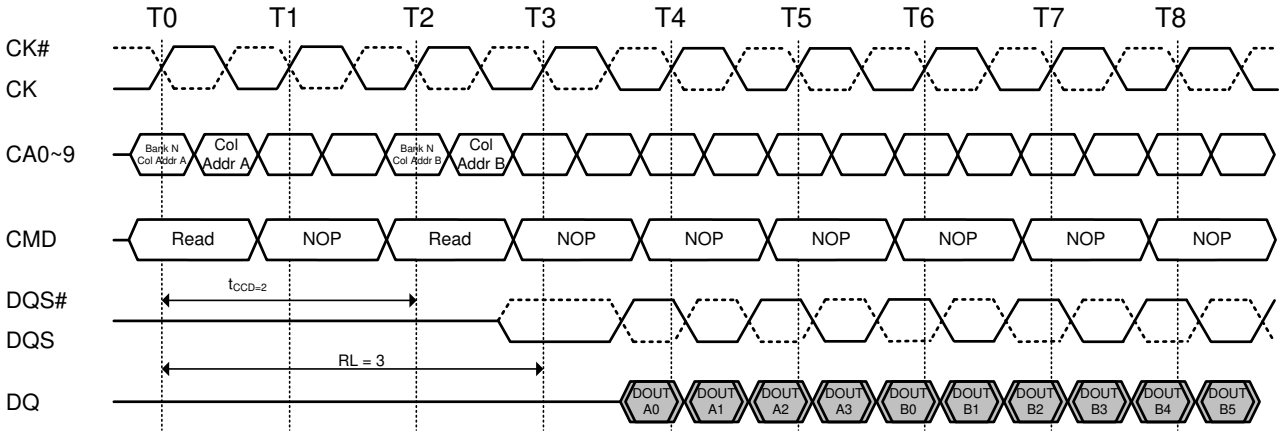
The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) And the Burst Length (BL). Minimum read to write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as "BL" to calculate the minimum read to write delay.

Figure 39. Burst read followed by burst write: RL = 3, WL = 1, BL = 4



The seamless burst Read operation is supported by enabling a Read command at every fourth clock cycle for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL = 16 operation.

Figure 40. Seamless Burst Read: RL = 3, BL = 4, t_{CCD} = 2



Notes:
1. For LPDDR2 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that t_{CCD} is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Figure 41. Read burst interrupt example: RL = 3, BL = 8, t_{CCD} = 2

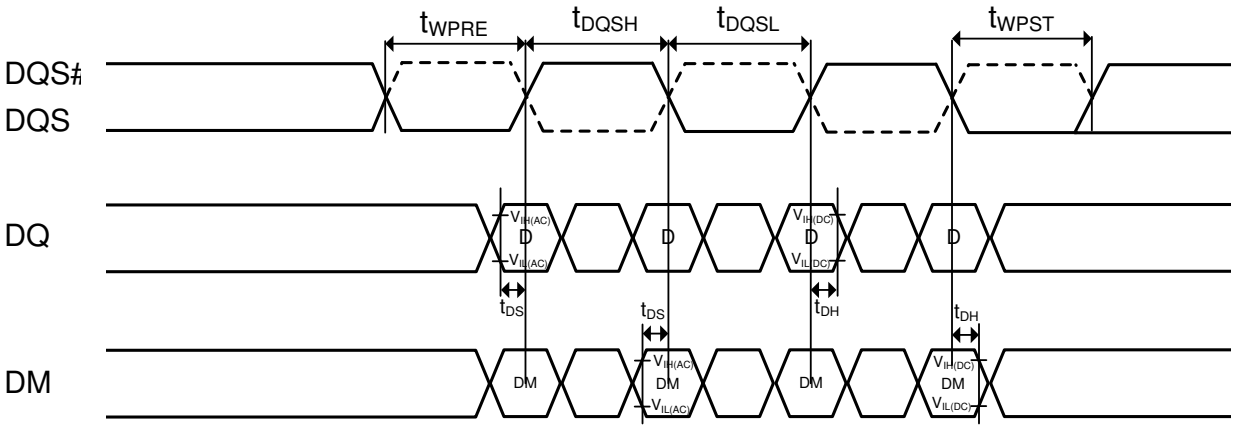


Figure 42. Data input (write) timing

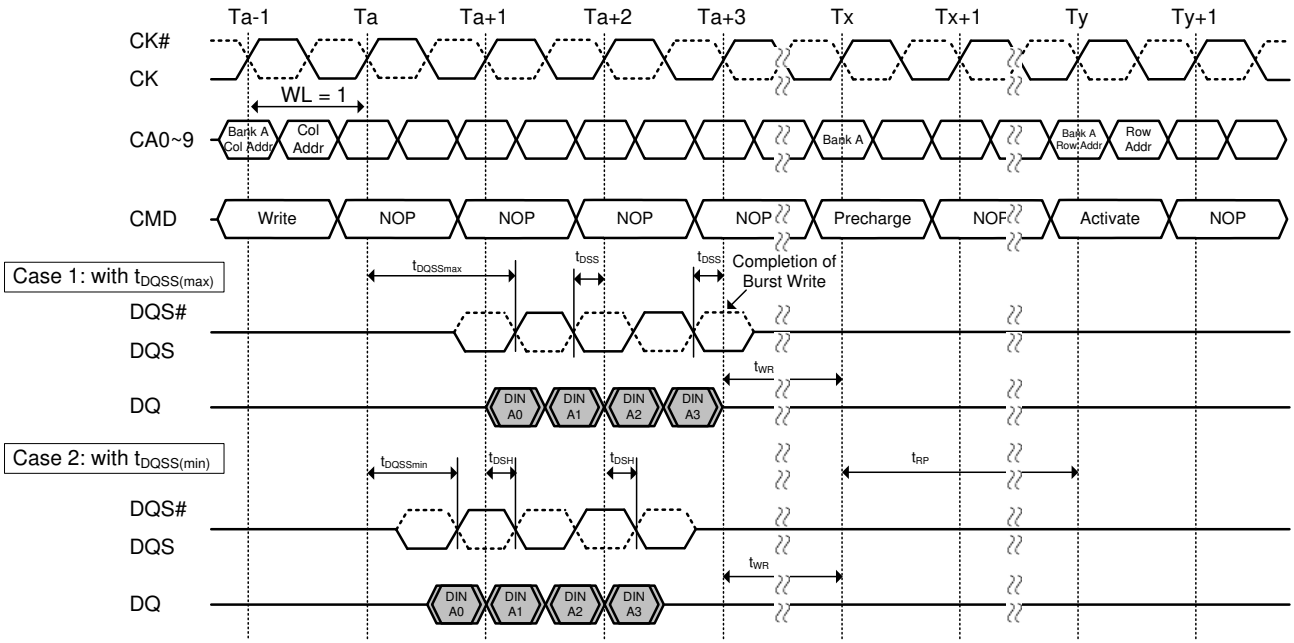
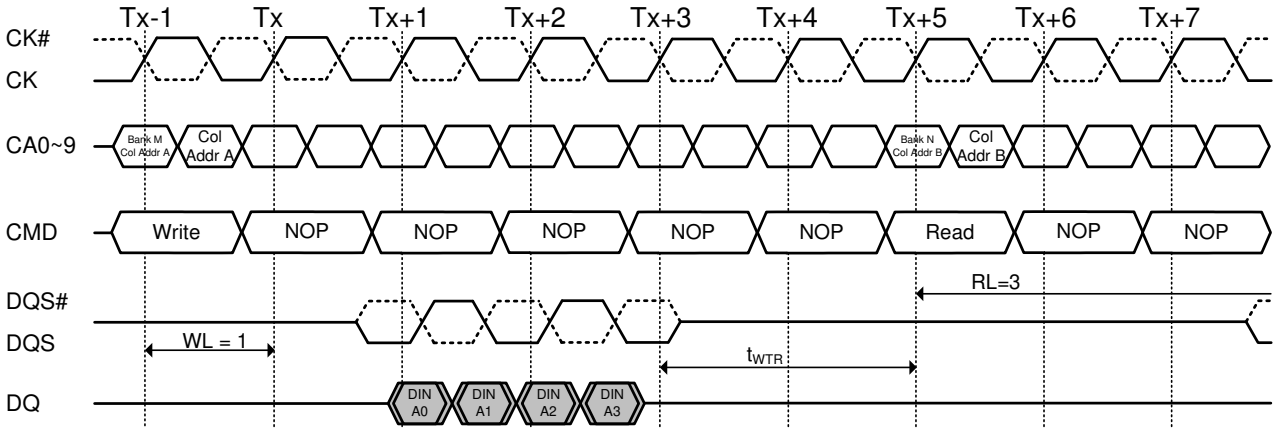
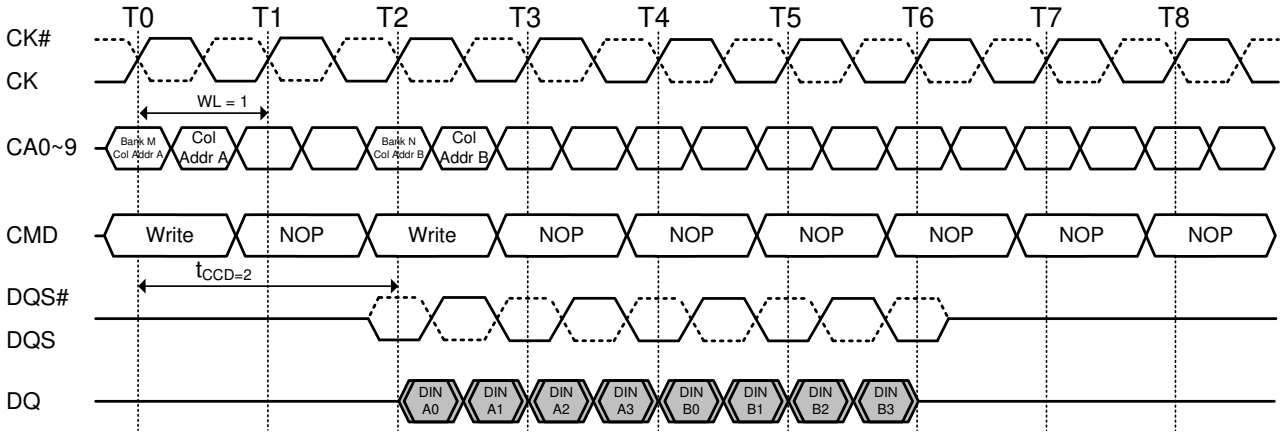


Figure 43. Burst Write: WL = 1, BL = 4



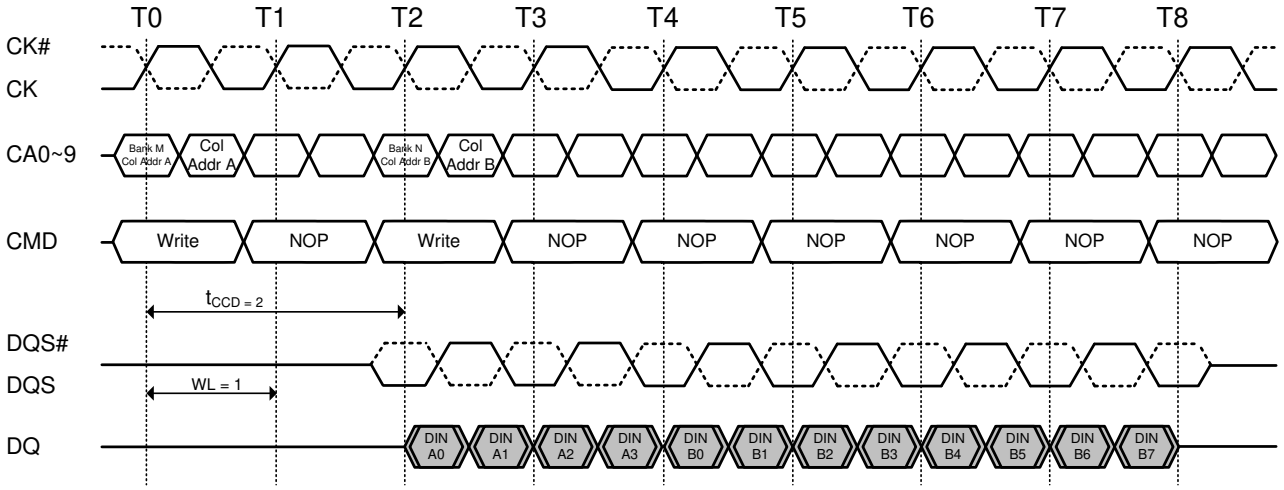
Notes:
1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
2. t_{WTR} starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as "BL" to calculate the minimum write to read delay.

Figure 44. Burst Write Followed By Burst Read: RL=3, WL = 1, BL = 4



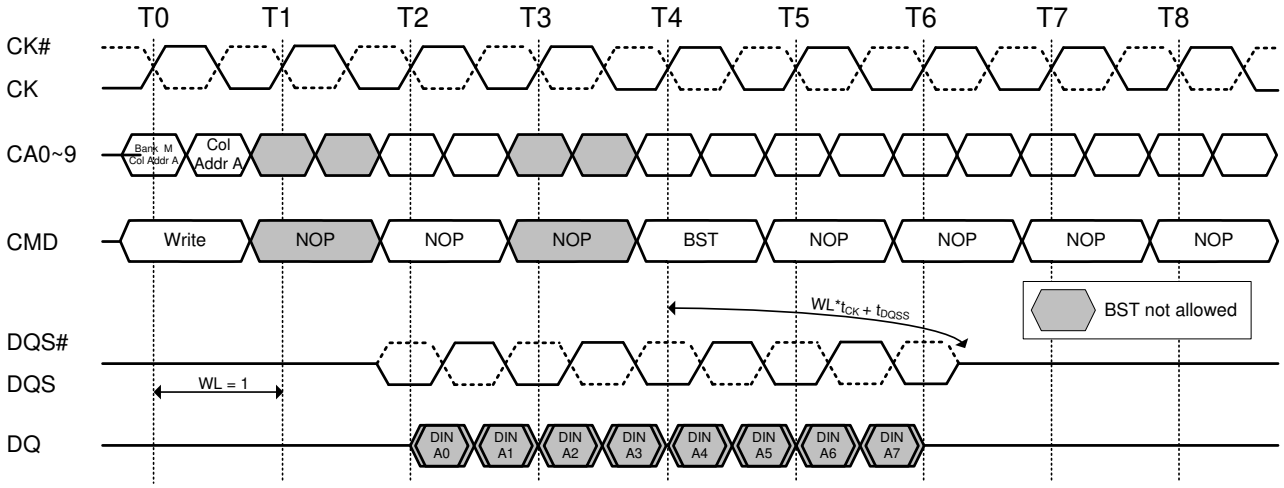
Notes:
The seamless burst write operation is supported by enabling a write command Every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 45. Seamless burst write: WL = 1, BL = 4, t_{CCD} = 2



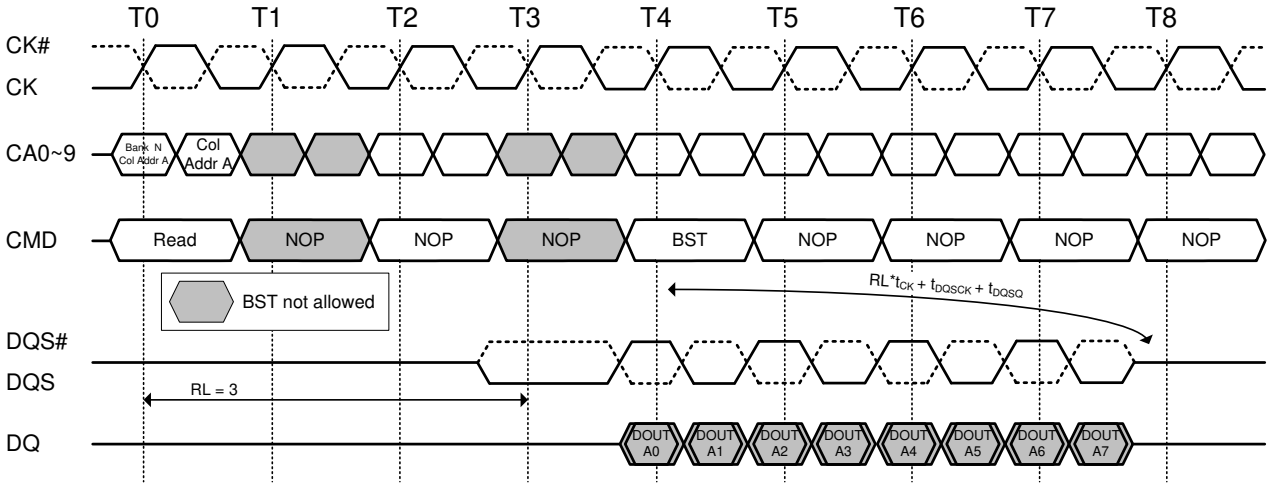
Notes:
1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that $t_{CCD(min)}$ is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

Figure 46. Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2



Notes:
1. The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write Command.

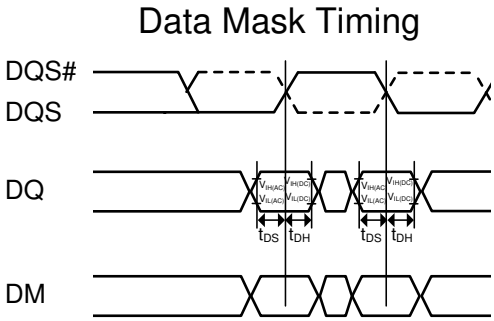
Figure 47. Burst Write truncated by BST: WL = 1, BL = 16



Notes:

1. The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Figure 48. Burst Read truncated by BST: RL=3, BL = 16



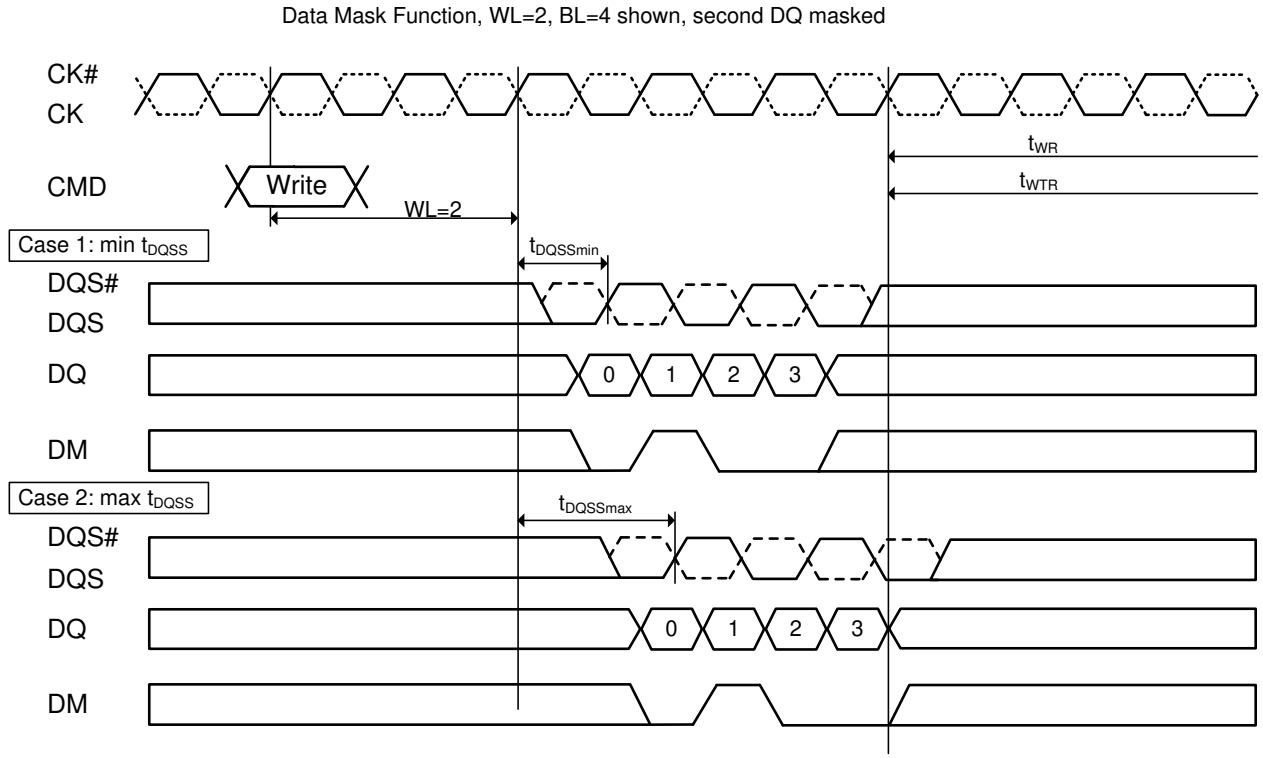


Figure 49. Write data mask

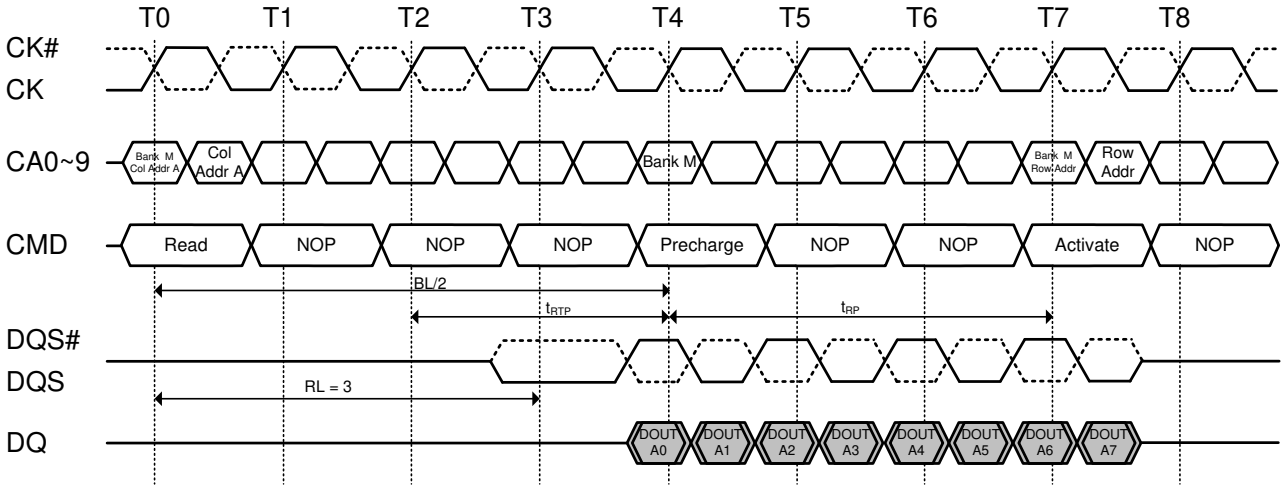


Figure 50. Burst read followed by Precharge: RL = 3, BL = 8, RU($t_{RTP(min)}/t_{CK}$) = 2

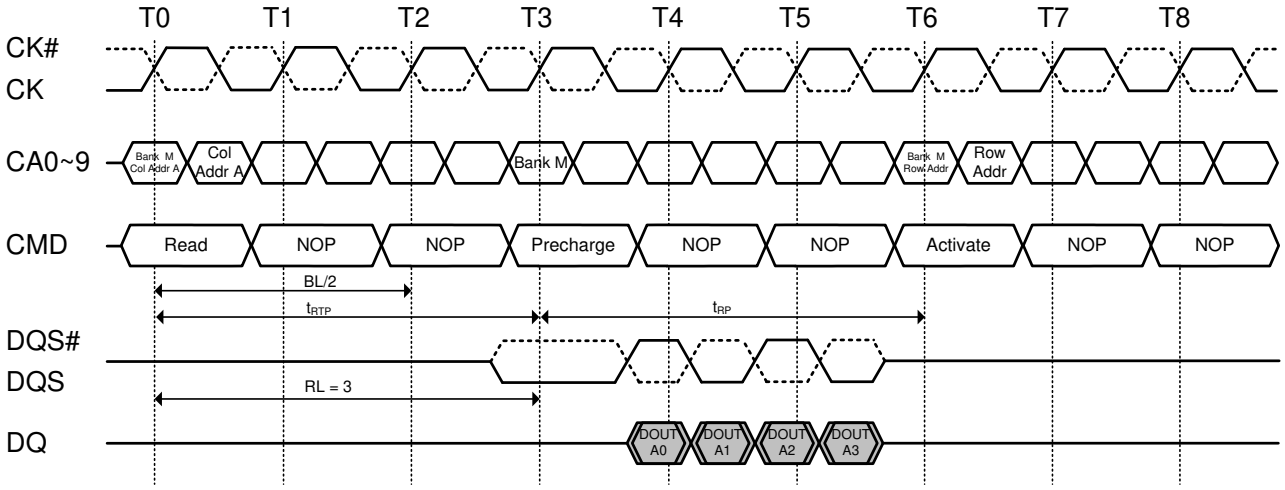


Figure 51. Burst read followed by Precharge: RL = 3, BL = 4, RU($t_{RTP(min)}/t_{CK}$) = 3

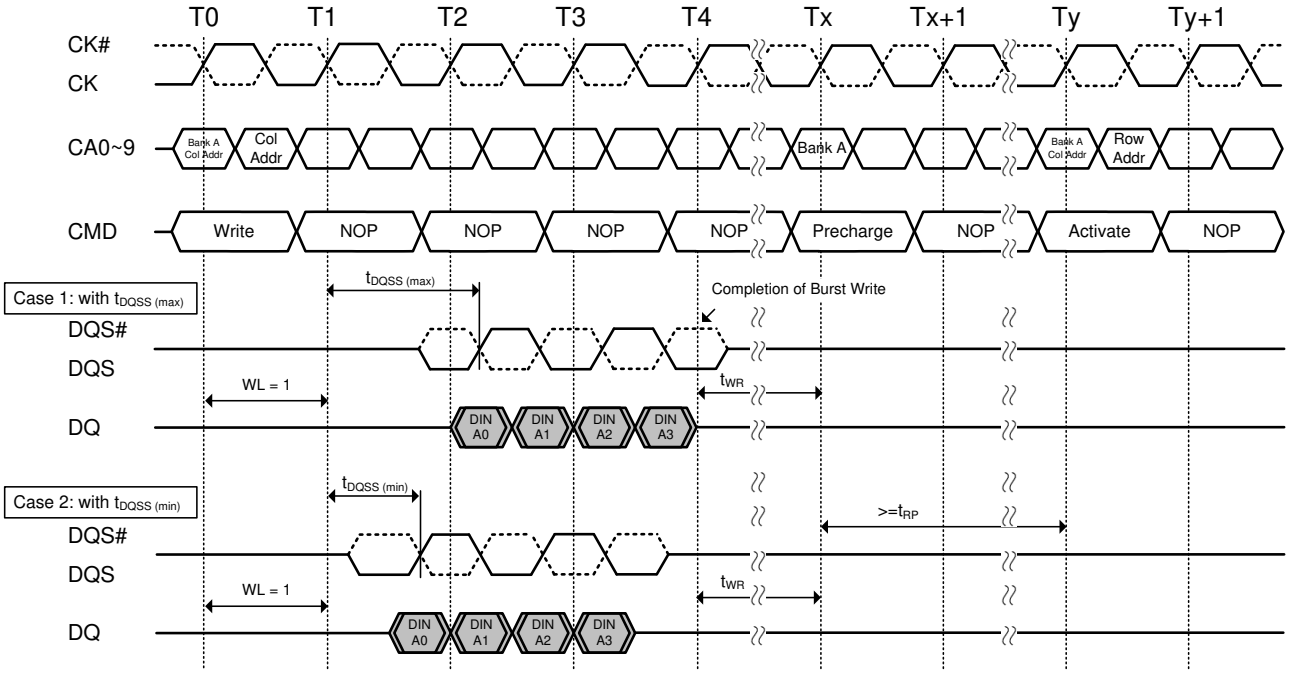


Figure 52. Burst write followed by precharge: WL = 1, BL = 4

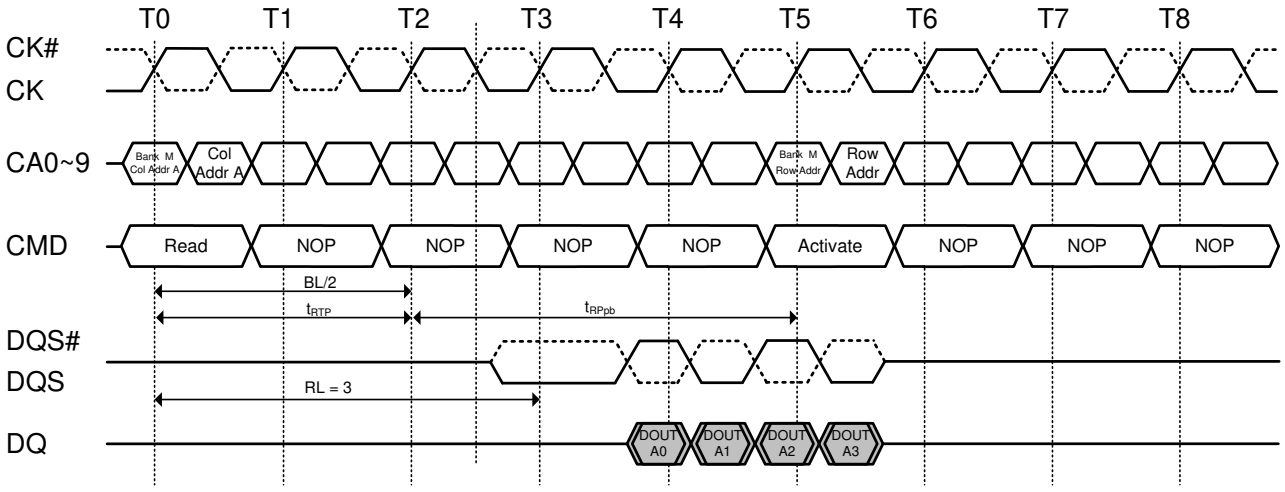


Figure 53. Burst read with Auto-Precharge: RL = 3, BL = 4, RU($t_{RTP(min)}/t_{CK}$) = 2

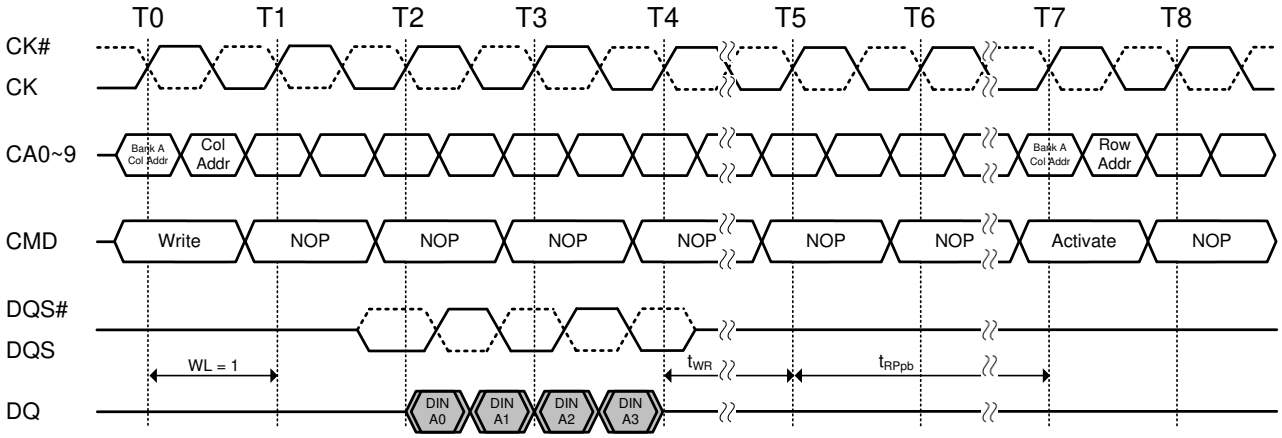


Figure 54. Burst write w/Auto Precharge: WL = 1, BL = 4

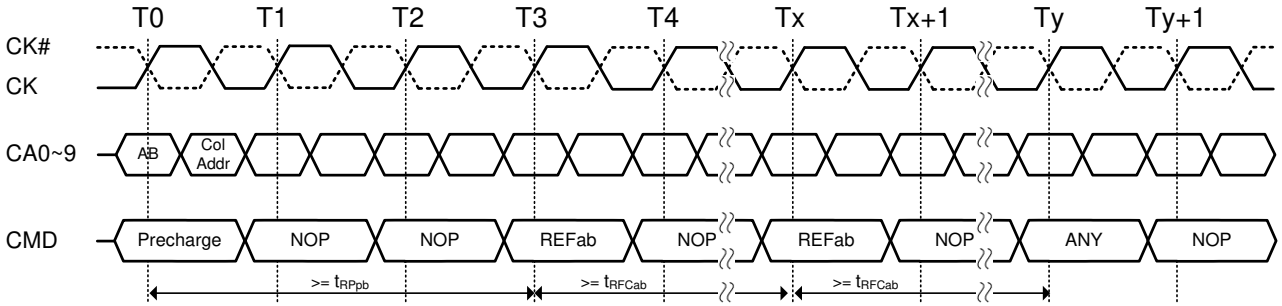
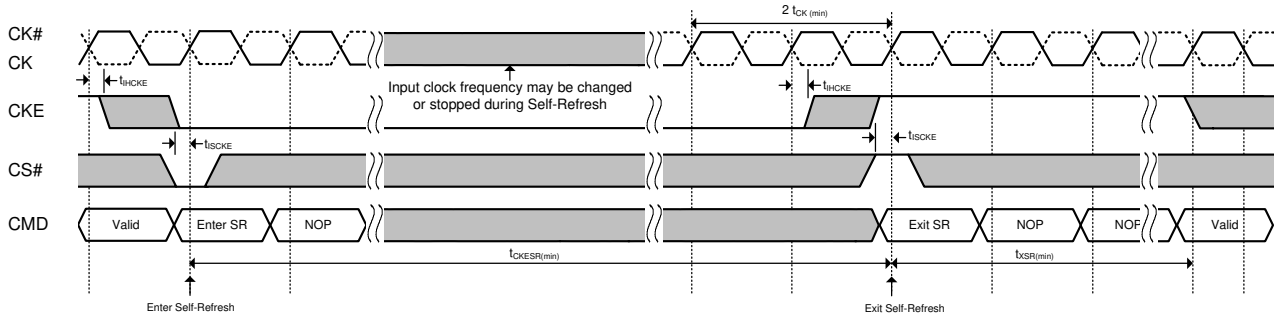
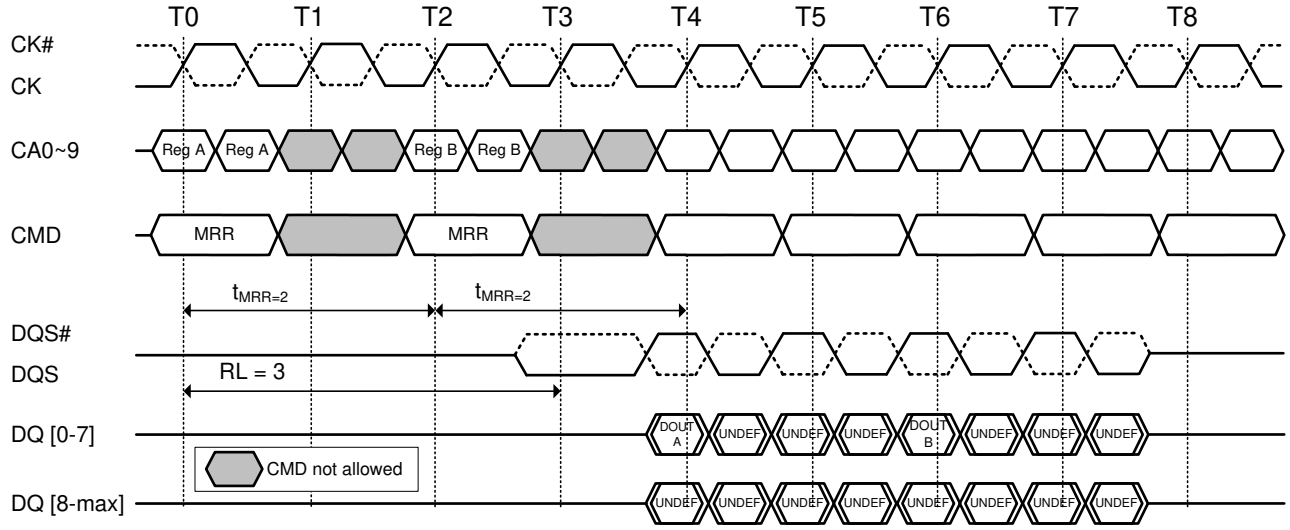


Figure 55. All Bank Refresh Operation



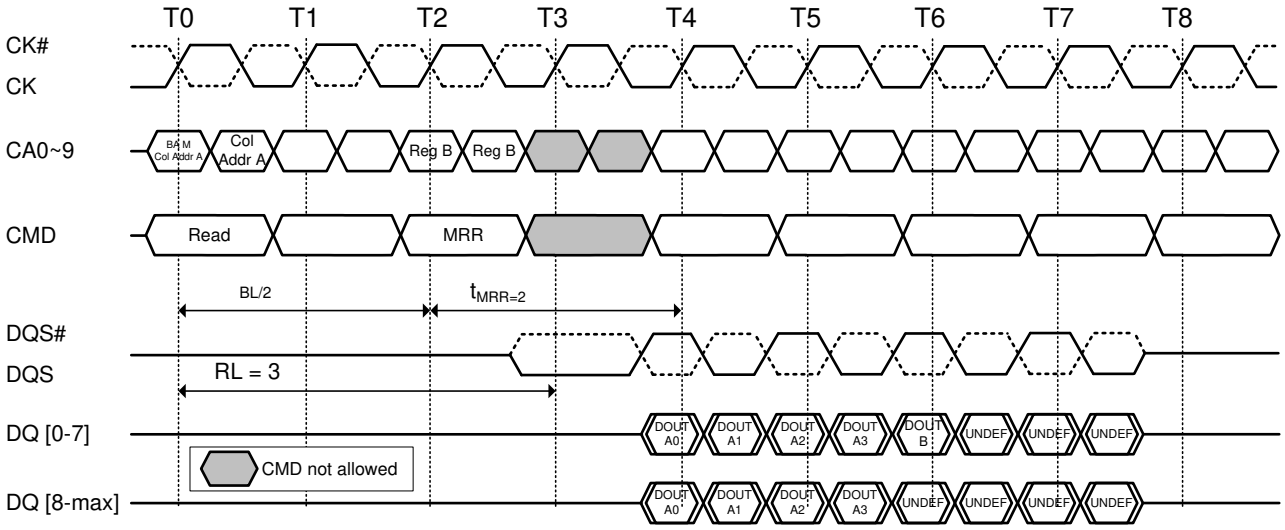
Notes:
1. Input clock frequencY may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
3. t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after t_{XSR} is satisfied. NOPs shall be issued during t_{XSR}.

Figure 56. Self-Refresh Operation



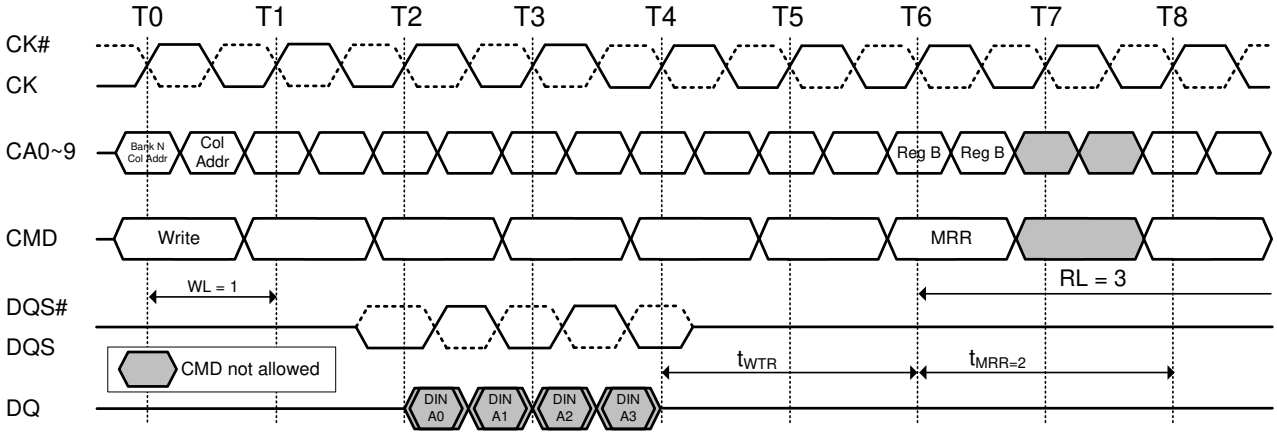
Notes:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + 4/2 + 1 clock cycles.

Figure 57. Mode Register Read timing example: RL = 3, t_{MRR} = 2



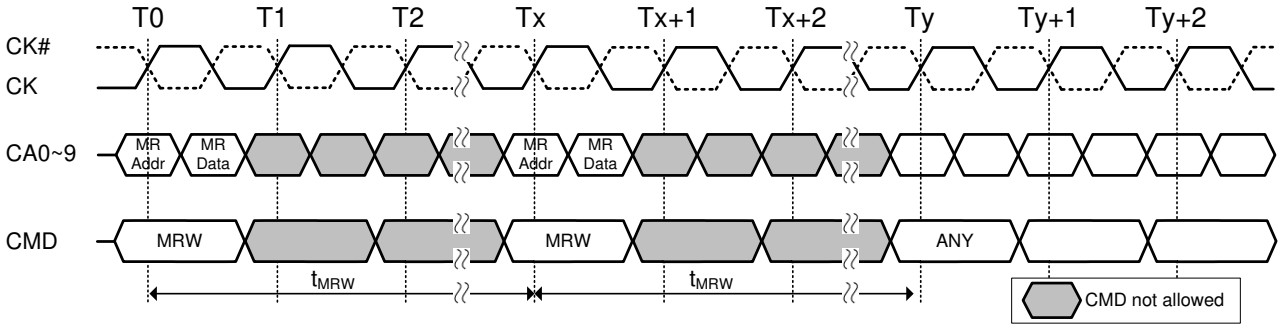
Notes:
1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

Figure 58. Read to MRR timing example: RL = 3, t_{MRR} = 2



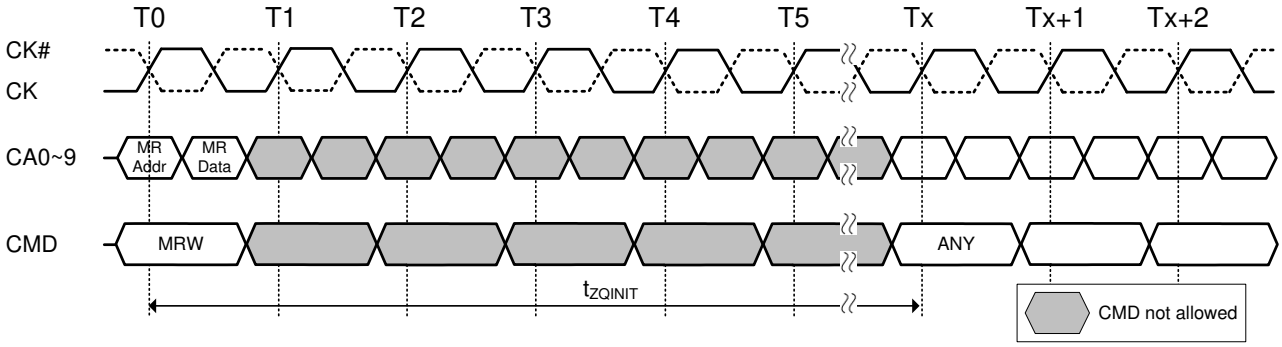
Notes:
1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

Figure 59. Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4



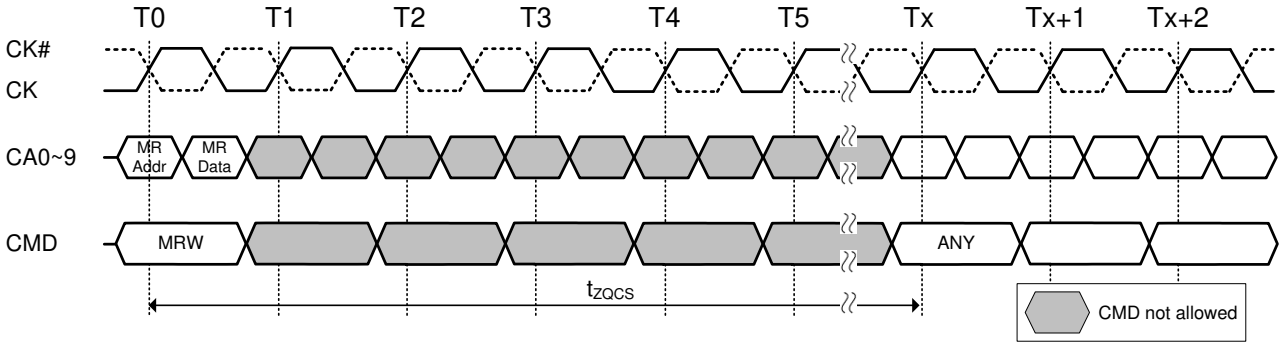
Notes:
1. The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

Figure 60. Mode Register Write timing example: RL = 3, t_{MRW} = 5



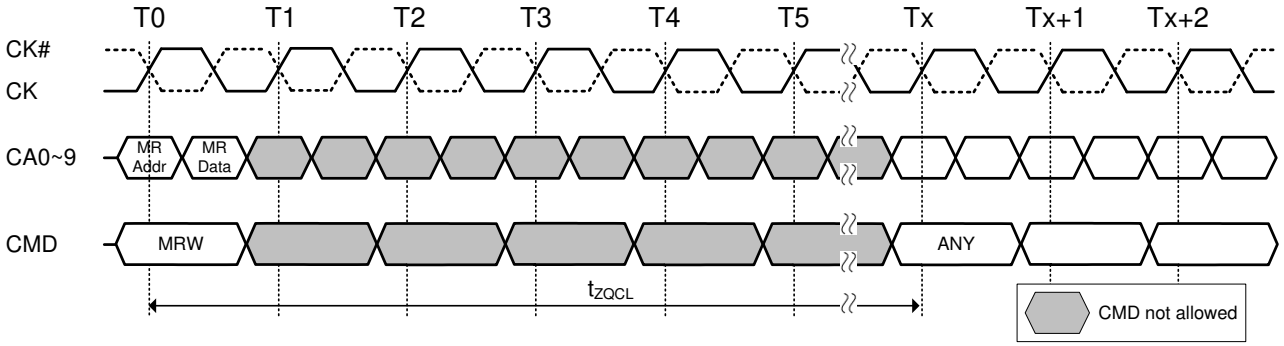
Notes:
1. The ZQ Calibration Initialization period is t_{ZQINIT}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 61. ZQ Calibration Initialization Timing



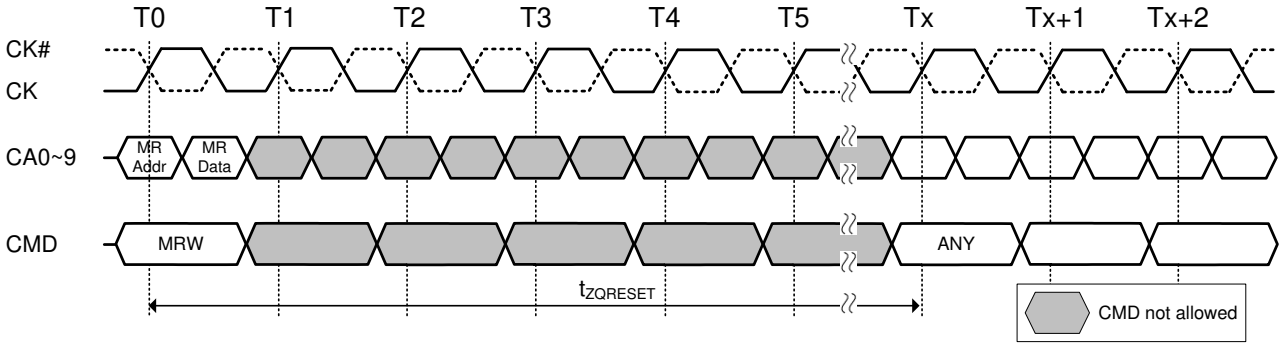
Notes:
1. The ZQ Calibration Short period is t_{ZQCS}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 62. ZQ Calibration Short Timing



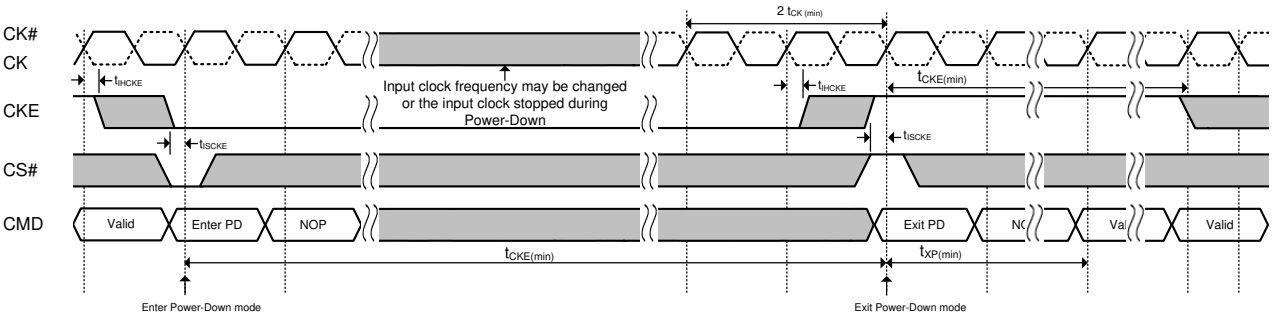
Notes:
1. The ZQ Calibration Long period is t_{ZQCL}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 63. ZQ Calibration Long Timing



Notes:
1. The ZQ Calibration Reset period is $t_{ZQRESET}$. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure 64. ZQ Calibration Reset Timing



Notes:
1. Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure 65. Basic power down entry and exit timing diagram

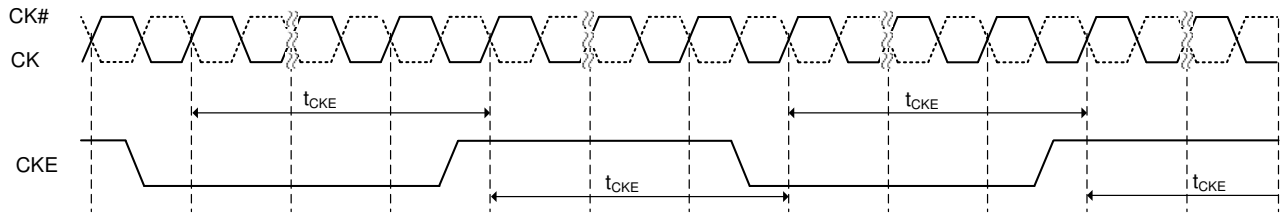
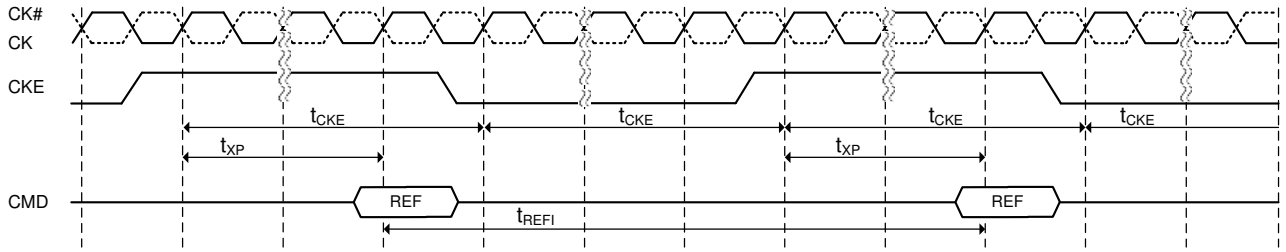
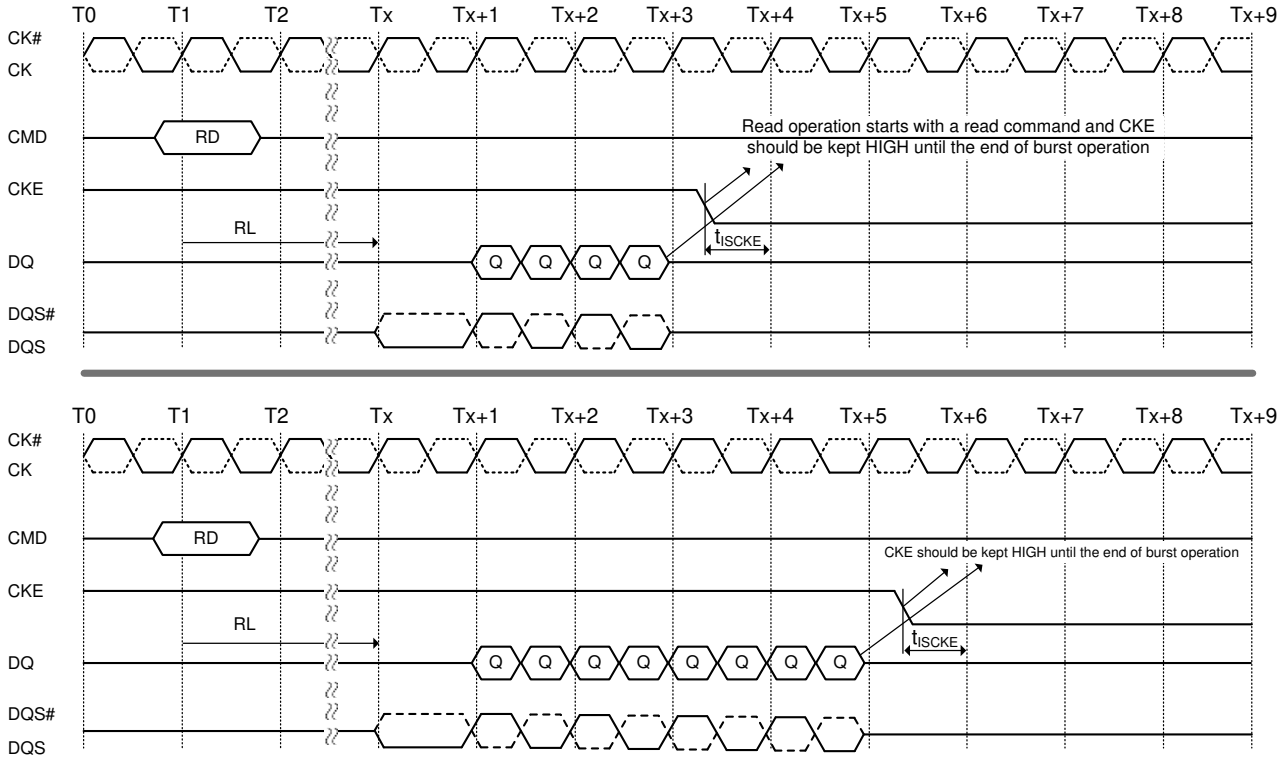


Figure 66. CKE-Intensive Environment



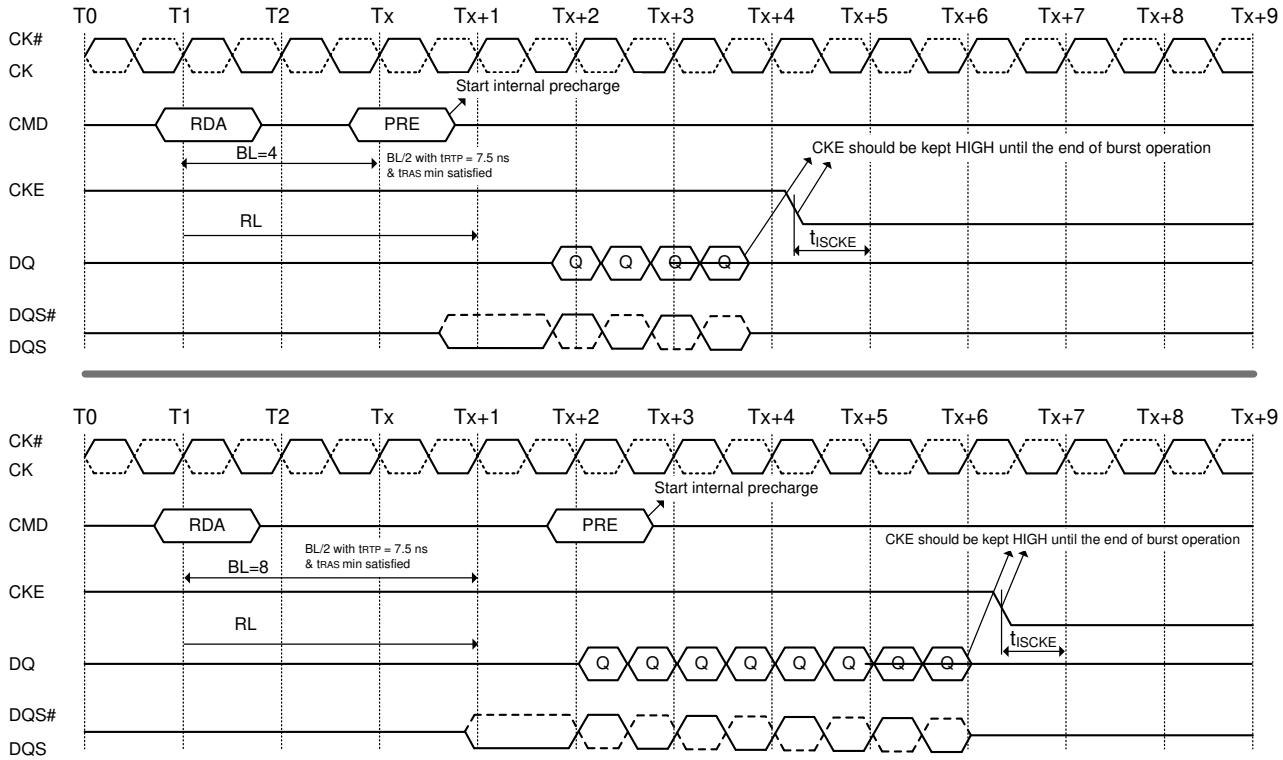
Note:
The pattern shown above can repeat over a long period of tiMe. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift.

Figure 67. Refresh to Refresh Timing in CKE Intensive Environments



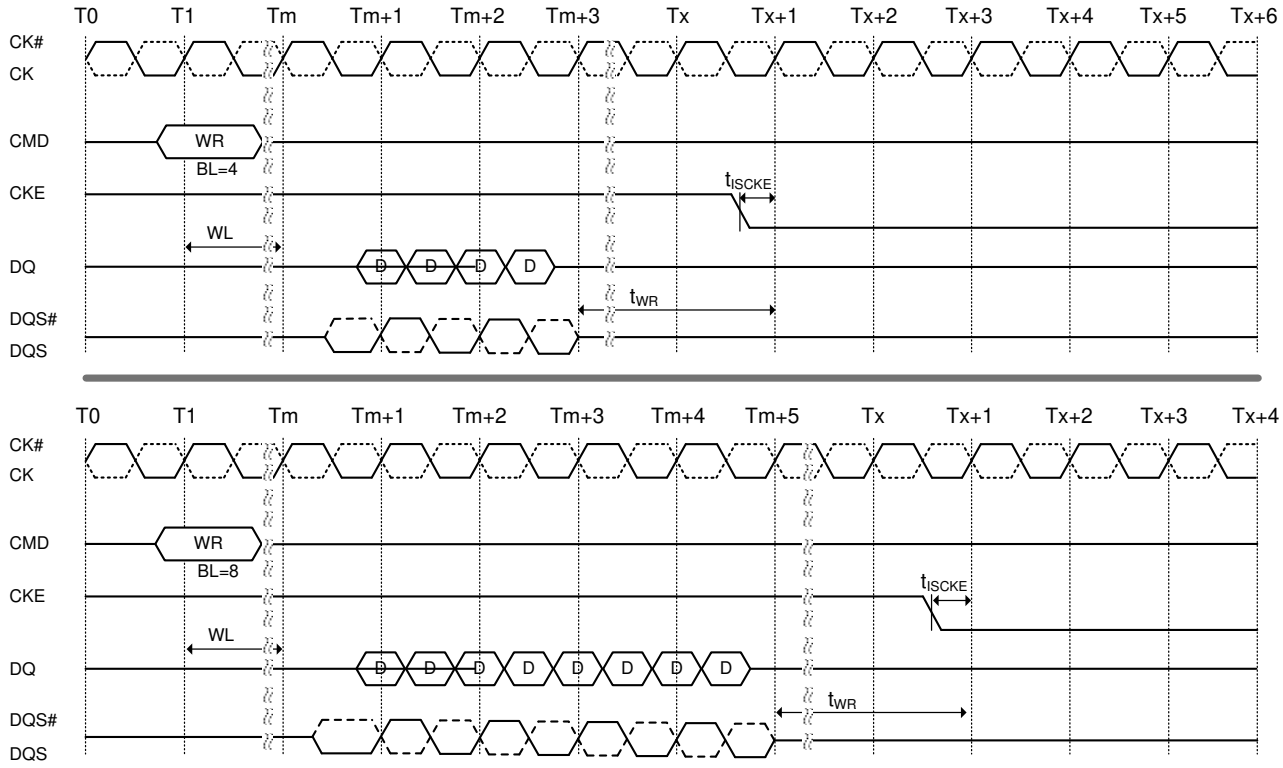
Note:
1. CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}$/t_{CK}) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Figure 68. Read to power-down entry



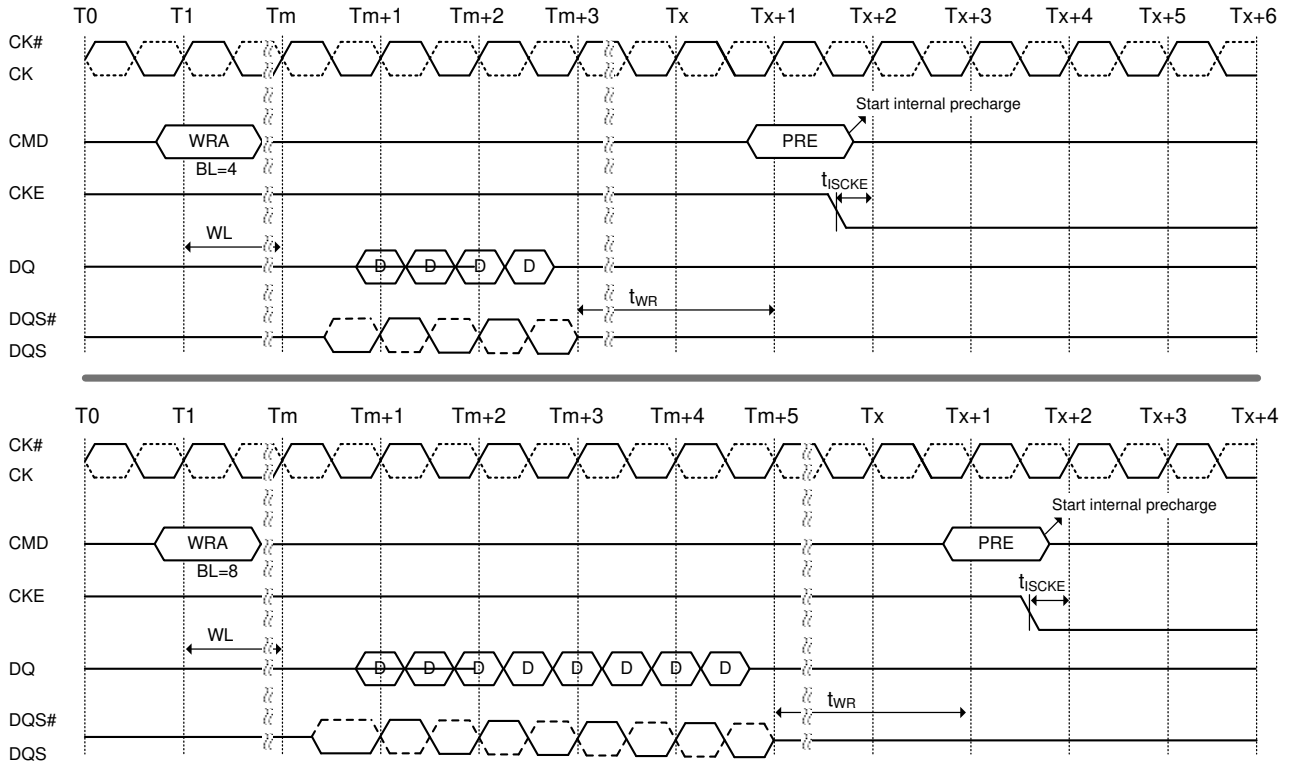
Note:
1. CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Figure 69. Read with autoprecharge to power-down entry



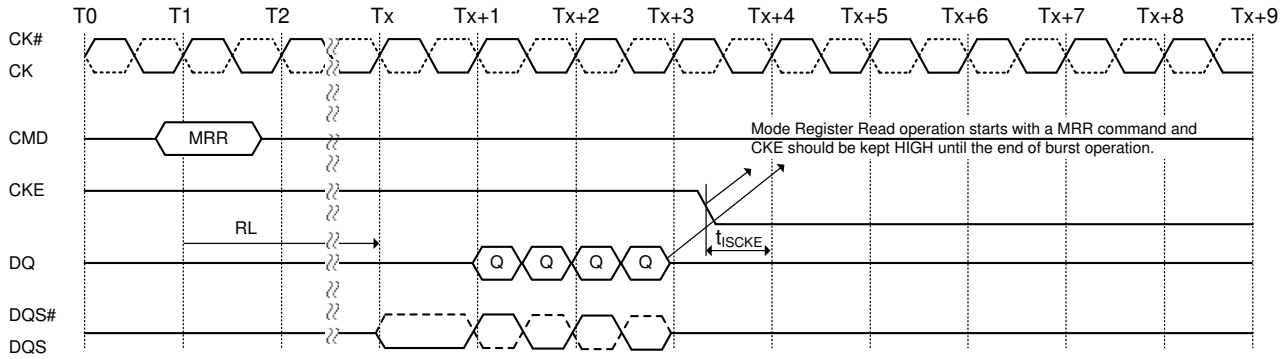
Note:
1. CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) clock cycles after the clock on which the write command is registered.

Figure 70. Write to power-down entry



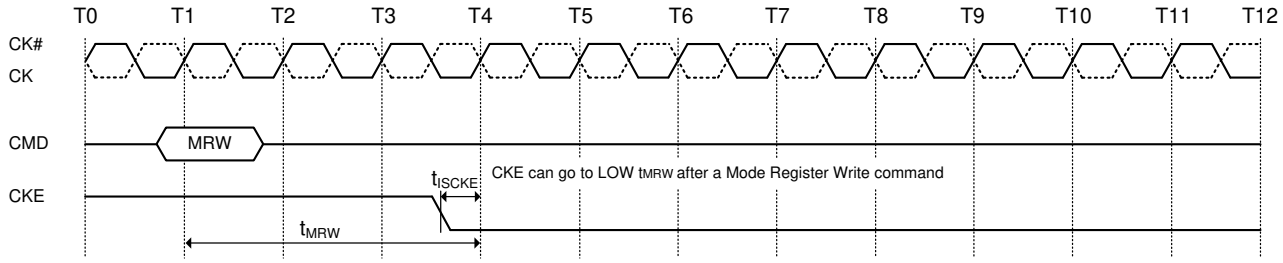
Note:
1. CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1 clock cycles after the clock on which the write command is registered.

Figure 71. Write with autoprecharge to power-down entry



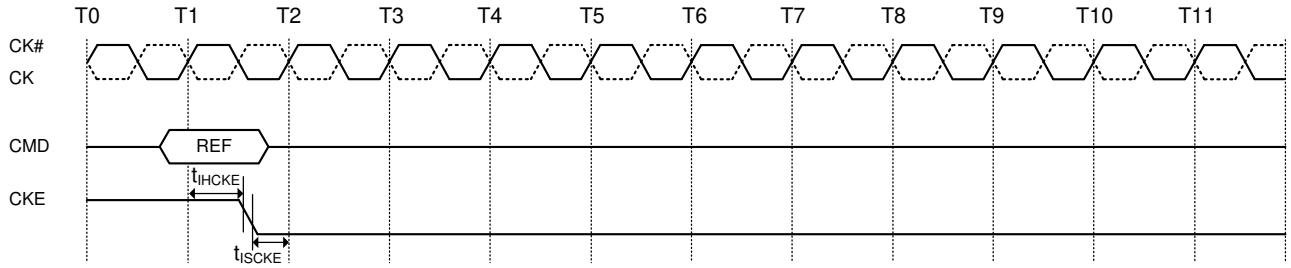
Note: CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + 4/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

Figure 72. Mode Register Read to power-down entry



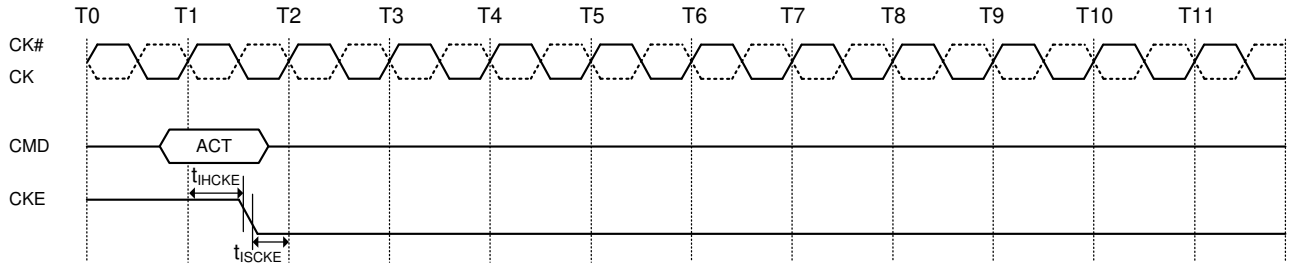
Note: CKE may be registered LOW t_{MRW} after the clock on which the Mode Register Write command is registered.

Figure 73. MRW command to power-down entry



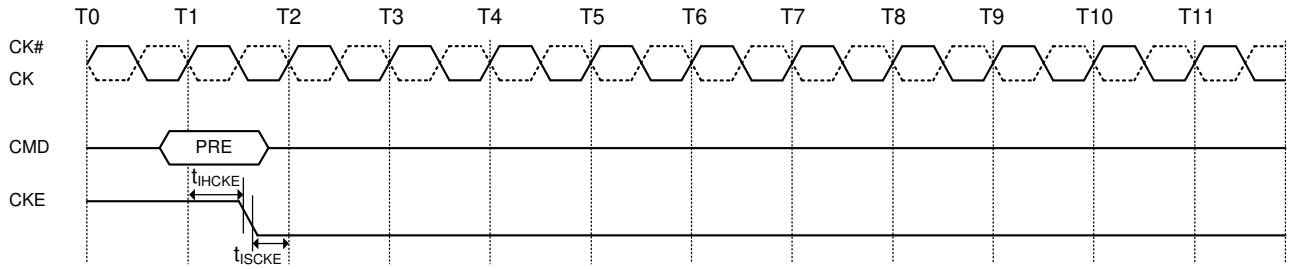
Note: CKE may go LOW t_{IHCKE} after the clock on which the Refresh command is registered.

Figure 74. Refresh command to power-down entry



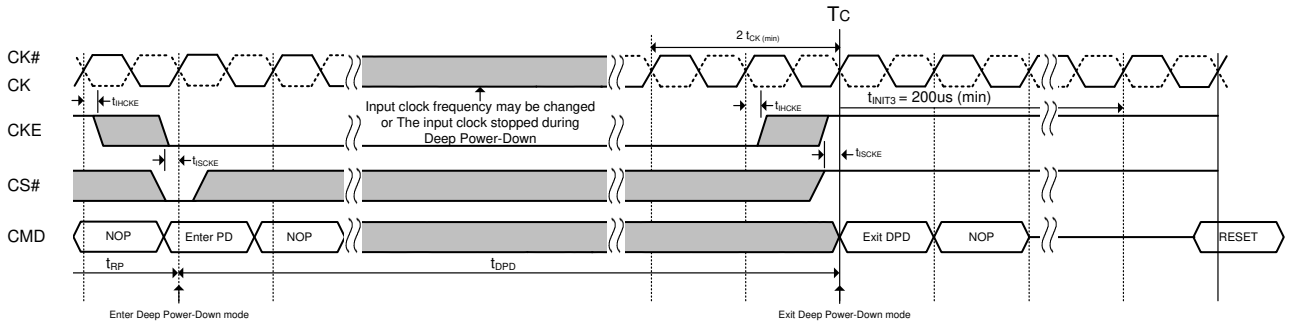
Note: CKE may go LOW t_{IHCKE} after the clock on which the Activate command is registered.

Figure 75. Activate command to power-down entry



Note: CKE may go LOW t_{IHCKE} after the clock on which the Preactive/Precharge/Precharge-All command is registered.

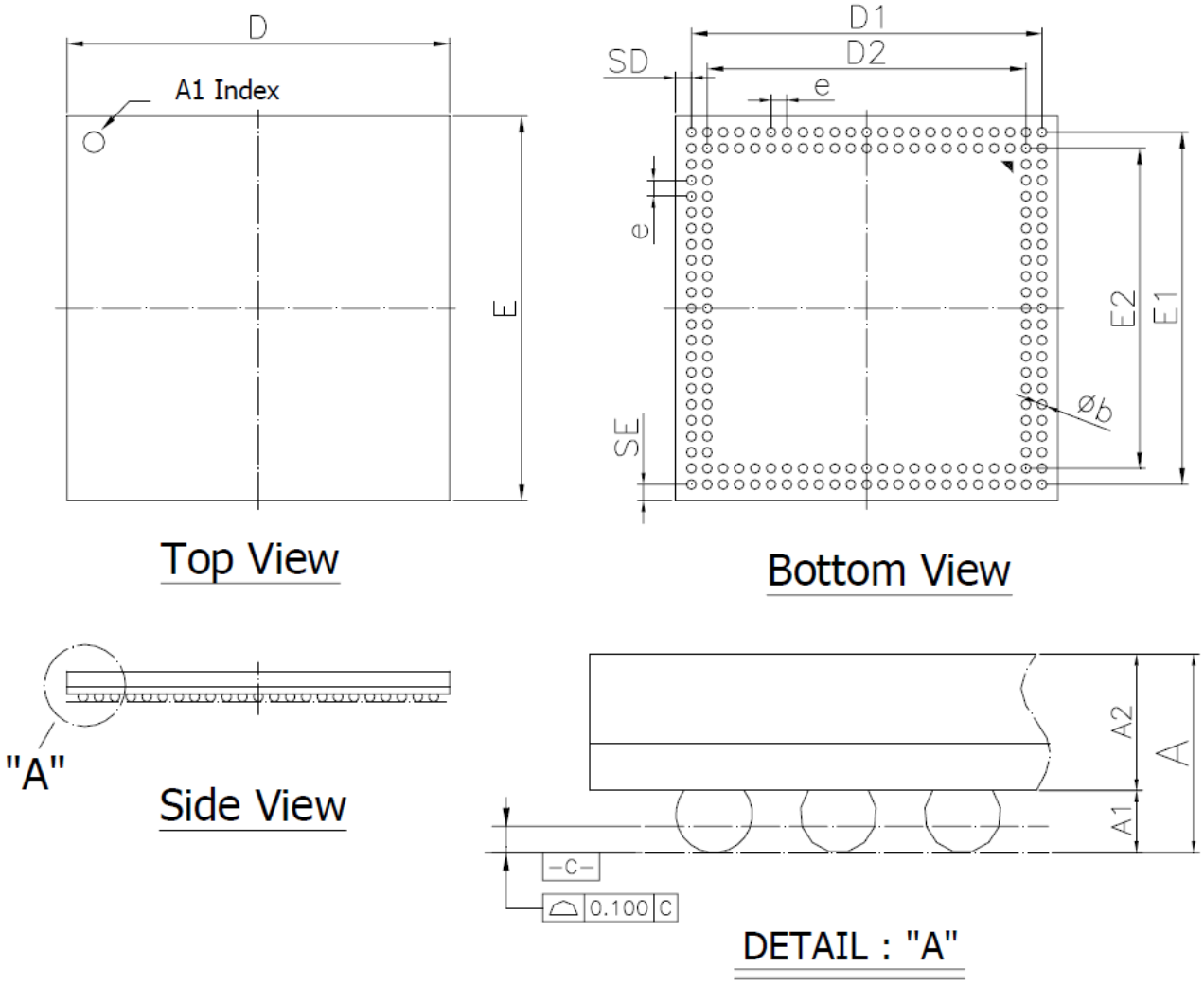
Figure 76. Preactive/Precharge/Precharge-all command to power-down entry



Notes:
1. Initialization sequence may start at any time after Tc.
2. t_{INIT3}, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see section "Power-up, Initialization, and Power-Off".
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure 77. Deep power down entry and exit timing diagram

Figure 78. 168-Ball FBGA Package 12 x 12 x 0.9mm(max) Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.035	--	--	0.900
A1	0.007	--	0.011	0.180	--	0.280
A2	0.020	--	0.025	0.525	--	0.635
D	0.469	0.472	0.476	11.90	12.00	12.10
E	0.469	0.472	0.476	11.90	12.00	12.10
D1	--	0.433	--	--	11.00	--
E1	--	0.433	--	--	11.00	--
D2	--	0.394	--	--	10.00	--
E2	--	0.394	--	--	10.00	--
SD	--	0.020	--	--	0.500	--
SE	--	0.020	--	--	0.500	--
e	--	0.020	--	--	0.500	--
b	0.010	0.012	0.014	0.25	0.30	0.35