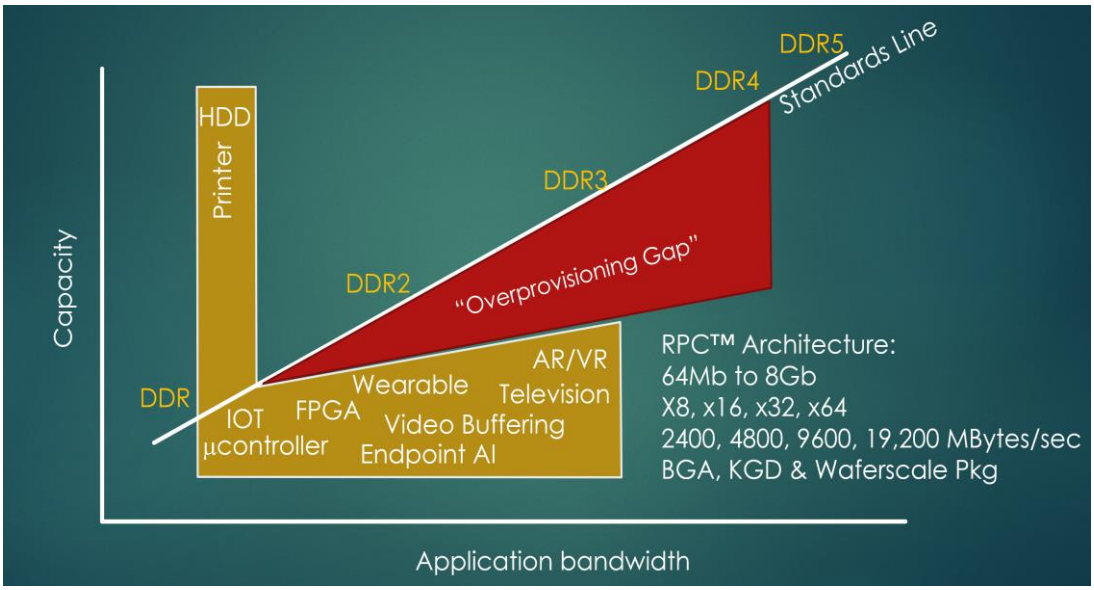
Reduced Pin Count (RPC®) DRAM

Etron Technology Inc

Feel "trapped" following the over-provisioned High Cost Memory Standards Road Map?



Memory Standards Road Map Overprovisions Emerging Markets

The Memory Standards Roadmap may serve the high performance, high density markets (and high cost) well BUT it HIGHLY overprovisions the new emerging markets in pin count, density, speed, and complexity! It's just overkill.

Etron Technology Inc. listens to their customers and not only provides standard memory products but also new innovative market solutions.

New DRAM Architecture

One example of listening to a customer's need, Etron developed a new evolutionary memory architecture: **A Reduced Pin Count DRAM.** This innovative patent pending architecture is an enabling solution to the new emerging markets of IOT, AR/VR and AI. It uses less than half the pins of a standard DDR3 memory yet still delivers low power, high speed and uses DDR3/LPDDR3 signaling.

OVERALL SYSTEM COST SAVINGS

With fewer signal pins and a smaller footprint the overall system cost can be significantly reduced. Controller cost is less, signal layout less complex, overall footprint is reduced, and advanced process nodes aren't required to meet the application requirements.

Contact Etron Sales for more information:

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RPC DRAM FEATURES:

Reduced Pin Count Architecture

- Less than half the pin count of a standard DRAM
- Only 22 Active signals
- Supports overlapped row/column operations
- Random addressing at full bandwidth

High Performance

- Bandwidth > DDR3 with < ½ the signals
- Low Power: No DLL, Deep Power-Down Mode
- DDR3/LPDDR3 Signaling
- Up to DDR2400 signaling speed
- X16 device: 4.8 GBytes/sec @ DDR2400

Low Cost Package Options

- First DRAM offered in WLCSP (lowest cost pkg)
- DDR3 96 ball PCB footprint is 10X larger than RPC
- Stacked Die MCPs
- X32 DDP in same package as DDR3 X16 package

Scalable Density and Configurations

- 64Mb to 8Gb
- X16, X32, X64

Cost Effective Miniaturization

- Smallest Package size available – WLCSP
- Same BW as DDR3 with <10% the footprint
- Controller size and complexity greatly reduced
- Overall PCB size and complexity reduced

See www.etronamerica.com

DDR3 – LPDDR3 – RPC DRAM Comparison

Feature/Option	DDR3	LPDDR3	RPC DRAM	RPC DRAM Advantage
Capacity/Package	1Gb - 8Gb	4Gb - 48Gb	256Mb – 8Gb	Low Density Optimal for Video Buffer / IoT
Bus Data Xfer Rate	800 – 2133 MT/s	1333 / 1866 MT/s	800 – 2400 MT/s	High Speed Data I/O Speeds
Bus Clock Frequency	400 – 1066 MHz	400 – 1066 MHz	400 – 1200 MHz	High Band Width With <4 CLKs restart
Voltage	1.5V	1.8V	1.5V	Single power source 1.8V for speed
Low Voltage Option	1.35V	1.2V	1.35V, 1.20V	Lower power, Speed 1.2V, 1.35V Options
Vref input	CA, DQ	CA, DQ	Vref	Power and Cost savings
Package Size	9 x 13.5mm FBGA	Varies, VFBGA	1.96 x 4.63 mm WLCSP 8 x 8 mm FBGA	Very Small foot print Cost savings, PoP
Ball Pitch	0.8 mm	0.4, 0.5 mm	0.4 mm WLCSP 0.8 mm FBGA	Pad Layout Optimal for KGD Option
Ball Count	96	168,178,216, 253,256	50 WLCSP 54 FBGA	Small PCB foot print Cost savings
Switching Signals	49	49	22	Reduced Pin Count, Less noise, Low cost, Easier layout, Less controller signals
Input Buffers	CK, CKE, CS, DM[0:1], RAS, CAS, ODT, WE, BA[0:3], ADDR[0:14]	CK, CS, CKE, ODT DM[0:7], CA [0:9]	CK, CS, STB	CMD/ADD multiplexed on I/Os and to Serial Port
I/Os	x4, x8, x16	x32, x64	x16, x32, x64	High I/O fewer inputs
Internal Banks	8 128Mbits/bank min	8 512Mbits/bank min	4 64Mbits/bank	Up to 4 open pages for optimal streaming
Burst Modes	BC4, BL8	BL8 only	Seamless, R/W toggle capable	Seamless burst cycles with Infinite duration
DLL	Required	n/a	n/a	Quicker bus up / turn time, Less power
Signal Termination	ODT / External	ODT / External	Selectable Series and/or VTT Parallel Terminated	Low power, HS PTP Applications
Rtt values (ODT) ohms	120,60,40,30,20	120,60,40,30,20	Optional ODT 27,36,40,51.4,60,90,120	Configurable, better voltage margin, less power
DQ Bus	SSTL_15	HSUL12	HSUL12	Lower power Higher speeds

Table 1-1. Product Information

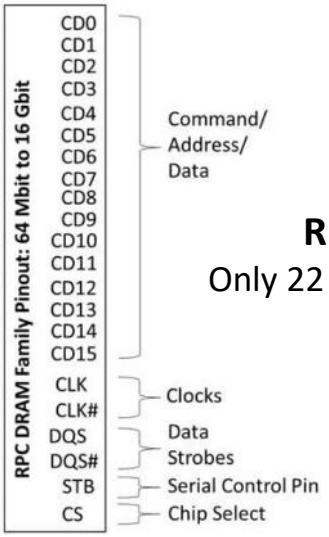
Part Number	Power Supply	Maximum Data Rate	Package Type	Availability
EM6GA16LGDA	V_{DD1} = 1.5V V_{DD}, V_{DDQ} = 1.5V	2400 MTPS/pin	KGD	TBD
EM6GA16LBMA			FBGA	TBD
EM6GA16LCAEA			WLCSP	TBD
EM6GA16LGDA		1866 MTPS/pin 1600 MTPS/pin	KGD	Now
EM6GA16LBMA			FBGA	Now
EM6GA16LCAEA			WLCSP	TBD
EM6HA16LGDA	V_{DD1} = 1.35V V_{DD}, V_{DDQ} = 1.35V	1866 MTPS/pin 1600 MTPS/pin	KGD	TBD
EM6HA16LBMA			FBGA	TBD
EM6HA16LCAEA			WLCSP	TBD
EM6MA16LGDA	V_{DD1} = 1.5V V_{DD}, V_{DDQ} = 1.2V	1600 MTPS/pin	KGD	~~TBD~~
EM6MA16LBMA			FBGA	~~TBD~~
EM6MA16LCAEA			WLCSP	~~TBD~~

GD: indicates Known Good Die
BM: indicates 8 x 8 x 1.2mm FBGA package
CAE: indicates Wafer Level Chip Scale Packages
A: indicates Generation Code

Now Sampling!

RPC DRAM Key Features:

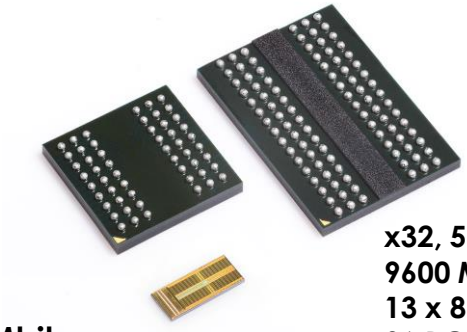
- Power Supplies: VDD = VDDQ = 1.2V, 1.35V or 1.5V (+/- 5%)
- DDR3/DDR3L bandwidth using 22 or 24 switching pins; 40 total pin count;
- Burst mode operation capable of seamless burst cycles of infinite duration even using random addressing
- Sequential and streaming addressing modes
- Double Data Rate (DDR) architecture
- Pipelined page activations
- 4 internal banks, supports bank interleave
- Low Power physical layer:
  - no PLL/DLLs
  - LPDRR3 HSUPL12 compliant signaling
- *Sequential and random addressing modes*
- *Differential input clock (CLK/CLK#)*
- *Differential bidirectional strobe (DQS/DQS#)*
- Full bank auto burst refresh
  - 64ms @0C =< Tc =< +85C
  - 32ms @85C =< Tc =< +95C
- Supports Point to Point & multi-drop applications
  - Programmable series terminated output driver option for low power high speed PTP use
  - ODT for other topologies
- Optimized Pad layout for Package on Package (PoP) applications and for stacked die MCPs
- Die-sized packaging options:
  - Known Good Die (KGD)
  - 50 ball Wafer Level Chip Scale Packages (WLCSP) for small PCB footprint
  - 8 x 8 mm 54 BGA 0.8mm Pitch



RPC DRAM
Only 22 Switching Signals

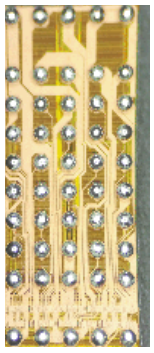
Package Offerings

x16, 256 Mbits
4800 MBytes/sec
8 x 8 mm
54 BGA
0.8 mm pitch



x16, 256 Mbits
4800 MBytes/sec
2 x 4.7 mm KGD &
50 WLCSP, 0.4 mm pitch

x32, 512 Mbits
9600 MBytes/sec
13 x 8 mm
96 BGA, 0.8 mm pitch



256Mb RPC DRAM DIE & WLCSP