# Legacy DRAM Finds Its Way to the Edge

By Gary Hilson 02.05.2020

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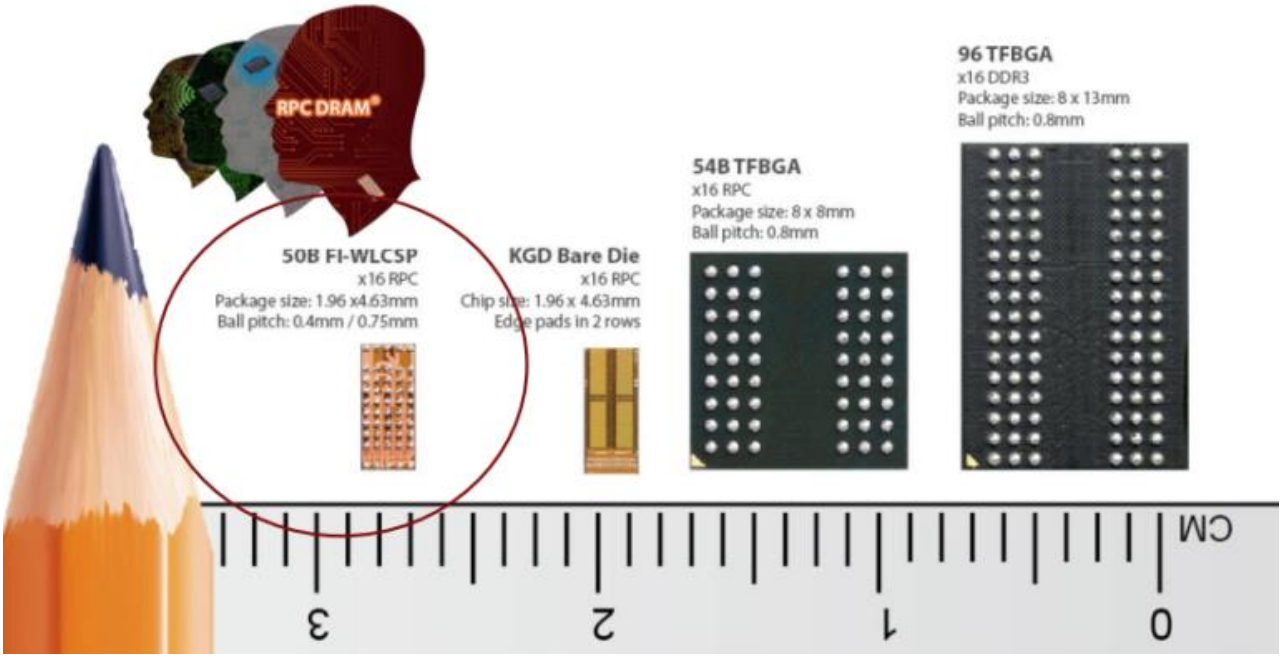
TORONTO — There has been plenty of discussion about how emerging memories might address opportunities created by the Internet of things (IoT) and obviate the need for expensive options such as SRAM. One company thinks low-pin DRAM may be the answer.

Richard Crisp, vice president and chief scientist for imaging and memory product development at Etron, said the company's DRAM represents a divergence from traditional architecture along the JEDEC road map to address applications that don't require the growing density, high pin speed, or all the bandwidth available in the latest DDR4, which has a minimum capacity of four gigabits. "There are a lot of applications out there that use significantly less than one gigabit worth of memory," he said. "There's interest in just having right-sized memories that are easy to use."

That's the impetus for Etron, which is looking to provide just enough DRAM to meet application needs while reducing the pin count of a typical DDR-type memory, said Crisp. And as the company went down the path of developing a small footprint, low pin-count memory, the world became interested in artificial intelligence (AI). "We started this without really thinking about AI at the time, but it sort of happened, and lo and behold we have an interesting solution for it."

A typical AI scenario is one where endpoints gather all sorts of data to send to a centralized cloud for processing with a big networking layer that interconnects both ends. But Etron likes to differentiate between endpoints and the edge, said Crisp, where an endpoint is a sensor gathering data from the external world, and the edge is a local, centralized computer that may do some aggregation of multiple sensors' data into a common stream with a fairly high performance media processor. This edge computer would do its own analytics on the stream before sending some intelligence to the cloud, he said, thereby requiring more performance than the endpoint, but still within some size constraints.

Etron's answer is a reduced pin-count (RPC) DRAM to support AI edge applications where they need a reasonably large amount of storage for data, such as reference images, and high enough bandwidth so that data can be processed quickly, said Crisp. RPC DRAM can provide the off-chip memory necessary, he said, but only in Fan-In Wafer Level CSP (FI-WLCSP) packages, which are very small and eliminate the substrate as well as any wire-bonding or flip-chip assembly steps.

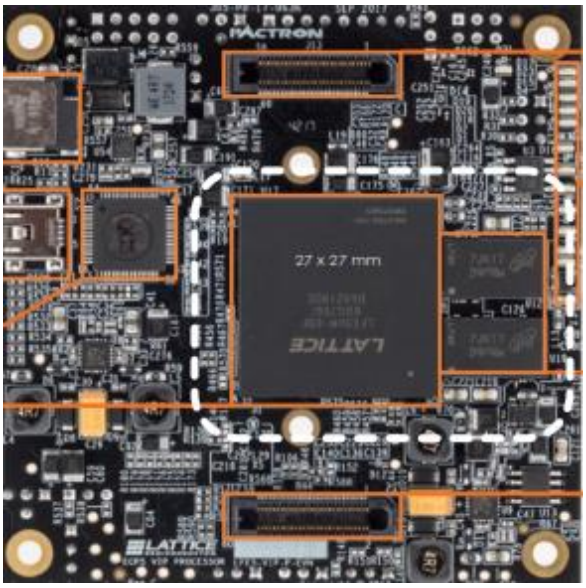



*Etron's RPC DRAM can be put in Fan-In Wafer Level CSP (FI-WLCSP) packages, which are very small and eliminate the substrate as well as any wire-bonding or flip-chip assembly steps. (Source: Etron)*

One company that sees potential in Etron's product is Lattice Semiconductor, which incorporated the RPC DRAM because of its very small form factor, said Kambiz Khalilian, Lattice's strategic marketing director. "What it allows you basically is the same performance as a standard DRAM but at a lower pin count." He said it's ideal for many of the "deep edge" applications Lattice supports where the performance/trade-off really matters. It enables data to be processed where it makes the most sense — including the edge — in a small form factor at low power where the bandwidth isn't available to send all data back to a server for processing.

Lattice complements the high performance and small footprint of its FPGA with the high bandwidth of the Etron RPC DRAM in its low pin count miniaturized WLCSP package, which uses less than half the signals of conventional DDR solutions. The pin count savings translates into reduced FPGA resource demands for the memory interface and smaller component footprints on a smaller PCB assembly.

Khalilian said that in some scenarios there needs to be more memory than what's embedded in Lattice's FPGA. "That's where these RPC DRAMs then come into play." And in a lot of edge camera applications, for example, each square millimeter matters. Adding further appeal to the RPC DRAMs is that they can be stacked on a board and still leave room for flash if needed, which not only optimizes layout but also addresses trade-offs among power, performance, and size.



Etron's road map began with a 75 x 75 mm three-board stack that included 27 x 27 mm Lattice FPGA and 13 x 9 mm DDR3 DRAM. (Source: Etron)

The fact that a customer has found merit in the technology and has incorporated it into a product is a sign the Etron concept has potential, said Jim Handy, principal analyst with Objective Analysis. And its use of a serial interface with a low pin count is where the industry is heading. However, it's using relatively low density, legacy DRAM to address an emerging use case: being able to process more data inside at edge — which in turn minimizes the bandwidth needed between the device and the server farm, he said, such as is the case with smart security camera designs. "If you put a lot of intelligence near the camera, then you don't need a whole lot of bandwidth because you can do facial recognition and then send a note back to the server."

Most companies offering low density DRAMs today, such ISSI and Alliance Memory, are doing so to keep older products alive because the legacy memory was discontinued by the larger players such as Micron. "There's a need for something like that that's too small for the majors to want to bother with," Handy said. Etron has taken the unusual step of going and rethinking and redesigning something that people would think of as a legacy density. "They end up getting something that's cheaper than the same size SRAM and that they can also put into a low pin count package."

He said the main challenge for the company is it's creating its own market for its technology. "Since they've aimed themselves squarely at Internet of things then that market does have a lot of room to grow."