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A Short Bio of Dr. Nicky Lu

As an inventor, researcher, professor, engineer, design architect, serial entrepreneur, and chief executive, Dr. Lu has dedicated his career to the worldwide IC design and semiconductor industry. He is the Founder of Etron (CEO/Chairman)/eYs3D/eEver/GTBF and the Co-Founder of GUC/Ardentec, Distinguished Research Chair Professor and Outstanding Alumnus of National Taiwan University (NTU), an IEEE Fellow, and a member of National Academy of Engineering (USA). Dr. Lu received the B.S. degree in electrical engineering from NTU and the M.S. and Ph.D. degrees in EE from Stanford University. Dr Lu is a recipient of the "IEEE 1998 Solid-State Circuits D.O. Pederson Award" for his leading contributions in high-speed dynamic memory design and memory cell device technology. In addition, Dr. Lu holds over 51 granted and 50 pending U.S. patents and has published more than 60 technical papers.

Question 1: Your educational journey is impressive. Starting in Taiwan, you earned your bachelor's degree before pursuing an M.S. and Ph.D. in electrical engineering at Stanford University. Can you tell us about the experiences or subjects that sparked your interest in this field? Were there any role models or mentors who guided your choice to pursue a career in electrical engineering?

Dr. Lu: In Taiwan, there is a nationwide university entrance examination where every student is ranked, and those with higher ranks can choose their preferred school and major. When I took the exam in 1971, I chose the National Taiwan University Electrical Engineering (NTUEE) Department as my first choice, which has consistently held the top position for STEM majors. It only admitted the top 110 students out of 100,000 examinees.

At that time, Taiwan had already developed a strong infrastructure in electrical engineering and electrical systems. However, knowledge about electronic systems was relatively limited. But I understood that electronics had the potential to make radios and TVs much smaller in physical size. So, I was determined to major in Electrical Engineering and focus on electronics.

Even though I had opportunities to pursue careers in medicine, business, or law, I firmly believed that the future trend was moving from Electrical Engineering to the booming field of electronics in the coming decades. Therefore, I chose to major in NTUEE.

During my senior year, Dr. Simon Sze was a visiting professor who taught a course on "Semiconductor." At that time, radios used vacuum tubes, and TVs used cathode ray tube (CRT). Professor Sze shared the history of the transistor, which was created in 1947 by William Shockley, Walter Brattain, and John Bardeen. Transistors had the potential to revolutionize telecommunications. The trend towards miniaturization looked very promising.

It was the time when solid-state circuits were replacing traditional vacuum tubes for major components in electronics. Around the same time, Stanford University established an experimental silicon processing facility for doing integrated-circuits research under the leadership of Professor Jim Meindl, who set up the first IC

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laboratory in a university in USA, equipped with advanced tools for realizing new inventions.

Professor Sze encouraged me to pursue advanced degrees abroad, especially at Stanford. In 1967, he was the inventor of non-volatile devices used in Flash memory. Later, my Ph.D. advisor at Stanford, Professor Meindl received the "2006 IEEE Medal of Honor" for his pioneering contributions to microelectronics, including low power, biomedical applications, physical limits, and IC interconnect networks. Many Silicon Valley startups were founded by his Ph.D. students. Both Professor Sze and Professor Meindl became my role models, setting an example for me to strive for excellence in my career.

Question 2: During your tenure at IBM Research and IBM HQs from 1982 to 1990, you made remarkable contributions to the semiconductor industry. Notably, you invented the SPT (Substrate-Plate Trench) DRAM cell, utilizing a novel 3D trench-capacitor structure, and created high-speed DRAM chips/circuits that had a significant impact. Could you discuss the challenges you faced during the development of these innovative technologies? What strategies did you employ to ensure their successful implementation and widespread adoption?

Dr. Lu: After completing my Ph.D. studies at Stanford under the guidance of Professor Jim Meindl, he recommended that I join the group led by his college/Ph.D. classmate, Dr. Bob Dennard, at IBM. Dr. Dennard was not only the inventor of the 1T1C DRAM cell but also the pioneer of Scaling Theory. At IBM, I had the privilege of working alongside many semiconductor industry masters, including Dr. Lewis Terman, Dr. Hwa Yu, and Dr. Dennard, who instilled in me the belief that "you must make some significant inventions and realize them into manufacturing for products in order to establish your reputation and position at IBM Research."

I devoted all my time to research at IBM. Around 1.5 years into my tenure at IBM, I invented the 3D trench-capacitor DRAM cell, a groundbreaking concept that uses the silicon substrate as the counter-electrode plate for the DRAM capacitor, leading to several other inventions.

At that juncture, IBM was manufacturing 1Mb DRAM using NMOS technology. The decision was made to utilize my invention as a technology driver and blueprint to establish and pioneer the world's first 8-inch wafer fabrication facility (wafer fab) and initiate a major transition to CMOS technology. This leap validated the viability of both logic circuits and 3D DRAM Cells, and CMOS technologies. The result was the production of the world's first 4Mb DRAM manufactured in large volume at an 8-inch wafer fab, marking IBM as the first company to deliver a 4Mb DRAM product worldwide. These DRAMs found their application in IBM mainframe computers and supercomputers.

To enable mass production of this innovative product, numerous key technologies for modern semiconductor manufacturing were developed. Notable examples include chemical-mechanical polishing (CMP) for planarizing surfaces, tungsten stud (W-stud) technology for connecting metal interconnectors to access semiconductor transistors, and an anisotropic etching technique of using reactive ion etching (RIE) for creating high-aspect-ratio trenches with a ratio over of 200:1. The trench capacitor serves as a significant charge reservoir, stabilizing voltage variations during transistor switching, in many present IC products.

What's most crucial is that these technologies were designed not just for a single generation of products but with the vision of spanning three to five generations, a concept inspired by Dennard's Scaling Theory. To this day, many of these inventions continue to be integral in modern semiconductor foundries.

Question 3: What motivated you to transition from IBM and embark on your journey in the early 1990s, where you played a pivotal role in shaping Taiwan's semiconductor industry and positioning it prominently today? We are curious to learn about the challenges you encountered while developing Taiwan's 8-inch-wafer and advanced logic/SRAM/DRAM technologies.

Dr. Lu: In my last 1.5 years at IBM, I was promoted to serve as the CEO's shadow, responsible for overseeing worldwide semiconductor technology development, proposing business strategies, and advocating for the R&D group. During this time, I observed IBM's high-speed DRAM being transferred to IBM Yasu fab in Japan. This experience taught me how to navigate the challenges of coordinating a cross-Pacific project between the U.S. and Japan, despite the significant time zone differences in 1980s when telecom is not so convenient like today's. Together, we developed a DRAM that was three times faster than any product available on the market at the time.

In the 1980s, the Taiwan government was strongly committed to investing in the semiconductor industry and recognized the need for a technical leader who possessed expertise in design, architecture, process, and technology. Dr. K. T. Li invited Dr. Morris Chang to participate in this initiative, and Morris proposed a foundry model that required design and process experts to drive technological development. KT then invited me back to Taiwan so that I could start up Etron Company, with the responsibility of defining the device technology and DRAM/logic chips necessary to enable a modern 8-inch

CMOS fab capable of manufacturing logic, SRAM, and DRAM. This opportunity allowed me to repay the knowledge and expertise that Taiwan had invested in me.

Leaving the comfort and well-organized environment of IBM, I joined Taiwan's "National Submicron Project" to contribute to the development of Taiwan's semiconductor industry. From 1990 to 1993, the Submicron Project successfully built a world-class 8-inch fab for mass-producing 16Mb DRAM and 4Mb SRAM. Importantly, the fab was designed to be scalable for advanced nodes, following the principles of scaling theory.

This transformation was characterized by two major goals: transitioning from the 1um technology node to 0.5um and increasing DRAM capacity from 4Mb to 16Mb. Everything had to start from scratch, and the challenge was to achieve this significant R&D and manufacturing leap within just four years. The key to our success lay in our ability to define a highly intelligent technology framework with well-established ground rules. This framework enabled us to **release five arrows simultaneously**: process, device, design, fab construction, and the development of an ecosystem and manufacturing infrastructure in Taiwan, including the introduction of advanced equipment and materials from overseas suppliers. Each of these areas presented numerous variables, necessitating meticulous consideration.

Every major stakeholder in the project had to master their specific task: K. T. Li provided crucial government financial support which ITRI needed, Morris Chang, drawing from his top-level executive experiences, developed the business model, C. Y. Lu led the big national technology project and built all CMOS processes and fab construction, and I was responsible for chip design, defined device structure, and advanced both architecture and process optimization for production. We were supported by a dedicated team of 200 new college graduates. We executed our grand plan with unwavering diligence.

I recall that CY and I organized a very solid but tough review meeting and exchanged work progress every night, mostly off hours to mid-night. Despite our tight schedule, we were committed to respecting others' patents, a principle I held dear due to my extensive patent training at IBM. This commitment ensured that our self-developed technologies would uphold the trust that Taiwan's government and K. T. Li had placed in us.

By 1993, Taiwan had successfully equipped itself with advanced, self-developed technology and world-class semiconductor products, marking a significant milestone in the country's semiconductor industry.

Question 4: As a visionary in the field, you have been a strong advocate for pioneering technologies like IC heterogeneous integration and the new Silicon4.0* Era. What fuels your passion for innovation? Could you share the strategies you employ to maintain a constant drive for progress, continuous learning, and staying at the forefront of technological advancements?

Dr. Lu: I'd like to reflect on this question with the benefit of hindsight. As the CEO of a fabless company like Etron Technology Inc., survival depends on continuous innovation and breakthroughs. The need to survive constantly drove me to push the boundaries of what was possible, for example, even up to the last four years, I have submitted over 50 U.S. patents, optimizing integrated circuits and semiconductor technologies and devices for the next decade.

I attribute my unwavering drive for progress, continuous learning, and staying at the forefront of technological advancements to three major factors:

First, the instinct to survive. The competitive landscape of the semiconductor industry demands continuous innovation, and this survival instinct has been a significant motivator for me.

Second, self-motivation has played a crucial role. I am deeply honored that my Stanford Ph.D. advisor and an intellectual titan of microelectronics and ICs, Professor Jim Meindl, recognized me as his "Top-Notch Student" on my Ph.D. dissertation approval. This acknowledgment has served as a constant source of inspiration and motivation.

Third, the imperative to prevent patent infringement lawsuits and to maintain technology independence have driven me to build an extensive portfolio of inventions.

In 1998, Etron went public, and IBM and Intel became our customers. Our cooperative model involved them specifying their requirements, and I would produce the products accordingly. They had a need for chip miniaturization and packaging. At that time, even multi-chip modules (MCP) were manufactured as package-in-package, necessitating packaging, and burn-in for reliability. This challenge prompted me to explore how to conduct burn-in tests on individual dice without packaging; essentially, burning in the dice using specially-designed on-die circuits to screen out faulty bits while maintaining the same 10-year reliability as packaged dice. This product concept became known as "Known Good Die (KGD)." My first customer for this innovative approach was Intel. I utilized TSMC technology with my innovative circuit design technologies to produce KGD in either SRAM or DRAM dice, which was then packaged with Intel's flash dice, respectively. This invention propelled Intel's chip into a blockbuster product in the market, and Intel awarded Etron a Preferred Quality Supplier Award, featuring a public recognition in the Wall Street Journal in 2003. Dr. Morris Chang, a key figure in Taiwan's semiconductor industry, was delighted with this recognition: TSMC manufactured dice could now be sold as KGD, establishing a new era of Heterogeneous Integration (HI). At the time, Intel's famous slogan was "Intel Inside," but Etron's products were "Inside Intel." Besides Intel, Seagate also embraced Etron's KGD products, which were used in their cutting-edge miniature hard drives (HD), allegedly featured in the first-generation iPod.

In 2004, I had the honor of being invited to deliver a plenary talk at the International Solid-State Circuits Conference (ISSCC). In my speech titled "Emerging Technology and Business Solutions for System Chips" I coined the concept of "Heterogeneous Integration (HI)." Since my Ph.D., I never missed attending ISSCC, as it provided an exceptional venue for inspiration, competitive analysis, and trend observation.

In 2005, the Global Semiconductor Alliance (GSA) invited me to speak. During my speech, I shared my perspective that HI would become the silicon trend beyond Moore's Law and Dennard's Scaling. In the Silicon 4.0 era, non-Silicon materials such as GaAs, GaN, optical fibers, and more could be integrated into Silicon wafers or packaged alongside Silicon dice in the same package. In summary, Silicon 1.0 followed Moore's Law, Silicon 2.0 introduced 3D transistors like Trigate or FinFET, Silicon 3.0 saw the integration of analog dice, digital dice, RF dice, memories, and more into silicon-centric chips, and Silicon 4.0 embraces a diverse array of materials and components, including MEMS and optical devices, integrated with silicon dice.

Question 5: Over the past three decades, your remarkable contributions to the advancement of semiconductor technologies in Taiwan and the promotion of its semiconductor industry have garnered widespread recognition. Can you provide further insights into how these advancements, facilitated by the companies you co-founded and other stakeholders, have empowered Taiwan to establish itself as a leading supplier of crucial silicon products and wafers? Moreover, in what ways has Taiwan's position in the global high-tech industry and its contributions to the global economy been strengthened as a result?

Dr. Lu: My journey in the semiconductor industry began with the introduction to Carver Mead and Lynn Conway's visionary book, "Introduction to VLSI Systems" during my last class at Stanford. In this book, they envisioned a future for semiconductors characterized by synthesizable circuit design and flexible process technology to cater to different product lines. This idea left a lasting impression on me.

When I participated the Taiwan's National Submicron Project, I aimed to translate this vision into reality by crafting device frontend and backend design rules that were more flexible for both transistors and circuit designs. During that era, as process nodes transitioned from 0.7um to 0.35um, it necessitated the replacement of equipment to manufacture advanced products. During my tenure as Silicon Program Manager for the CEO at IBM, frequent visits to Japan provided me with an important insight. I discovered that Japanese fabs didn't reinvent new technology for every process node migration. They embraced forward scaling without abandoning the major construction rules of the previous-generation technology, enabling the reuse of most existing equipment and thus significantly reducing the development time for new technology. The key to this approach, adding up my experience of defining design rules for an IDM (Integrated Device & Manufacturing) Company was the adoption of innovative flexible foundry rules in order to serve more diversified customer needs.

Embracing this principle, I applied it in the Submicron Project to develop Taiwan-specific design rules. These rules enabled forward migration to new process nodes while adhering to reduced area demands dictated by Moore's Law. Expensive equipment was only employed at key steps in the process. T-rules were characterized by more generous design rules for scaling, resulting in forward/backward changes in compatible layout rules, but still keeping improved performance, lower power consumption, smaller die area, and reduced costs. Later it is recognized the paramount importance of flexible design rules in the upcoming foundry model to remain competitive.

From VLSI (very large-scale integration) to ULSI (ultra-large-scale integration) and then to GSI (giga-scale integration), Taiwan has emerged as a global supplier offering a valuable technology platform. This platform is characterized by its flexibility, cost-effectiveness, and rapid time-to-market capabilities, exemplified by the TSMC Open Innovation Platform. The backbone of this platform lies in its devices, equipment, and processes, all of which are designed to be more flexible and user-friendly for fabless companies; for example, the SMIF-box was adopted to relax the tighter demand on clean-room classification as needed by dimensional scaling, and the wise adoption of the alignment principle defined by ASML long-term used methodology.

In essence, for the logic-chip focused business model in Taiwan, the faster migration to new generation of process nodes embraces less elaborate tools, providing high quality and flexibility for designers. This approach has empowered Taiwan to establish itself as a leading supplier of critical silicon products and wafers, strengthening its position in the global high-tech industry and contributing significantly to the global economy.

Question 6: In addition to being a distinguished professional in the worldwide IC design and semiconductor industry, you have also actively participated in various technical committees and conference organizations. How has your active involvement in these activities influenced the field of semiconductor technology? What motivates you to take on these service roles, and how do you believe these roles benefit both individuals and the semiconductor community as a whole?

Dr. Lu: I have had the privilege of serving on the Technical Program Committee (TPC) for the International Solid-State Circuits Conference (ISSCC) from 1988 to 2012, dedicating 24 years to the review and selection of papers. Additionally, I've been actively involved as a panelist, moderator, and organizer for evening panels and sessions, earning recognition through winning the Best Evening Panel/Session award four times out of 12 invitations. My motivation for participating in these activities has always been to give back to the society that has provided me with so much. I've been humbly recognized as a global semiconductor key opinion leader, and with an equitable and open-minded approach, I've made it a priority to select papers for publication based solely on their merit.

I can vividly recall presenting my Ph.D. research at the First Symposium on VLSI Technology in 1981, with my professor, Jim Meindl, videotaping my speech. My research work ultimately secured a significant grant from DARPA for him and Stanford IC Lab. In the audience, Takeishi-san, the head of semiconductor R&D at Toshiba, congratulated me with the words, "Nicky, you did a great job." This experience left a lasting impression on me that our chip industry did respect individual contribution no matter how competitive we are from different institutions, and how respectful for our industry leaders to carry out more important mission on enhancing human civilization by our technical expertise.

I also contributed by serving on the TPC for the IEEE Symposium on VLSI Circuits (VLSI Symp.) from 1990 to 2021. During my tenure on these committees, I witnessed the remarkable evolution of semiconductor technology, from VLSI to GSI (giga-scale integration). I never saw my role on the TPC as merely a source of motivation, but rather as an invaluable opportunity. It allowed me to review and stay informed about the latest advancements in technology—a profound honor for someone deeply immersed in the world of semiconductors.

Throughout my career so far, I've been incredibly fortunate to work on pioneering projects such as IBM's DRAM Technology and later Taiwan's first 8-inch wafer fab. Today, technology has progressed to the point of 12-inch fabs. I consider myself a diligent researcher who has consistently prioritized serving our solid-state society over personal fame and fortune.

Question 7: In the field of semiconductor and IC design, especially in the era of artificial intelligence (AI), what do you find to be the most captivating trend? Could you share your vision for potential innovations that may emerge in the next few years? What breakthroughs or advancements do you anticipate, and how do you foresee their impact on industries and society as a whole?

Dr. Lu: As of 2023, one of the most captivating trends in the field of semiconductor and IC design is undoubtedly artificial intelligence (AI). In just the past 10 months, we've witnessed numerous breakthroughs in this high-tech arena.

First and foremost, AI technology has made significant strides, transitioning from convolutional neural networks (CNN) to transformer-based large language models (LLM). Machines are now capable of comprehending human knowledge. In an astonishingly short span, ChatGPT, for instance, has garnered over 100 million active users. This development is paving the way for closer collaboration between AI robots and humans, aligning with MIT's motto, "mens et manus," which translates from Latin to "Mind and Hand." Together, they hold the potential to shape a brighter future.

Secondly, the convergence of quantum computing and AI is on the horizon. In the coming years, we can anticipate discovering superior materials and methodologies for practical application to another computing-power boom, likely around 2030.

Thirdly, 2023 is witnessing the widespread deployment of autonomous cars, a technological advancement that promises to revolutionize transportation.

Fourth, the advent of room-temperature superconductors is an exciting prospect. AI and human collaboration may unlock new materials and methods to achieve this long-sought-after phenomenon.

Fifth, AI's predictive capabilities are poised to help humanity better prepare for natural disasters, such as floods and droughts. Given the challenges posed by climate change, driven in part by global warming, semiconductor technology combined with AI can serve as a guiding force, akin to a skilled hunting dog in search of solutions.

Sixth, the semiconductor industry is progressing towards the 1nm process node. While Moore's Law traditionally dictated that transistor density would double with each new generation of process technology, recent advancements have deviated from this trend, please see Table 1 below.

Nonetheless, there is ample room for innovation in achieving lower power consumption, increased speed, and reduced costs through the optimization of both monolithic and heterogeneous integration (MHI), as epitomized by the Silicon 4.0 era. It's projected that we use an optimized MHI method to catch up the desired performance and density targeted by Moore's Law in terms of "Peak Quoted Transistor Densities by volume (MTr/mm^3) rather than by planar area" (see Figure 1).

Table 1.
Comparison of Transistor Density (Unit: 1 Million/mm^2)

	Peak Quoted Transistor Density (MTr/mm^2)				
AnandTech	**Company A**	**Company B**	**Company C**	**Company D**	**If Obey Moore's Law**
22nm		16.5			
16nm	28.88 →				(28.88)
14nm		44.67	33.32		37.72
10nm	52.51		51.92		73.93
7nm	91.20	100.7	95.08		150.88
5nm	138.2		126.9		295.73
4nm	143.7	123.4			462.08
3nm	215.6				821.48
2nm				333.33**	1848.32
					↑ Further Calculations & Desired (Lu)

*ref1: https://en.wikichip.org/wiki/5_nm_lithography_process
**ref2: https://semiwiki.com/semiconductor-manufacturers/tsmc/298875-is-ibms-2nm-announcement-actually-a-2nm-node/

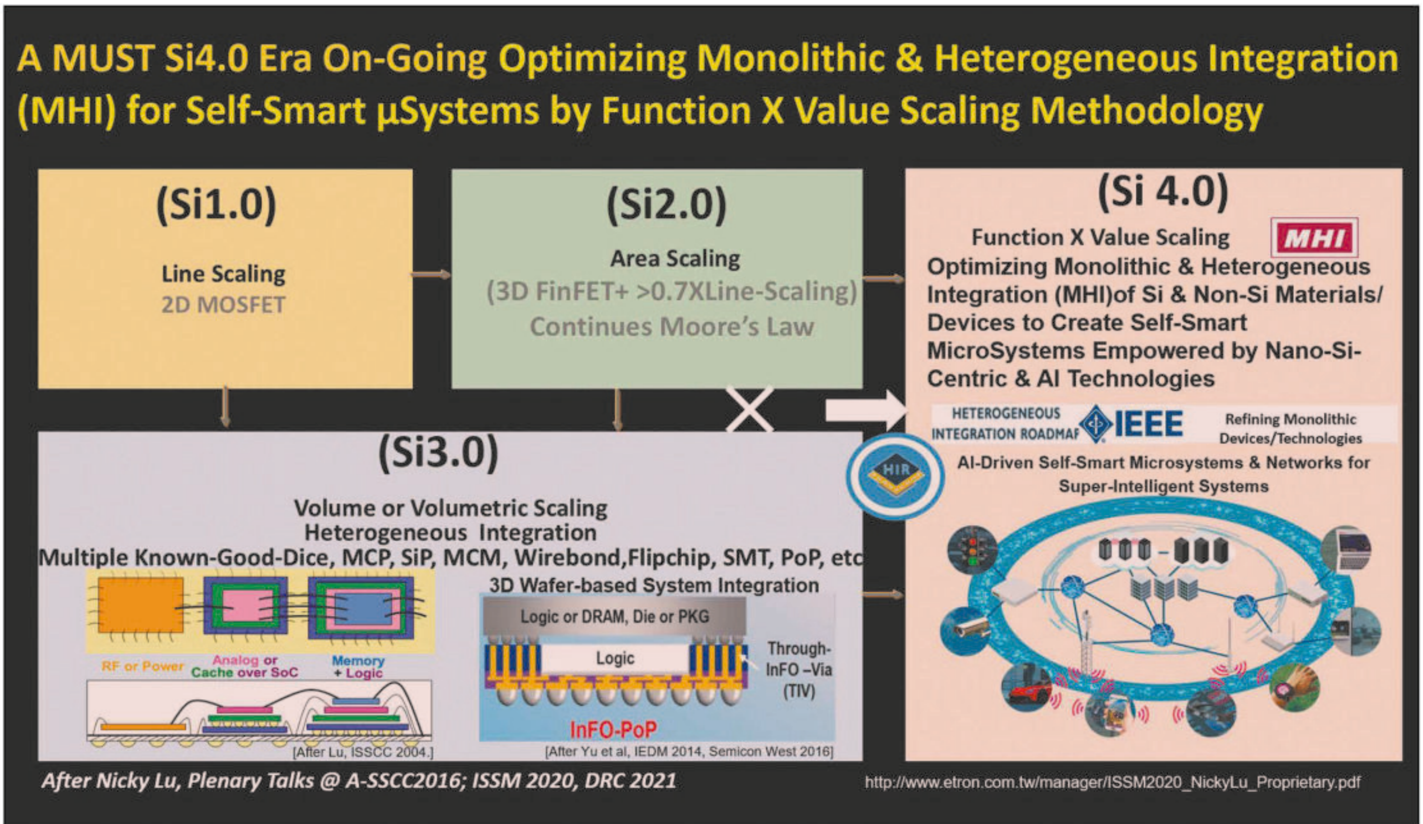

Figure 1. A Si4.0 era on-going optimizing monolithic and heterogeneous integration (MHI) for self-smart µSystems by function × value scaling methodology.

Additionally, we face challenges related to heat dissipation in stacked dice configurations.

My vision entails a commitment to continuous invention, both as a researcher and in my role as CEO. The spirit of invention remains a core trait of an IEEE member. I encourage all readers to persist in their pursuit of innovation to advance semiconductor technology further.

Question 8: As an esteemed figure in the fields of research, engineering, invention, design architecture, entrepreneurship, and executive leadership, your outstanding achievements have earned you numerous prestigious accolades and awards, including being recognized as a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) and a Member of the National Academy of Engineering (NAE). Reflecting on your extraordinary life journey, how do you personally define success? Additionally, what guidance or advice do you have for the younger generation?

Dr. Lu: This is indeed an excellent question. I am grateful to have received numerous honors and accolades from society. My fundamental belief has always been that "Real talent will eventually be recognized, and profits will come in due time." Fame and fortune are not the primary objectives one should pursue; they are outcomes, rewards that follow dedication and commitment. To succeed, one must develop their skills continuously, strive for self-improvement, and remain dedicated to the process of invention, creation, and realization.

The semiconductor industry offers an exciting and rewarding career path. With innovation and creativity, one can transform their work into an entire industry. The field is teeming with talented individuals capable of inventing and creating. With the ongoing developments in quantum computing, artificial intelligence (AI), heterogeneous integration (HI), and the march towards 1nm technology nodes, there are boundless opportunities for inventing, realizing breakthroughs, and enhancing the quality of human life.

In the semiconductor industry, success is ultimately defined by one's contributions. In this field, recognition and opportunities will come to those who make significant contributions. It's not about pursuing fame and fortune; they come naturally as a result of dedication and meaningful work.

To the younger generation, I offer the following perspective: Why do some view the semiconductor industry as tough? It might be because they seek quick success, akin to what is often achievable in software and AI. I don't fault this perspective.

In 2023, during an ISSCC evening panel, I shared an anecdote about a close friend of mine who works on Wall Street. He is a successful businessman and one day expressed envy towards me. He envied the fact that, even at the age of 50 at that time, I was still passionately working in the field I loved. He, on the other hand, desired to continue his work but his company didn't allow it because they think that over 45 could be too old. I told the audience in the panel discussion that in our society every youth can have the opportunity to make choices and should make your own decision at an early appropriate time. You have the chance to choose your own career path, and regardless of the choice, you should not have regrets. Just like in life, you can keep dating girls until you're old or at your age of 30 or so you decide to marry a partner for your life and to be a loyal partner, and neither choice is incorrect. The key is to make your career decision when you understand yourself on what you have passions and then move forward without regrets.

I've spent over 46 years in the semiconductor industry, and my son, Tim, who graduated from MIT and was an Associate Professor and by now has worked from an entrepreneur to a CEO of his own startup in the field of synthetic biology and gene medicine, he has followed what he likes and enjoys. When asked why he wanted to start his own company, Tim responded that he was simply following in his father's and his uncle's footsteps. My hope for IEEE members and indeed all individuals is that we recognize the unique opportunities we have in this world. We possess brilliant minds, and while we may lack wealth, we have the chance to work passionately on endeavors that matter. Our goal should be to achieve milestones and make a positive impact on the world. It is through our existence and our dedication to our work that we can change the world for the better. This is the spirit we should uphold, and together, we can achieve even greater things. Thank you for this interview.